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Highly Contrasting Static Charging and Bias Stress Effects in Pentacene Transistors with Polystyrene Heterostructures Incorporating Oxidizable *N,N′*-Bis(4-methoxyphenyl)aniline Side Chains as Gate Dielectrics

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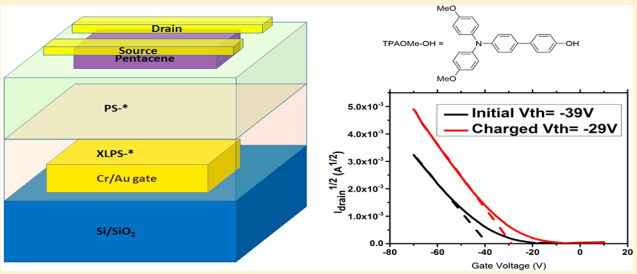
Supporting Information

ABSTRACT: Charge storage and trapping properties of polymer dielectrics govern the charge densities of adjacent semiconductors and greatly influence the on−off switching voltage (threshold voltage, V_{th}) of organic field-effect transistors (OFETs) when the polymers are used as gate insulators. Intentional charging of polymer dielectrics in OFETs can change V_{th} and affect the bias stress. We describe a chemical design and fabrication protocol to construct multilayer-stack dielectrics for pentacene-based OFETs using different polystyrene (PS)-based polymers in each layer, with oxidizable *N,N*-bis(4-methoxyphenyl)anilino (TPAOMe)-substituted styrene copolymers in arbitrary vertical positions in the stacks. Thermal, byproduct-free cross-linking of benzocyclobutene subunits provides integrity to the multilayer structure by preventing dissolution of the previous deposited layer. Neutron reflectivity data verified the multilayer morphology. We compared the V_{th} shift before and after charging the stacks by application of ±100 V across 0.5−1 μm total film thicknesses. Bias stress was the dominant effect in bilayer devices with a TPAOMe layer in contact with the pentacene, indicated by the direction of V_{th} shift associated with either polarity of external electric field. In structures with no TPAOMe subunit in contact with the pentacene, when charging with −100 V on top of the source and drain electrodes, electron injection from pentacene to dielectric was the major charging mechanism, again consistent with the bias stress direction. When charging with +100 V, bilayer devices without TPAOMe showed little change in V_{th}, suggesting there was no bias stress effect or charge injection in these devices for this charging polarity. For the bilayer devices with the TPAOMe layer in the bottom, and the trilayer devices with TPOMe in the middle, when +100 V was applied, the V_{th} shifts were opposite those expected from bias stress. Dipole formation or partial ionization of chargeable groups at the interface between the dielectric layers are likely polarization mechanisms in these cases. A simple analytical model supports the plausibility of these mechanisms. This work provides examples of both stabilization and shifting of V_{th}, and therefore controlling charge carrier density, in semiconductors overlying the dielectric multilayers.



INTRODUCTION

Electronics based on flexible materials are attractive for use on a wide variety of substrates including foldable, curved, and conforming surfaces for various applications.[1,2] Sensing, energy conversion, and memory devices have been made with organic semiconductors (OSCs) due to their possible transparent, flexible, and printable attributes.[3−7] Besides the OSCs, chargeable dielectric polymers that are easy to modify through molecular tailoring and can be easily processed in solution are considered promising candidates for the fabrication of transparent, flexible, and nonvolatile organic field-effect transistor OFET-based components.[8−10] More broadly, charge storage in polymer dielectrics can control the initial charge densities of OFETs and other semiconductor devices.[11,12]

Gate dielectric polymers have a great influence on the threshold voltage (V_{th}, the gate voltage beyond which on-state mobility is observed) of OFETs because the bulk and interface properties of polymers affect the number densities, energies, and mobilities of charger carriers in the OSCs.[13,14] V_{th} is a measure of free or trapped charge carrier density in the conductive path through a gated transistor semiconductor.

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Therefore, at a given gate voltage (V_g), the free or trapped charge carrier density changed by a charging process causes a different output current profile and thus a different V_{th}.

Charge trapping is common in dielectric polymers and can occur within the bulk dielectric or at the interface between the dielectric and organic semiconductor.[15] Methods to tune V_{th} and charge the device include charging of embedded grains or nanostructures and embedding a floating gate sandwiched between two dielectric layers.[16,17,8] An evaporated Au film embedded between polysilsesquioxane layers in poly(3-hexylthiophene) (P3HT)-based memory devices showed V_{th} shift after charging due to the electron transfer from the depletion region of P3HT to the Au floating gate.[18] A ZnO trap layer sandwiched between methyl silsesquioxane gel dielectric layers showed long retention time and low operating voltage.[19] Another way to modify V_{th} is to store charge in the bulk dielectric of a chargeable polymer. One example is poly(2-vinylnaphthalene),[20] which has quasi-permanent electret chargeability. Another is poly(vinylidene fluoride) (PVDF),[21,22] a ferroelectric polymer that has quasi-permanent dipole polarization that changes direction in response to an applied electrical field. Hydrophobic polymers such as those based on polystyrene showed stable V_{th} shift compared to hydrophilic dielectric polymers.[10] The effect of thickness on the charge trapping of single-poly(*N*-vinylcarbazole)-gate dielectric pentacene-based OFETs was investigated. The charge trapping capacity showed a Gaussian distribution along the thickness, and the surface tuning distance for charge injection showed exponential decrease.[23] On the basis of that, a single continuous dielectric was found to consist of a tunneling layer near the channel in addition to the chargeable bulk.

The bias stress effect may arise from charge trapping or detrapping at the interface between the semiconductor and gate dielectric. That results in charges becoming localized and immobile in the first case or freer to be transported in the second case.[24−26] In one experiment, delamination of OFETs showed that charge trapping in a stressed device only occurs in the gate dielectric.[27] Subtle physical and chemical effects at the interface affect the charge trapping, such as the presence of branching and chain ends greatly increasing the bias stress effect.[28,29] A fluorinated gate dielectric, which was highly hydrophobic and which altered the morphology and adhesion ability of the interface, showed the ability to decrease the charge trapping density at the OSC/dielectric interface, thus lowering the bias stress effect.[30] According to the accepted understanding of the bias stress effect as generally applied to p-channel (hole-carrying) OSCs, positive charge trapped in the dielectric interface leads to fewer mobile holes in the channel of the OSC for a given applied gate voltage and thus increases the magnitude of V_{th}.[27,31]

We have recently demonstrated[9] charge trapping and bias stress effects in pentacene-based OFETs with multilayer dielectrics composed of styrene copolymers. The substituents in these polystyrene (PS)-based polymers were triphenylamine (TPA) and fullerene (C_{60}). The former is a strong electron donor often used in OLED devices, and the latter is an electron acceptor. Devices with a bilayer gate dielectric in which a substituted-PS layer was on top and in contact with the pentacene were found to have a strong charging trapping effect as demonstrated by increased V_{th} shift. Meanwhile, devices with a trilayer gate dielectric were found to have decreased V_{th} shift, which could possibly be due to the polarization of the substituted PS in the middle layer compensating for the charging trapping or bias stress effects in the top layer. This paper established a method to introduce vertically localized functionality in single PS-based polymers and utilize charged heterostructures in various electronic devices.

In this paper, we constructed a series of PS-based multilayer dielectrics that show even more pronounced charging effects. We introduce a new substituent unit, *N*,*N*-bis(4-methoxyphenyl)anilino (triphenylamine-OMe, TPAOMe), which is a stronger electron donor than TPA.[32,33] Analogous to what we had done in previously published work,[9] we constructed three types of vertical multilayer structures in pentacene bottom gate OFETs with the substituted PS layer in the top, middle, and bottom. 4-Vinylbenzocyclobutene was used as the cross-linking subunit to ensure the integrity of the different vertical stacks and prevent any small molecular byproducts.[9] No inorganic dielectric was used, and the PS-based polymers were used as the sole gate dielectric materials. Different charging effects were observed as V_{th} shifts from multilayers with different vertical positions of the PS substituents, including stability to charging, bias stress, and charging counter to bias stress effects. V_{th} shifts were more obvious and more precise in the current work, and the directions of the shifts were generally consistent with what would be expected from bias stress. However, in two new and striking cases, the shifts were opposite from expectations based on bias stress, and for those cases, alternative polarizing mechanisms are proposed. A charge distribution model was correlated to the observed shifts, and effects of different leakage current levels were evaluated. The systems described in this work offer greater systematic modulation of static charge-induced semiconductor charge densities than has previously been achieved with polymer electret gates.

EXPERIMENTAL SECTION

Synthesis of PS-Based Polymers. *Synthesis of Diarylamine* ***3***. An oven-dried round-bottom flask was evacuated and backfilled with nitrogen to maintain inert atmosphere. $Pd_2(dba)_3$ (dba = dibenzylideneacetone, 25 mg, 0.03 mmol) and $P(tBu)_3HBF_4$ (16 mg, 0.05 mmol) were added to this flask, and the flask was placed under vacuum for 10 min. Then, *p*-methoxyaniline (0.5 g, 4 mmol), *p*-bromoanisole (0.5 g, 2.7 mmol), and sodium *tert*-butoxide (0.4 g, 4 mmol) were added under the flow of nitrogen gas, and the flask was placed under vacuum for 30 min, following which it was filled with nitrogen gas. 30 mL of freshly degassed, dry toluene was added via a cannula, and the reaction vessel was placed in a preheated oil bath at 105 °C. The reaction was continued under nitrogen for 10 h. After completion of the reaction, the reaction mixture was cooled to room temperature and filtered over Celite. Toluene was removed *in vacuo*. To the resultant slurry, 50 mL of deionized (DI) water was added, and the product was extracted into ethyl acetate. The product was purified using column chromatography using hexanes/ethyl acetate to obtain the product as an off-white solid. This was recrystallized from hexanes to obtain the pure product as needlelike crystals (0.43 g, 1.9 mmol, 70%). The ^{1}H NMR of the product was found to agree with previous literature.[34]

Synthesis of Triarylamine ***6***. An oven-dried round-bottom flask was evacuated and backfilled with nitrogen to maintain inert atmosphere. $Pd_2(dba)_3$ (18 mg, 0.02 mmol) and $P(tBu)_3HBF_4$ (12 mg, 0.04 mmol) were added to this flask, and the flask was placed under vacuum for 10 min. Then, **3** (0.45 g, 2 mmol), **5**[35] (0.8 g, 2.1 mmol), and sodium *tert*-butoxide (0.2 g, 2.1 mmol) were added under the flow of nitrogen gas. The flask was placed under vacuum for 30 min, following which it was filled with nitrogen gas. 40 mL of freshly degassed, dry toluene was added via a cannula, and the reaction vessel was placed in a preheated oil bath at 105 °C. The reaction was continued under nitrogen for 3 h. After completion of reaction, the

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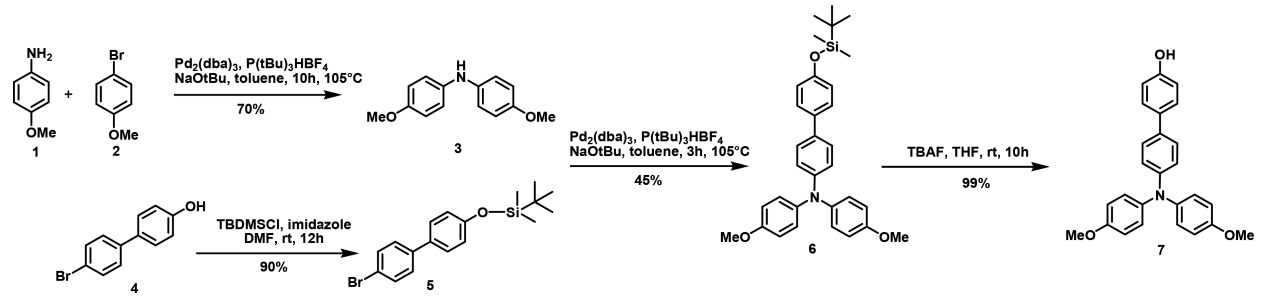
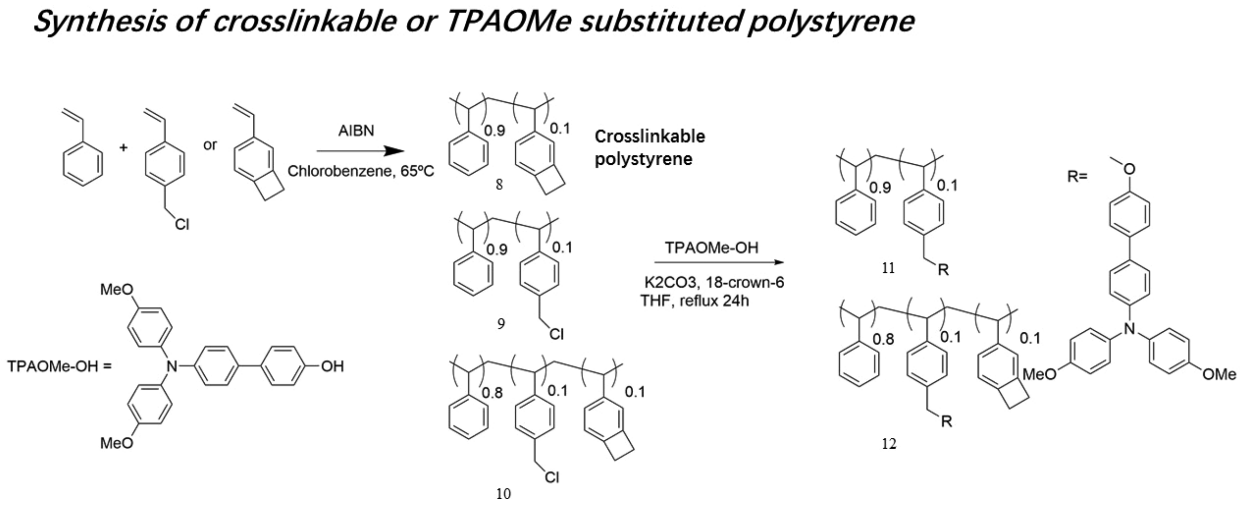
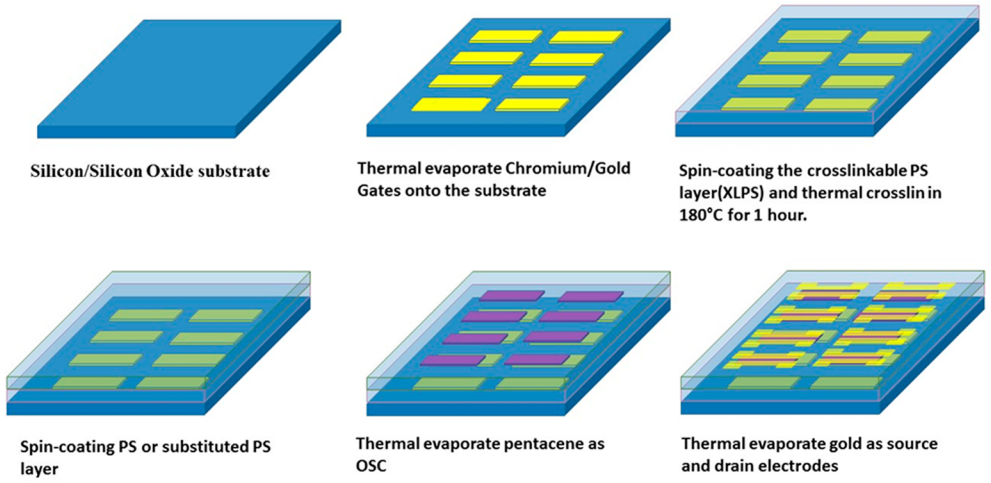
Scheme 1. Synthesis of *N,N*-Bis(4-methoxyphenyl)-4-(4-hydroxyphenyl)aniline (7)



Scheme 2. Synthesis of PS-Based Polymer Dielectric with Cross-Linkable and Chargeable Subunits



Scheme 3. Fabrication Protocol for Pentacene-Based OFETs with PS-Based Polymers as Sole Gate Dielectric Materials[a]



[a]There are eight OFET devices per 1 in. square Si/SiO_2 substrate.

reaction mixture was cooled to room temperature and filtered over Celite. Toluene was removed *in vacuo*. To the resultant slurry, 50 mL of DI water was added, and the product was extracted into ethyl acetate. The product was purified using column chromatography using hexanes/ethyl acetate to obtain the product as a pale yellow oil (0.47 g, 0.9 mmol, 46%).

Synthesis of Triarylamine ***7***. In an oven-dried round-bottom flask, **6** (0.47 g, 0.9 mmol) was dissolved in 20 mL of freshly degassed, dry THF. To this solution, a 1.0 M solution of tetrabutylammonium fluoride (1.35 mL, 1.35 mmol) was added, and the reaction was performed at room temperature under nitrogen for 10 h. After completion of reaction, the solvent was removed *in vacuo* to obtain the pure product as an off-white solid (0.35 g, 0.9 mmol, 99%).

Synthesis of XLPS ***8****, PS-10% Cl* ***9****, and XL-PS-10% Cl* ***10***. The cross-linkable polymer (XLPS) and the precursor polymers (PS-10% Cl and XLPS-10% Cl) were synthesized using the protocols described in our previously published work.[9]

Synthesis of PS-10% TPAOMe ***11*** *and XLPS-10% TPAOMe* ***12***. 0.3 g of 10% XLPS or XLPS-10% Cl was dissolved into 10 mL of dehydrated THF, and then 4-hydroxyphenyl-TPAOMe (198.6 mg, 0.5 mmol), K_2CO_3 (69 mg, 0.5 mmol), KI (41.5 mg, 0.25 mmol), and the cyclic polyether K+ complexing agent 18-crown-6 (13.2 mg, 0.05

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mmol) were added swiftly to avoid excess moisture inside. The reaction mixture was then sealed and heated at reflux under nitrogen at 70 °C for 24 h. After cooling to room temperature, the mixture was poured into water (200 mL) and then filtered. The filtrate was washed with water and methanol three times, and the residue was redissolved in THF and precipitated in methanol (150 mL). The purification procedure was repeated three times, and the final polymer was dried under vacuum overnight, yielding 66% of the desired product polymer.

Device Fabrication and Imaging. *Substrate Preparation and Gate Deposition.* The steps used for making test devices are illustrated in Scheme 3. Silicon wafers with 300 nm silicon oxide (used only for its inertness and flatness) deposited on top were diced into 1 in. squares and then soaked in 3:1 concentrated H_2SO_4:30% H_2O_2 for 30 min (*caution*: *highly corrosive*!) followed by sonicating in water, acetone, and isopropyl alcohol for 15 min each. The substrates were then dried in nitrogen flow, and chromium/gold (5 nm/35 nm) was then thermally evaporated through a mask to give eight gate pads per wafer.

Gate Dielectric Deposition. Multilayers of substituted polystyrene dielectric were spin-coated over the entire substrate under a dry nitrogen atmosphere in a glovebox. All spin-coating solutions were prepared by dissolving the polymers in chloroform, sonicating at 30 °C for 60 min, and filtering into a second vial through a 0.45 μm hydrophobic PTFE syringe filter. The solution was spin-coated with a speed of 1500 rpm (25 Hz) for 60 s, and the film thickness was varied by using different solution concentrations ranging from 20 to 40 mg/mL.[9] To ensure an intact multilayer structure, cross-linking of the XLPS polymer was done in a vacuum oven at 180 °C under 70−80 mmHg for 1.5 h. For all other plain or substituted polystyrenes, the film was annealed in the same vacuum oven at 50 °C under 70−80 mm for 30 min.

Pentacene Semiconductor and Source-Drain Gold Electrode Deposition. The 50 nm pentacene was thermally evaporated via a substrate mask to give eight panels aligned over the chromium/gold gate pads electrodes. Following the deposition of pentacene, gold electrodes were thermally evaporated onto the pentacene through a shadow mask over the gate panels to give 6 mm length and 1.25 mm width source-drain pair channels.

Scanning Electron Microscope (SEM) Cross-Section Imaging. An XLPS/XLPS-TPAOMe/PS trilayer device with spin-coating solution concentrations of 35, 30, and 30 mg/mL and XLPS/PS bilayer devices with spin-coating solution concentrations of 40 and 20 mg/mL fabricated using the procedure described above were fractured using a diamond scribe to expose their cross sections. The cross sections were sputtered with platinum before imaging. Images were obtained using a JEOL 6700F SEM.

Neutron Reflectivity. *Fabrication of Samples for Neutron Reflectivity.* Thermal oxide was completely removed from 38 mm × 38 mm silicon wafers in 6:1 buffered hydrofluoric acid solution. Substrates were then cleaned, and bilayer polymer stacks were fabricated using the procedures described for "gate dielectric deposition" above. The polymer layers were deposited by spin-coating from 10 mg/mL solutions.

Neutron Reflectivity Measurements. Neutron reflectivity measurements were performed on the polarized beam reflectometer (PBR) at the NIST Center for Neutron Research. The beam consisted of 4.75 Å neutrons, as selected with a vertically focusing pyrolytic graphite monochromator. Borated aluminum masks were used to restrict the vertical extent of the beam to a 30 mm tall region in the center of the sample. Specular reflectivity measurements were performed in the range $0.2° < 2\theta < 4.4°$, where 2θ is the scattering angle, which corresponds to a wave vector transfer Q perpendicular to the substrate spanning $0.005\ Å^{-1} < Q < 0.1\ Å^{-1}$. Background measurements were taken in the same range of 2θ with the sample angle offset from the specular condition by 0.3°.

The range of measurement was divided into three configurations of the four vertical slits that define the PBR's beam divergence. For $Q < 0.045\ Å^{-1}$ slits of width 0.5, 0.5, 1, and 1 mm were used; the range $0.035\ Å^{-1} < Q < 0.7\ Å^{-1}$ was measured using slits of 0.7, 0.7, 1.2, and 1.2 mm, and the range $Q > 0.06\ Å^{-1}$ was measured using slits of 1.5, 1.5, 1.5, and 2 mm. For each sample, data from all three configurations were fit simultaneously to the same theoretical model (see below).

RESULTS

In this work, we introduce polystyrenes substituted with the chargeable TPAOMe group, which is a stronger electron donor than the TPA used in our previous published work.[9] 10 mol % TPAOMe was introduced after polymerization through the side-chain reaction with 4-vinylbenzyl chloride precursor. The 10% concentration was found to balance the trade-off between good polymer solubility, leading to smooth spincast films and high enough donor concentration to be electronically influential.

The work presented here includes several procedural improvements. More concentrated polymer solutions were used to spin-coat the dielectric layers, and a mild annealing step was added after spin-coating. The more robust polymer films that resulted allowed higher charging voltages to be applied and showed reduced gate current leakage and lower probabilities of device short circuits compared to the previous published work.[9] Furthermore, the charging process was done using the same system as for $I-V$ testing, reducing the chances of devices being altered or destroyed by multiple probing. The gate-semiconductor current was monitored during charging, verifying the stability of the dielectric barriers during this process.

Cross-sectional images of the PS polymer dielectric and the thicknesses of the layers were obtained by SEM. As shown in Figure 1a for a XLPS/XLPS-TPAOMe/PS trilayer (bottom-to-top layer structures are given as left/right or left/middle/right in text) and in Figure 1b for a XLPS/PS bilayer, distinct dielectric layers were visible due to their differing brightness in the SEM images. Sharp focus was not obtained due to the rough cross section and charging of the dielectric films from the electron beam. These results verified that the deposition of the second or third layer onto the previously deposited and cross-linked layer(s) did not destroy the integrity of the dielectrics.

Figure 2 shows the measured neutron reflectivity for two bilayer films. The films were identically prepared with bottom layers of cross-linkable polystyrene with 10% TPAOMe (XLPS-TPAOMe) and a top layer of perdeuterated polystyrene (d8-PS). The deuteration provided scattering contrast between the two organic layers. The data from the three slit configurations have been rescaled to show continuous reflectivity profiles.

Neutron reflectivity can be used to generate a depth profile of the nuclear composition of thin films.[36] This profile incorporates information about the thickness and chemical composition of each layer as well as the interfacial roughnesses between the layers. Information about the composition is in the form of the scattering length density (SLD) ρ. The interfacial roughnesses are modeled as a series of thin layers with infinitely sharp boundaries whose SLD is interpolated between the two adjacent layers by an error function of the form $\mathrm{erf}\left(\frac{z-z_i}{\sigma_i\sqrt{2}}\right)$, where z_i is the location of the layer boundary determined by the layer thicknesses and σ_i is the layer roughness reported. The SLD profile $\rho(z)$ can then be used to generate a theoretical reflectivity profile which can be compared to the measured profile and refined using nonlinear

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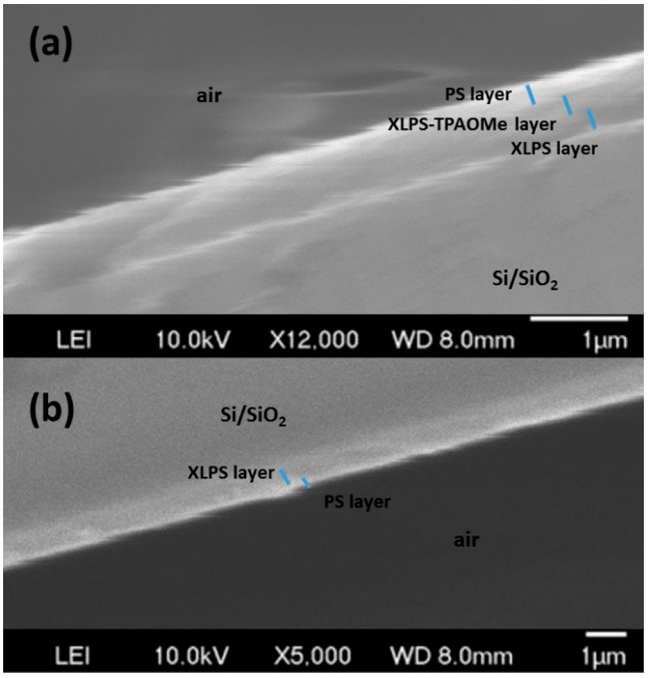

Figure 1. Cross-section SEM images of representative polymer heterostructures. (a) XLPS/XLPS-TPAOMe/PS trilayer device and (b) XLPS/PS bilayer device. Film deposited on the silicon/silicon oxide substrate. For the trilayer, the thickness of each layer top down was 320 ± 12 nm, 300 ± 13 nm, and 300 ± 16.0 nm. For the bilayer, the thickness of each layer top down was 170 ± 8 nm and 300 ± 20 nm. The determination of thickness was based on 10 measurements of each layer with uncertainties expressed as one standard deviation.

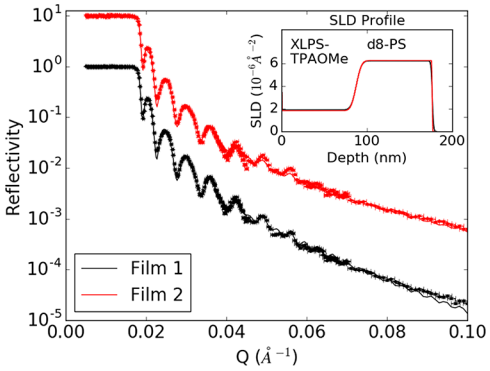

Figure 2. Measured reflectivity for two bilayer films of spin-coated XLPS-TPAOMe/d8-PS. The upper set of data has been offset by a factor of 10 for clarity. The solid lines through the data are best-fit model curves determined from analysis described in the text. This modeling yielded the scattering length density (SLD) profiles shown in the insets with interfacial roughnesses at the XLPS-TPAOMe/d8-PS interface of 4.81 ± 0.02 nm and 4.92 ± 0.03 nm for film 1 and film 2, respectively. The zero of the depth axis is the top of the underlying Si wafer. Error bars on the data and fitting parameters correspond to ±1 standard deviation.

χ^2 minimization. This modeling was performed using the Refl 1D software package.[37] The resulting SLD profiles from this procedure are shown in the inset of Figure 2, and the corresponding reflectivity profiles are plotted with their respective experimental data in Figure 2.

These results show that spin-coated layers formed from cross-linkable polystyrenes modified with the TPAOMe group have thicknesses consistent with those obtained previously for unsubstituted and TPA-substituted cross-linkable polystyrenes.[9] The mean interfacial roughness at the XLPS-TPAOMe/d8-PS interface for the two samples measured was 4.86 ± 0.02 nm. This was 5.5% of the total layer thickness, demonstrating the integrity of the copolymer during the cross-linking process. However, the significant increase in interfacial roughness when compared to the value of ∼2.5 nm found previously for TPA-substituted polystyrenes[9] is consistent with the effects of an increase in free volume and steric hindrance of the TPAOMe functional group compared with the smaller TPA moiety.

The charge trapping properties of the PS-substituted dielectric films were investigated by measuring the threshold voltage shift (ΔV_{th}) before and after charging by observing the transfer characteristics of OFETs. In this paper, we denote a negative sign of ΔV_{th} as representing a more negative V_g required for the OFET to reach the "on" state ("more difficult to turn on"), while a positive sign of ΔV_{th} represents a less negative voltage required to reach the "on" state ("easier to turn on"). The transfer curves were obtained by measuring drain current with V_g increasing from +10 to −70 V, and the drain-source bias fixed at −70 V. V_{th} was determined as the x-intercept of a linear fit to the square root transfer curve in the V_g range where it is approximately linear.[13] We compared V_{th} before and after charging and calculated ΔV_{th} by subtracting the V_{th} before charging from V_{th} measured immediately after charging. The voltage we used to charge was V_{chg} = +100 or −100 V applied simultaneously to the source and drain electrodes with the gate electrode grounded. This ensured sufficient stored and trapped charges.

I−V measurements on the devices were performed within 4−5 h after fabrication. Charging time for each device was 5 min, and the measurement (transfer and output) required 1−2 min, so the testing time for each device was 11−15 min.

We measured charge trapping and V_{th} shifts in pentacene OFET devices with four different dielectric compositions. The compositions of the dielectrics and the spin-coating concentration of each dielectric layer for each kind of device are presented in Table 1. The transfer curves of the four different devices before and after charging at V_{chg} ± 100 V as well as schematics of each device structure are illustrated in Figure 3. In general, higher spin-coating concentration (30−40 mg/mL, compared to 20 mg/mL used in our previous work) more reliably prevented short circuits or current leakage.

Table 1. Dielectric Layer Structure and Spin-Coating Concentration of the Four Different Device Configurations Shown in Figure 3

dielectric composition (bottom-to-top)	spin-coating concentration (mg/mL)
XLPS/PS	40/20
XLPS/TPAOMe	40/30
XLPS/XLPS-TPAOMe/PS	35/30/30
XLPS-TPAOMe/PS	40/30

Leakage currents varied considerably from device to device, as discussed later, but were typically within an order of magnitude of 0.1 μA for 50 V applied to the gate, for a resistance of 500 MΩ. The specific capacitance for 500 nm thick polystyrene is about 10 nF/cm^2, and the device area is about 0.5 cm^2, so gate capacitance for each device is about 5 nF. Thus, the RC time constant is on the order of seconds. The charging time is 2 orders of magnitude larger. The lowest-

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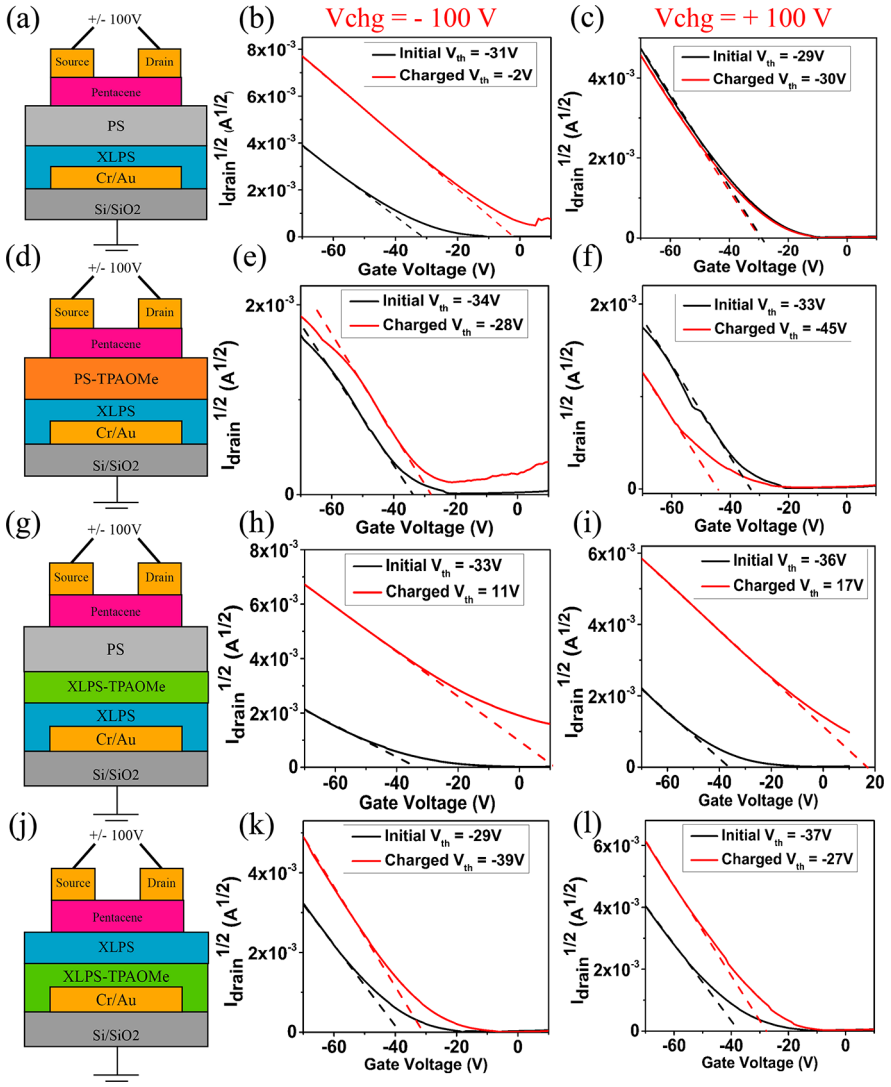

Figure 3. (a, d, g, j) Schematics of the pentacene OFET device architectures studied. (b, e, h, k) Representative transfer curves for corresponding pentacene OFET devices before and after charging at V_{chg} = −100 V. (c, f, i, l) Transfer curves for four different corresponding pentacene OFET devices before and after charging at V_{chg} = +100 V.

leakage-current devices could have *RC* time constants on the same order as the charging time. Recording a transfer curve also takes seconds and involves only transient application of gate voltage equal to the charging voltage. Thus, charging effectiveness should be relatively independent of *RC* time constraints, and there should be minimal discharging during most of the transfer curve recording procedure.

Transfer curves from multiple devices with each dielectric configuration and each charging polarity were obtained before and immediately after charging, and V_{th} shifts were calculated. A compilation of the V_{th} shifts for all the devices measured is shown in Figure 4, together with means and ranges for each sample configuration/charging polarity pair. For the bilayer structure with no substituent (XLPS/PS), steady and large positive V_{th} shifts were observed when applying V_{chg} = −100 V to the source and drain electrodes during charging. When applying V_{chg} = +100 V, inconsistent and negligible V_{th} shifts were observed.

Again referring to Figure 4, V_{th} shifts in the directions that would result from bias stress effects were seen in bilayer structures with a 10% TPAOMe-substituted layer on top of the

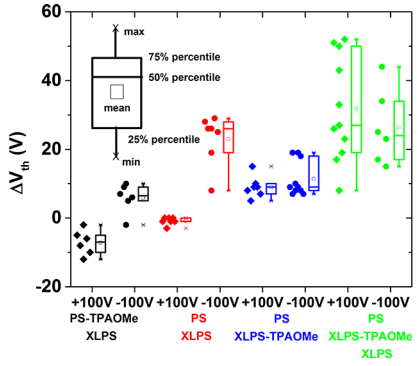

Figure 4. A boxplot of the threshold voltage shifts ΔV_{th} as a result charging with V_{chg} = ±100 V. We denote negative shift as an increase in the magnitude of the V_{th}, indicating devices were harder to turn on and a positive shift as a decrease in the magnitude of the V_{th}. From left to right: V_{th} shift for XLPS/PS-TPAOMe, XLPS/PS, XLPS-TPAOMe/PS, and PS/XLPS-TPAOMe/XLPS.

cross-linked PS layer (XLPS/PS-TPAOMe). We observed a consistent positive V_{th} shift when V_{chg} = −100 V was applied

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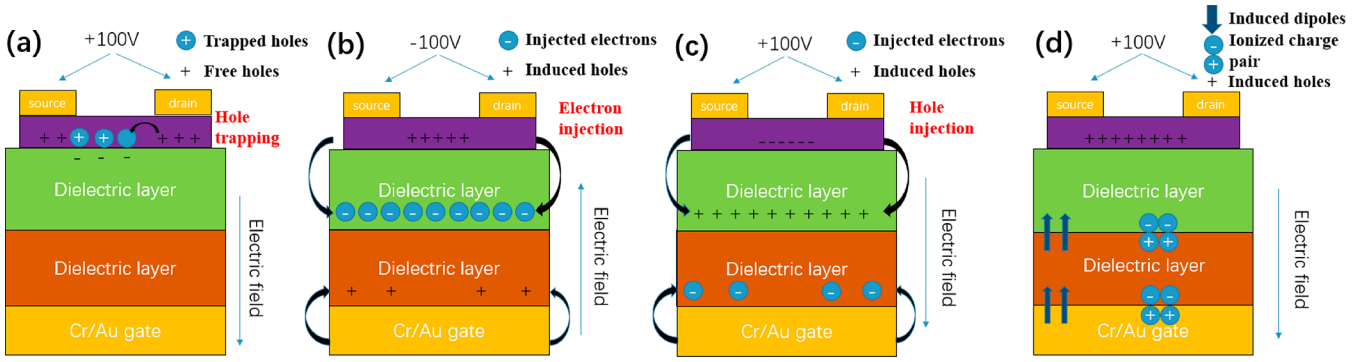

Figure 5. Schematic representations of three charging mechanism: (a) OSC/dielectric bias stress effect, (b) electron injection from the source and drain through the semiconductor, (c) hole injection from the source and drain through the semiconductor, and (d) dielectric polarization or partial ionization within the dielectric or at interfaces.

on top and a consistent negative V_{th} shift when V_{chg} = +100 V was applied. The data indicate that the substituted layer near the OSC/dielectric interface responded to the applied electric field to trap or free charge carriers in the adjacent pentacene layer, which is consistent with the theory of bias stress effects.[26] For the trilayer structure (XLPS/PS-TPAOMe/PS), large negative threshold voltage shifts, which made the devices much easier to turn on, were observed when *both signs of voltages were applied*. The situation was very different from the unsubstituted bilayer structure because V_{chg} = +100 V resulted in large V_{th} shifts in the same direction as that resulting from V_{chg} = −100 V, while there was no obvious V_{th} shift in the unsubstituted bilayer structures in the case of V_{chg} = +100 V. In the charging of the last bilayer structure (XLPS-TPAOMe/PS), somewhat smaller V_{th} shifts were observed when both signs of V_{chg} were applied. The direction of shifts was the same as that of the trilayer structure and again independent of the sign of V_{chg}.

DISCUSSION

In our previous study of the pentacene-based OFETs with PS-based multilayer dielectrics, neutron reflectivity experiments showed that spin-coating cross-linkable, chemically similar, hydrophobic polymer solutions created multilayer dielectric structures with distinct boundaries between the layers.[9] The SEM and neutron reflectivity measurements in this present study show that this approach can be extended to PS-based polymers with the larger TPAOMe functional group on side chains to the PS backbone in any vertical position in the multilayers. Furthermore, the previous study indicated there was no obvious structure change during the charging of substituted PS-based multilayer pentacene OFET devices, again from neutron reflectivity experiments. Therefore, we should also be able to exclude structural change-induced effects in the charging mechanism in this study.

For many of the combinations of layers portrayed in Figure 4, we obtained at least two devices with gate leakage currents 2 orders of magnitude less than the on currents. The V_{th} shifts for these devices were well within the ranges shown in Figure 4 for the sets of devices that included the full leakage current range. We assembled a series of square-root and log transfer curves from pairs of devices with a particular architecture, included in the Supporting Information. One member of each pair (the upper set of curves for each sample) has relatively low off current and/or off-current change after charging, while the other (the lower set of curves for each sample) has relatively high off current magnitude and/or change. For each pair, we see that the V_{th} shifts are comparable and in the ranges depicted in Figure 4. Thus, we have experimental evidence that while the charging process may cause some change in charge injection or breakdown properties of the gate dielectrics, the static charge distribution, responsible for the V_{th} shifts, is not greatly sensitive to this aspect of the charging process.

Furthermore, previous investigators have presented both theoretical and experimental[38−41] findings regarding a device modification leading to changed gate leakage current and the accompanying V_{th} shift. In all these cases, the V_{th} shifts are very small (1−5%) compared to the V_g range being swept. All of our V_{th} shifts (excluding the one that we consider negligible) are at least 10% of the V_g range, and for the three architectures that showed the most substantial V_{th} shifts, the magnitudes of those were much higher than that. A numerical model of the effect of various magnitudes of gate dielectric resistance (leakage current) on the determination of V_{th} is presented in text accompanying Figure S12. Our leakage current levels are well within the range in which our V_{th} shifts would be negligibly affected.

For bilayer structures with substituted chargeable layer (PS-TPAOMe) on top and in direct contact with the semiconductor, V_{th} shifts in the directions that would result from bias stress effects were observed. When positive bias was applied on top (same effect as negative gate voltage applied on the gate), free charge carriers (holes in pentacene) were trapped and became immobile near the interface, reducing the drain current and thus the threshold voltage (Figure 5a). This effect was not observed for the bilayer devices without TPAOMe. When negative bias was applied to the TPAOMe-on-top bilayer, a positive V_{th} shift was observed instead, indicating that immobile charge carriers were released and became free as electrons were injected into the dielectric (Figure 5b).

For all the devices with XLPS or PS on top, electron injection from semiconductor to dielectric was again the dominating effect when V_{chg} = −100 V was applied, resulting in a large positive V_{th} shift (Figure 5b). On the contrary, the large positive V_{th} shift observed in the positive charging case for the trilayer and the XLPS-TPAOMe/PS bilayer devices indicated a different mechanism of device polarization. A possible explanation was that the TPAOMe layer was polarized to form dipoles responding to the applied electric field or even became partially ionized (Figure 5c). The accumulating negative ends of the dipoles or ions presented at the top parts of the interface could have induced free holes in the

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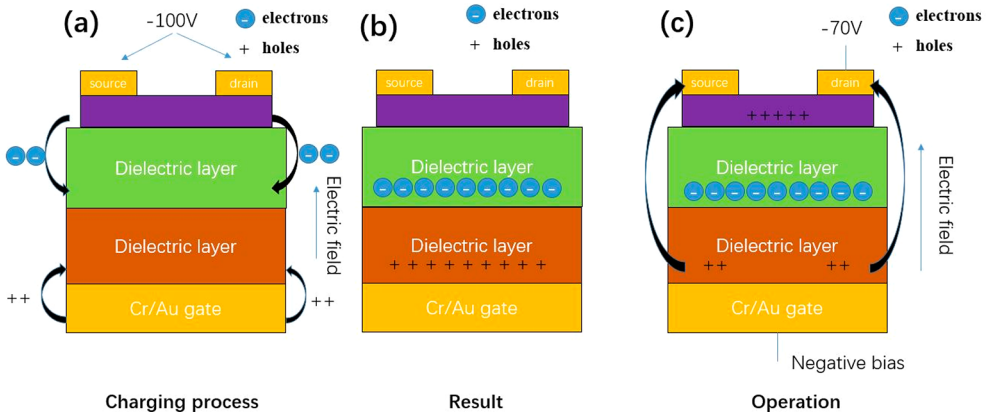

Figure 6. Schematic diagrams representing three stages of static charge storage: (a) charges are injected from each conductive interface some depth into the dielectric, (b) arrangement of injected static charges after application of charging voltage is terminated, and (c) distribution of charges after the circuit is connected for operating the transistor.

pentacene. Charging effects in the trilayer were generally larger than for the XLPS-TPAOMe/PS bilayer devices. A possible reason was that in the trilayer case the bottom cross-linked layer and the top PS both served to stabilize the stored charges by blocking their dissipation into either the pentacene OSC or the gold gate electrode. This mechanism would also be consistent with charges stored in the bulk, rather than at the outer interfaces, of the trilayer. This observation of larger average V_{th} shifts from the trilayers supports the hypothesis that the TPAOMe groups do play a role in hosting and stabilizing the static charges and help define the distances between average planes of mutually compensating holes and electrons in the dielectrics. While we hypothesize that ionized TPAOMe groups are sites of stored positive charge, the structural irregularity and free volume associated with this group could also lead to increased sites where charge could be trapped.

As an order-of-magnitude estimate of a reasonable quantity of charge injection, let us assume that a maximum of one hole or electron is injected into each column of dielectric, perpendicular to the film planes, with an area equivalent to the TPAOMe subunit plus the stoichiometric number of nonfunctionalized styrenes. Initially, Coulombic repulsion would enforce this restriction, but as some charges penetrate into the dielectric, it is understood that multiples of them may be injected in the same vertical column. Still, there may be a limit to how deeply into the dielectric the charges could be injected by application of 100 V, and it is possible that certain planes within the dielectric, such as near layer interfaces, may be particularly stable locations for static charge. It should also be understood that while TPAOMe is designed as a hole trap, either holes or electrons could be additionally stabilized by nearby polarization of the TPAOMe group. Finally, while strictly speaking it would be necessary to solve Possion's equation for an assumed charge distribution to calculate voltages at different positions within the dielectric, the effects on the OFET characteristics would be the same if average planes of charge are invoked, effectively forming the plates of a capacitor.

To connect the degree of charging of the TPAOMe groups to the shift in V_{th}, we assume one TPAOMe group is present for every 14 styrene subunits consisting of a phenyl ring and two other non-hydrogen atoms. Each styrene subunit would be 0.3 nm^2 in area if it were flat. Using this area (reasonable if we assume that the tilt of the subunits and the free volume around them roughly cancel) yields an estimate one TPAOMe per 4 nm^2 of area and an effective areal density $n_a = 2.5 \times 10^{13}$ TPAOMe per cm^2. Within the effective capacitor model described above, the corresponding areal charge density σ on the TPAOMe can be written as

$$\sigma = n_a f e = \varepsilon \varepsilon_0 V / d$$

where f is the fraction of TPAOMe groups that are charged, V is the voltage drop between the two planes of charge, and d is the separation between them. With $\varepsilon = 2.7$ for polystyrene, this yields d (nm) = $0.6V/f$. Thus, for a 10 V V_{th} shift and a charge separation d = 300 nm, which is the thickness of one layer in a trilayer as shown in Figure 1, the fraction of TPAOMe units that hold a unit charge would be 2%. Figure 7 shows the range of the charged fraction f accessible vs effective charged layer spacing for various values of V, corresponding to the V_{th} shifts in Figure 4.

While it is not possible to determine the specific charge densities and spacings for these cases, the plausible combinations of values as shown in the plot are accessible considering the compositions and hypothesized dimensions of the TPAOMe-containing films and can accommodate the

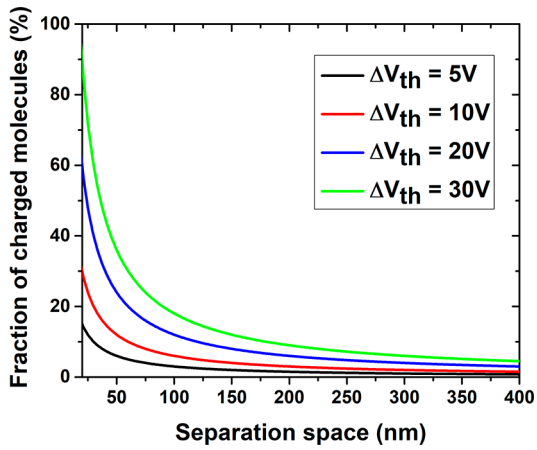

Figure 7. Possible relationships between fraction of charged TPAOMe subunits in an average plane of the subunits, possible distances between the planes, and observed V_{th} shifts.

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interfacial and the charge-separated schemes shown in Figure 5.

An interesting trend is displayed by all of the V_{chg} = +100 V data taken together. V_{th} shifts progress from more negative to more positive with TPAOMe on top, absent, on the bottom, and in the middle. This trend is consistent with TPAOMe imposing additional negative V_{th} by trapping positive charge. This makes the device more difficult to turn on when at the pentacene interface but easier to turn on when remote from it, while the effect is largest with the TPAOMe flanked by unsubstituted PS barriers. The "more negative" V_{th} effect of TPAOMe is also observed for the TPAOMe on top relative to the unsubstituted PS on top with V_{chg} = −100 V charging, but the increased charge density in pentacene induced by negative charging appears to saturate and is not significantly higher with TPAOMe added in layers remote from the pentacene.

CONCLUSION

We synthesized a series of cross-linkable and chargeable PS-based dielectric polymers with 10% benzocyclobutene and 10% TPAOMe function groups. Using these polymers as the sole gate dielectric, we constructed three different types of multilayer stack dielectrics for pentacene- based OFET devices, with the TPAOMe-substituted chargeable layer either in contact with the pentacene, in contact with the gate, or sandwiched between PS layers without TPAOMe. Thermal cross-linking the benzocyclobutene subunits ensured successful successive deposition of the polymer layers via spin coating. We compared the V_{th} shift before and after charging the devices to V_{chg} = ±100 V and propose three charging mechanisms to account for the variety of behaviors observed, using heterostructures without TPAOMe groups for comparison. V_{th} shifted in the direction corresponding to the sign of the charging bias in the bilayer device with TPAOMe layer in contact with the pentacene, the same direction as is generally associated with bias stress. Electron injection from pentacene to dielectric was found from negative charging of devices with no chargeable subunit layer in contact with the pentacene. Formation of polarized dipoles or partial ionization occurred in the bilayer devices with chargeable subunits remote from the pentacene when V_{chg} = +100 V was applied, contrary to bias stress effects. The location of the chargeable subunits in different locations in these heterostructures allows the selection between two different dielectric charging mechanisms and thus new means of controlling charge density in semiconductors. This charge density control is relevant to OFETs and other semiconductor-containing devices, such as thermoelectrics and topological insulators.[42,43]

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.macromol.8b00596.

Spectra for synthesized compounds and polymers; plots of representative high- and low-leakage current devices; numerical leakage current model (PDF)

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Notes

The authors declare no competing financial interest.

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