SCIENTIFIC REPORTS

OPEN

Long-term drift of Si-MOS quantum dots with intentional donor implants

Received: 25 May 2018
Accepted: 27 April 2019
Published online: 21 May 2019

M. Rudolph[1], B. Sarabi[2], R. Murray[2], M. S. Carroll[1] & Neil M. Zimmerman[2]

Charge noise can be detrimental to the operation of quantum dot (QD) based semiconductor qubits. We study the low-frequency charge noise by charge offset drift measurements for Si-MOS devices with intentionally implanted donors near the QDs. We show that the MOS system exhibits non-equilibrium drift characteristics, in the form of transients and discrete jumps, that are not dependent on the properties of the donor implants. The equilibrium charge noise indicates a 1/*f* noise dependence, and a noise strength as low as $1\ \mu eV/\sqrt{Hz}$, comparable to that reported in more model GaAs and Si/SiGe systems (which have also not been implanted). We demonstrate that implanted qubits, therefore, can be fabricated without detrimental effects on long-term drift or 1/*f* noise for devices with less than 50 implanted donors near the qubit.

For semiconductor quantum dot (QD) based qubits, charge noise has been identified as a critical parameter influencing the fidelity of the qubit[1]. Measurements indicate that the noise is 1/*f*-like, which results in a quasi-static dephasing signature, where the low-frequency noise components (with respect to the qubit operations) dominate the dephasing[2,3]. We explore the impact of implanting donors near the active QD regime of Si-SiO_2 devices on the strength of the low frequency charge noise. In particular, we measure the charge offset drift Q_0, which has its biggest impact on the possible integration of devices[4]. Previous studies have shown an order of magnitude reduction in Q_0 for a Si-SiO_2 MOS system compared to dielectric stacks that include AlO_x (present with Al top gates)[4,5]. However, the influence of donors in QD systems has not been studied. The process of donor implants is necessary for donor-based qubits, which have recently demonstrated extremely long coherence times[6]. The QD qubit motivating this work is a QD-donor double well system operated in a two-electron singlet triplet scheme[7–9]. This hybrid system has the potential to provide very long coherence times, as have been shown in single donor qubits. In addition, searching for the elusive donor-donor coupling[10] is bypassed by the tunability of the QD-donor coupling. Due to the statistical straggle of donor implantation, the exact location of a donor can be estimated to within only tens of nanometers, so more donors than are necessary are implanted to ensure that a donor is placed in a target zone[11,12]. We study the effects of various quantities of implanted donors on the low frequency charge noise and show that, for certain devices, the process of implanting donors does not affect the charge noise.

Long-term drift was measured for six devices. The silicon source material and devices were all fabricated at Sandia National Labs, with minimal differences in the process flow[13]. Two of the devices have isotopically enriched ^{28}Si substrates, while the other four are naturally abundant silicon. The material stack consists of the Si substrate, a 35 nm SiO_2 gate oxide, and a 200 nm poly-Si gate. The poly-Si layer is patterned with one of the geometries shown in Fig. 1(a), where each device is capable of forming two QDs, one in the lower half of the device and one in the upper half. The QDs are formed by either a gated wire (GW) or a split-wire accumulation gate (SWAG), with two geometries mirroring the design (MGW, MSWAG) and one geometry mixing the designs (GW-SWAG). Simulations of the electron density for actual operating voltages are shown in Fig. 1(b) to highlight the differences in QD sizes and proximity to the implanted donors. Next, some devices received donor implants confined near the QD regions by a pattern mask (yellow boxes). Both 120 keV Sb and 45 keV P ions were studied; both species have similar target depths of 28 nm, but the Sb implants have a narrower straggle (18 nm compared to 25 nm). The total number of donors implanted differs between the devices due to a difference in both the implant fluence and the implant window size. In addition, the location of the implant differs between devices, with some devices having the implants around the QD being studied, while other devices have implants on the other half of the device around the inactive QD. Table 1 provides the parameters for each of the devices studied. For the number

[1]Sandia National Laboratories, Albuquerque, NM, 87185, USA. [2]National Institute of Standards and Technology, Gaithersburg, MD, 20899, USA.Correspondence and requests for materials should be addressed to N.M.Z. (email: neil.zimmerman@nist.gov)

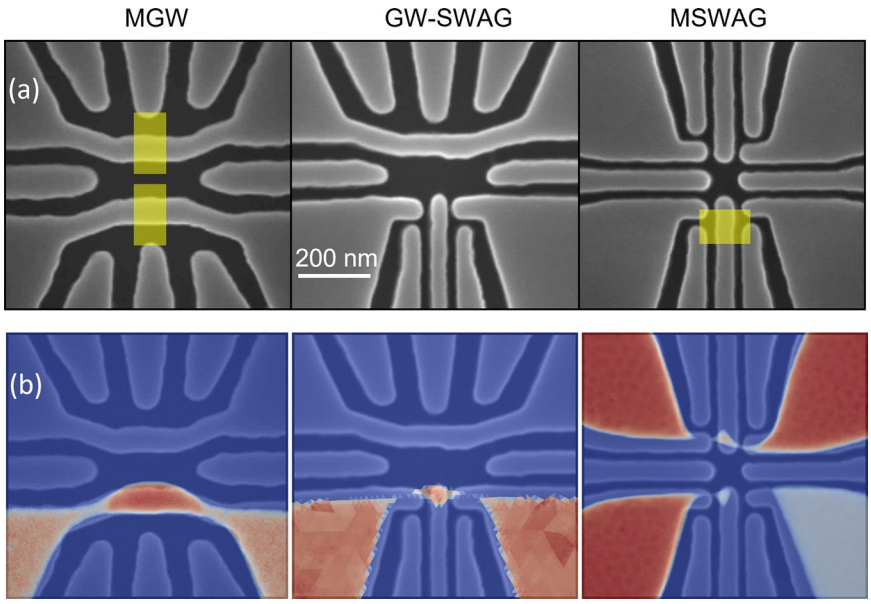

Figure 1. (**a**) Scanning electron micrographs of the three device designs measured. The light gray are the poly-Si gates, and the yellow regions are where donors are implanted. (**b**) Simulated electron density (red regions) for each of the devices using operational voltages. The lower half of the device is turned on for MGW and GW-SWAG, while for MSWAG both the lower QD and upper charge sensor are on.

Device	DA	DB	DC[a]	DD[a]	DE	DF
Geometry	GWSWAG	GWSWAG	MSWAG	MGW	MGW	MGW
Implant donor	—	—	P	P	Sb	Sb
Implant energy (keV)	—	—	45	45	120	120
Implant Fluence (10^{11} cm^{-2})	—	—	4	8	4	4
Anneal (°C)	—	—	1000	900	900	900
Number of donors	0	0	27 (13)	60 (60)	45 (0)	0 (45)
Substrate Resistivity (Ωcm)	$>10^4$	$>10^4$	$>10^{4\,b}$	$>10^{4\,b}$	$>10^4$	$>10^4$
$T(K)$	4.1[c]	4.1[c]	0.2[c]	0.2[c]	2.3[d]	2.3[d]
σ_0 (μeV)	40 ± 15	70	4	—	9 ± 3	12 ± 4
$e\sigma_0/E_C$ ($10^{-3}e$)	15	15	0.5	—	9	12
τ_{tr}(hr)	6	11, 3.3	—	—	17	>30
β	2.65 ± 0.24	1.29 ± 0.12	1.07 ± 0.13	—	0.85 ± 0.015	0.89 ± 0.18
σ_β (μeV) at 1 Hz	—	7 ± 3	1 ± 0.6	—	7 ± 4	5 ± 3

Table 1. Compilation of device parameters. The number of implanted donors is separated into donors near the measured SET and, in parentheses, donors on the opposite device of the SET. Measurements performed at the indicated temperature exhibited a standard deviation in the chemical potential drift and charge offset drift of σ_0 and $e\sigma_0/E_C$, respectively. For devices where the lever arm was not measured, bounds for σ_0 are estimated from values of the charging energy measured for other devices with identical geometries. For instances where a transient drift can be fit to an exponential, the decay parameter τ_{tr} is reported. The exponent of the spectral density β and the noise strength σ_β at 1Hz are provided. [a] ^{28}Si device. [b]Resistivity of natural silicon substrate. The resistivity of the ^{28}Si epi-layer is not measured. [c]Measured at Sandia National Labs. [d]Measured at NIST.

of implanted donors, we distinguish between the number of donors implanted near the active QD from donors implanted near the inactive QD (in parentheses). All implanted devices received an activation anneal, while all devices received an identical post-fabrication forming gas anneal.

To measure the long-term drift characteristics of our devices, a QD is tuned up in the lower half of the device. For Devices DC and DD, the upper QD is also present, but the drift is only measured on the lower QD. The simulated electron densities of the devices during operation are displayed in Fig. 1(b). The relative position of the QD chemical potential at fixed charge occupation is measured either through the transport Coulomb blockade signature in the lower QD, or it is measured by the charge-sensed response of the upper QD. The functional form of the transport measurement depends on the ratio E_C/k_BT. For values less than 5, the Coulomb blockade is not robust, and the data is approximated by a sine function[4], where

$$I(V, t) = I_0 + I_1 V + A \sin[2\pi(C/e)(V + \Delta V(t))]. \quad (1)$$

here, V is the gate voltage applied, and C is the capacitance of the gate to the QD. In this region, the conductance has contributions from the quantum Coulomb blockade effect and the classical transistor turn on, the latter of which is approximated by a linear voltage response to the small voltage swings applied. The chemical potential position is assigned to the phase $\Delta V(t)$ of the sine fit. For values of $E_C/k_BT \gtrsim 5$, where E_C is the QD charging energy, the Coulomb blockade is robust and the conductance goes to zero. The data is fit to[14]

$$I(V, t) = A \cosh^{-2}[B(V + \Delta V(t))]. \quad (2)$$

The chemical potential is defined by the peak center. For the charge sensing measurement, the chemical potential is extracted by a fit to the center of a Fermi-Dirac distribution[15]

$$I(V, t) = I_0 + I_1 V + \frac{A}{1 + \exp[B(V + \Delta V(t))]}. \quad (3)$$

A linear background approximating the direct charge sensor response to the gate is included. Examples of all three types of data are presented in Fig. 2(a). The measurement is repeated approximately every 10 minutes for multiple days to track changes in the position of the QD chemical potential. The traces in Fig. 2(a) are offset for clarity with each scan separated by a day, with later scans on the top.

The extracted voltage shifts $\Delta V(t)$ are device and geometry specific, and are converted to charge offset drift. For many-electron QDs, the regular period of the Coulomb blockade peaks indicates the voltage required to change the QD occupation by one electron, and so the QD chemical potential position can be expressed in units of charge, where $\Delta Q_0(t) = e\Delta V_N(t)/(V_{N+1} - V_N)$, with N the QD occupation[4]. Figure 2(b–g) show the long-term charge offset drift for each of the devices. Measurements performed via direct electronic transport and remote charge sensing have qualitatively similar behavior. It is also useful to convert the charge offset drift to a chemical potential drift, which is important for relating the noise to qubit performance. If the gate lever arm α is known, the chemical potential drift is simply $\Delta\mu_0(t) = -\alpha\Delta V_N(t)$, where α has units of eV/V. The two can be related by $\Delta\mu_0 = -(E_C/e)\Delta Q_0$. For instances where α is accurately known, the chemical potential drift is indicated on the right axes (note negative sign). Please see the Supplemental Information for a discussion of energy vs. charge units.

The characteristics of the drift observed (Fig. 2) in the devices can be separated into three categories.

1. A transient relaxation. This can occur after a thermal shock such as a cooldown. Measurements were performed within a few hours of cooldown for devices DA, DE, and DF, and the chemical potential position initially follows a quasi-exponential relaxation until the saturation after about 2 days. Regions of thermally induced transients are indicated by (■). Transient relaxation also occurs after a non-equilibrium charge reconfiguration due to an external voltage shock. This is evident in device DB where the spikes observed at hours 24, 48, and 72 were induced by work being performed near the cryostat. Device DE has two shock events as well. The relaxation here is also on the order of a day. Electrostatically induced transients are indicated by (□).
2. Isolated discrete jumps. Reconfiguration of isolated charges in the device can induce a chemical potential shift with no subsequent relaxation. Two such events are visible in device DB at hours 75 and 110. Devices DC, DE, and DR also display this behavior, which are indicated by (★).
3. Local fluctuations about a stable mean value are present in all measurements and originate from the charge noise induced by remote charge reconfigurations and gate noise. Examples of these are highlighted in the figure. The size and spectrum of these local fluctuations measure the intrinsic equilibrium charge noise of the system. For device DA, there exists a dominant slow two-level-fluctuator, while the equilibrium fluctuations for the other devices are on faster time scales.

Device DD shows significantly different behavior than the others, with a slow, non-monotonic drift dominating the charge offset measurement. This device will be excluded in the following discussion and revisited at the end.

Before discussing these results in detail, we wish to put the charge offset drift in the context of previous measurements. As discussed above, the charge offset drift is an important feature for the prospect of integration of single electron devices in general, and has been measured in a variety of devices[4,16]. In particular, the general observation has been that phenomena such as the transient relaxation and slow, non-monotonic drift have not been observed in all-Si devices fabricated from silicon on insulator (SOI) substrates, which have demonstrated background levels of drift of $e\sigma_0/E_c \lesssim 0.03$e. Here σ_0 is the standard deviation of $\Delta\mu_0(t)$. We note that infrequent discrete shifts have been observed. Si devices with aluminum gates have shown non-monotonic drift[5], with $e\sigma_0/E_c \approx 0.15$ e; while devices based on Al/AlO_x/Al tunnel junctions have large instabilities with non-monotonic drift, transient relaxation, and frequent discrete shifts, with overall fluctuations $e\sigma_0/E_c > 1$ e. These observations have been interpreted as suggesting that the general behavior and magnitude of the charge offset drift depends on the quality of the insulators surrounding the quantum dot.

However, our observations in all-Si devices with bulk Si substrates, as shown in Fig. 2, of transient relaxation and (in one case) slow, non-monotonic behavior, show different behavior than those previous results in all-Si SOI-based devices. Both all-Si architectures exhibit infrequent discrete shifts, which are often correlated with external impulses on the measurement apparatus[17]. It is apparent from this difference that the previous general

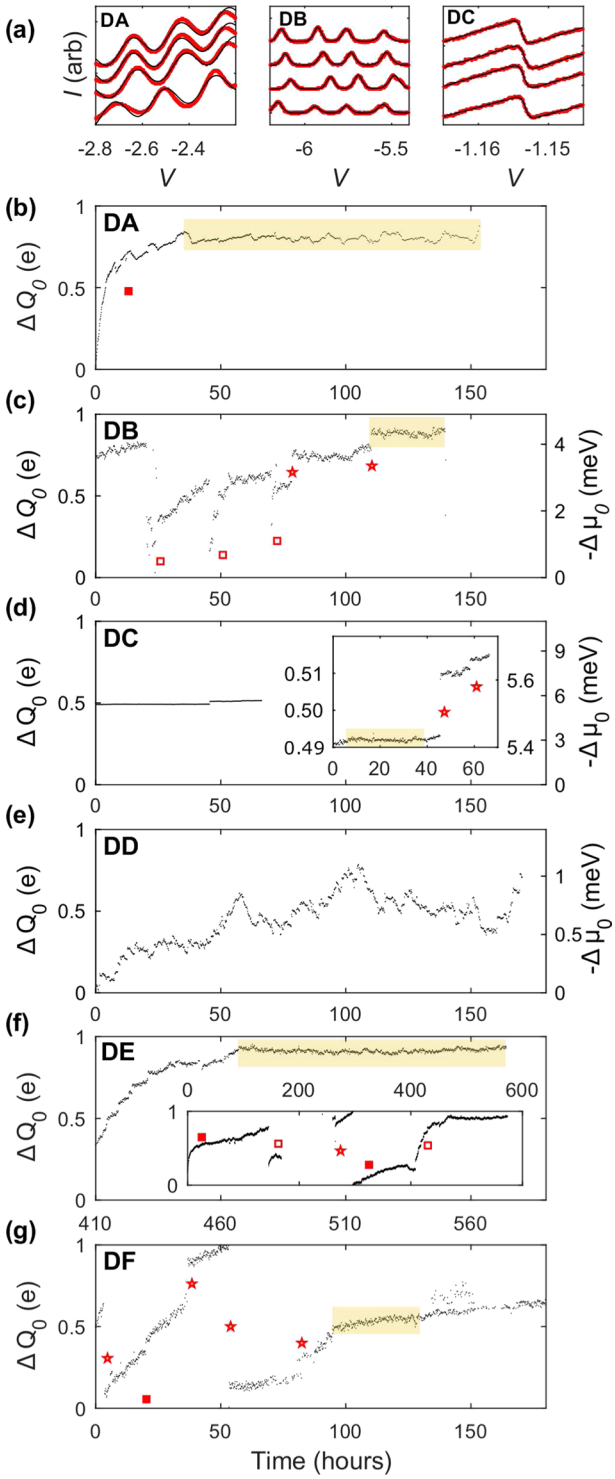

Figure 2. (**a**) Example fits to the chemical potential position for electron transport measurements (left, Eq. 1; middle, Eq. 2), and for charge-sensed measurements (right, Eq. 3). Traces are taken a day apart, and horizontal shifts represent $\Delta V(t)$. (**b–g**) Charge offset drift for devices DA-DF. Occurrences of transient relaxation due to thermal shock (■) and external shocks to the measurement apparatus (□) as well as discrete charge redistributions (★) are annotated. Regions where local fluctuations of charges dominate are highlighted yellow, and are where σ_0 is measured.

conclusion that the charge offset drift depends only on the materials quality of the nearby insulators is insufficient, and that the device architecture may also play a role. We now proceed to discuss the transient relaxation, discrete shifts, and local fluctuations in our devices. The results are summarized in Table 1.

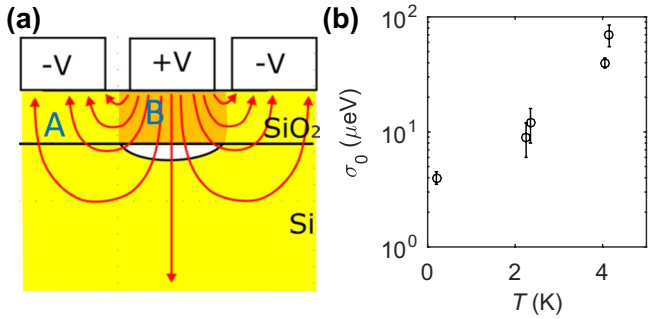

Figure 3. (**a**) Qualitative electric field profile near the QD. In region A (yellow) the electric fields point away from the QD, which in region B (orange) the electric fields point toward the QD. (**b**) The standard deviation of the local chemical potential fluctuations as a function of electron temperature.

Transient Relaxation

For the transient relaxation present, the direction of the relaxation is the same in all devices. The transient decay time τ_{tr} for the relaxation, computed by an exponential fit $e^{-t/\tau_{tr}}$, is found to be between 3 and 17 hours for the 3 instances. Both devices DE and DF have an instance of a longer relaxation of >30 hours, but do not reliably fit an exponential form. All devices were measured in different cryostats and have different donor implant parameters, suggesting an intrinsic origin of the transient behavior. Notably, devices DA and DB had no donor implants, while device DE was implanted, indicating that the addition of donors near the QD does not affect the transient behavior. In all cases, the relaxation lowers the chemical potential of the QD. This can occur when negative (positive) charges migrate away from (toward) the QD, requiring the electric field point towards the QD (region B in Fig. 3(a)). In our lithographic devices, the confining lateral electric fields point away from the QD at the interface (region A in Fig. 3(a)), ruling out the reorientation of slow interface traps. We offer two hypotheses for the transient relaxation.

- In the SiO_2, the fields closest to the QD point towards it while farther away they can point away from the QD (Fig. 3(a)). The capacitive effect of charge motion would be dominated by the closer regions, consistent with lowering the chemical potential, and indicating that the charge motion inducing the transient relaxation can occur in the SiO_2 (region B). Because presence of the donors in the Si does not significantly affect the relaxation, this would suggest that any damage induced in the SiO_2 from the implant process (an anneal step is performed to minimize damage) does not affect the relaxation.
- When the device is first turned on, a depletion region must be formed in the substrate before electrons can accumulate at the interface. With our low-doped substrate, the depletion region is about 1μm at equilibrium. In order to grow the depletion region, electrons must be injected into the substrate to neutralize the acceptor atoms. At low temperatures, the substrate is frozen out (insulating), so it is possible that the rate at which the depletion region can respond to large voltage swings is limited due to electrons tunneling through the substrate from the implanted ohmic regions[18,19]. This mechanism would induce transients lowering the chemical potential for sudden positive voltage changes, which is consistent with normal operations during device turn on after cooling down. This is independent of any deliberate donor implantation performed, and would exist in all devices. The magnitude of the effect may be dependent on the amount of area enclosed by positive voltages (size of QD and reservoir gates). In addition, SOI-based devices may suppress this effect as the depletion region is significantly reduced compared to bulk-Si based devices, so there are fewer background dopants to equilibrate.

Discrete Shifts

The large discrete shifts observed in the QD chemical potential (device DB at hours 75 and 110, device DC at hours 45 and 58, device DE at hour 280, device DF at hours 8, 40, 52, and 80) are also all a lowering of the QD chemical potential. Note that discrete shifts are observed in both implanted and non-implanted devices. If an electron tunnels between two isolated interface trap sites, the observed shifts would be caused by an electron tunneling away from the QD. However, the electric field would detune two trap sites such that there would be a larger probability of electrons tunneling toward the QD (assuming a random distribution of trap levels in both space and energy), contrary to our observations. The discrete jumps in our devices are more likely to be caused by isolated interface electrons tunneling to the leads either directly or via cotunneling through the QD, leaving behind an ionized hole trap in the SiO_2. Note that the maximum magnitude of these events in about 0.5e which is due to the screening effect from the reservoirs. One would expect these discrete transitions to saturate, similar to the transient behavior, after some time scale. However, the individual jumps present are separated by >10 hours, and there are not enough discrete transitions to gather statistics and define a time scale for saturation. The magnitude of the discrete shifts does seem to decrease over time, indicating that the closer traps (regions of higher fields) satisfy more quickly. As with the transient behavior, the discrete features are observed in both implanted and non-implanted devices, suggesting a mechanism intrinsic to the MOS system and not the implant parameters.

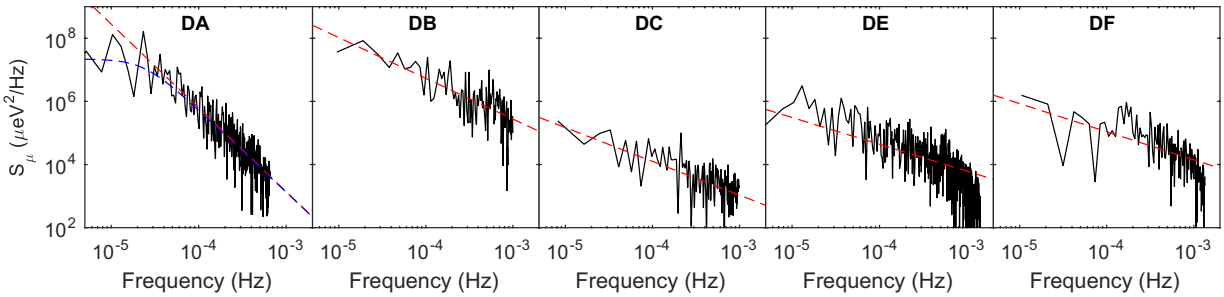

Figure 4. Power spectral density of the chemical potential drift for all devices, excluding DD. The dotted lines are power law fits, which are tabulated in Table 1.

Local Fluctuations

In between the transient and discrete shifts in the chemical potential, the chemical potential drift is stable about a mean value. The fluctuations about this mean are presumably caused by metastable charge fluctuations in the device. We compute both the standard deviation σ_0 and the spectral density of these local fluctuations. The data used in these calculations are indicated by the high-lighted regions of Fig. 2(b–g). Since there may still be some slow transient behavior in these regions, a quadratic background is removed before the analysis. The spectral density is computed by the Fourier transform of the fluctuations, which are shown in Fig. 4. Power law fits of the form $S_\mu = \sigma_\beta^2(1\text{ Hz})^{\beta-1}/f^\beta$ are applied to each spectrum (extracted parameters are in Table 1) and reveal that all devices (both implanted and non-implanted) except DA exhibit a $1/f$ noise dependence (device DB has β slightly higher than 1, which may be due to a quadratic background not being sufficient to describe the residual slow drift). In MOS systems, one typically observes $1/f$ noise, whose origin can be attributed to an ensemble of a random distribution of two-level fluctuators[20]. Since fluctuators are temperature dependent[21], this model would predict an increase in the noise strength as temperature increases, which has been observed in GaAs and Si-based QD systems[2,22]. In Fig. 3(b), the variance of the chemical potential drift σ_0 for each device is plotted against their electron temperatures. While direct comparison of the noise strength between different devices introduces unknown errors due to differences in specific disorder configurations in each device, a monotonic increase in noise is observed over the sample set of five devices. The standard deviation in the charge offset drift $e\sigma_0/E_C$ and the spectral noise strength σ_β also exhibit a monotonic increase with temperature. We note that shot noise, Johnson noise, and instrument noise for these measurements are estimated to combine for, at most, a contribution of 0.04 μeV^2/Hz, which is well below the levels measured.

To improve the performance of a QD qubit system, it is important to minimize the charge noise. The charge noise measured in QD qubit systems is often of $1/f$ nature, and the best reported values of the noise strength σ_1 (where $\sigma_1 = \sigma_\beta$ for $\beta = 1$) have been in the range of 1–10 μeV at 1 Hz at temperatures of ~0.1 K for unimplanted GaAs, Si/SiGe, and Si-MOS devices[2,3,22]. At similar temperatures, we measure for device DC $\sigma_1 = 1\ \mu$eV, which lines up very well with this strength. The process of intentionally introducing donors near the QD does not significantly degrade the charge noise characteristics, and in fact the noise strength is similar to non-implanted MOS devices as well as nominally cleaner SiGe and GaAs devices[2,3].

For device DA, the increased low frequency noise is due to a dominant two-level-fluctuator present. Since the QDs are zero-dimensional objects and only sample a relatively small spatial distribution of fluctuators, one can expect that there is a reasonable chance for a dominant fluctuator to exist that will skew the random distribution of fluctuators that produces the $1/f$ noise. The noise spectrum of a symmetric two-level fluctuator is $S_{sTLF} \propto [f_c^2 + (2\pi f)^2]^{-1}$, where f_c defines the corner frequency separating a low frequency f^0 dependence and a high frequency f^{-2} dependence and characterizes the fluctuator time-scale[23]. The power-law fit to the spectrum for device DA omits frequencies less than 2×10^{-5} Hz (equivalent to time-scales of $1/f_c = 13$ hrs which is consistent with Fig. 2(b)) to characterize the noise roll-off. We find $\beta = 2.65$, which is greater than the expected value of 2. This may be an artifact of the FFT as the time domain data indicates that the nature of the fluctuator is changing over the course of the measurement (fluctuator size is increasing with time). The spectral density at 10^{-3} Hz for device DA is approaching that of devices DC, DE, and DF, so one may expect a return to $1/f$ behavior for slightly higher frequencies than explored here.

The drift characteristics of device DD does not fit the same characteristics as the rest of the devices. It exhibits a much larger amplitude of drift, and the drift is not monotonic as in the case of the transient decay. Nominally, device DD is similar to device DC in materials and the measurement temperature, with the differences being the device design and the quantity of donor implants. We rule out the influence of the differing device design, as the noise characteristics in device DE (same design and similar processing as device DD) are consistent with device DC. The other differing aspect is that device DD received a donor implant density twice that of the other devices, which, coupled with a larger implant window, resulted in more than 3 times the donors being implanted. While the other devices suggested that the implant process does not significantly effect the noise characteristics, there may be a threshold in the implant density or quantity for which the noise does become detrimentally effected. It is also possible that the measurement system for this device introduced extra noise.

In summary, we have measured the low-frequency charge offset drift characteristics of intentionally implanted Si-MOS QD devices. The devices have various lithographic designs and implant parameters. In addition to equilibrium noise features, non-equilibrium features in the form of transient relaxation on the time scale of a few days

and also discrete charge reconfigurations are present. However, these non-equilibrium features are not dependent on the donor implants. We note that the non-equilibrium features were not observed in previously measured SOI based Si-MOS QD devices. The noise spectra indicate $1/f$ noise in the low-frequency range, as expected in Si-MOS devices, and devices with implanted donors exhibit noise magnitudes similar to best reported values in unimplanted Si-MOS, SiGe, and GaAs. While there may be a detrimental effect on noise for high implant densities, modest implant densities provide a low-noise QD system for which a coupled QD-donor qubit can be accessed.

Methods

Device fabrication. Phase 1 (silicon foundry): The initial material stack is fabricated using a 0.35μm silicon foundry process at Sandia National Laboratories. The starting material is a 150 mm diameter float zone $\langle 100 \rangle$ n-type silicon wafer with a room temperature resistivity of $>10\,\text{k}\Omega\text{cm}$. The two enriched silicon devices (DC and DD) start with a p-type float zone substrate with a 0.7 μm thick epitaxial ^{28}Si (500 ppm ^{29}Si) layer. A 35 nm thermal silicon oxide is grown at 900 °C with dichloroethene (DCE) followed by a 30 min, 900 °C N_2 anneal. The next layer deposited is a 200 nm amorphous silicon layer followed by a $5 \times 10^{15}\,\text{cm}^{-2}$, 35 keV arsenic implant at 0° tilt. The amorphous layers are crystallized later in the process flow to form a degenerately doped poly-silicon electrode. In the silicon foundry, the poly-Si is patterned and etched into a large scale region, a "construction zone" around $100 \times 100\,\mu\text{m}^2$ in size, that will later be patterned using e-beam lithography to form the nanostructure. After etching, ohmic implants are formed using optical lithography and implantation of As at $3 \times 10^{15}\,\text{cm}^{-2}$ density at 100 keV. An oxidation anneal of 900 °C for 13 min and an N_2 soak at 900 °C for 30 min follow the implant step and serves the multiple purposes of crystallizing, activating and uniformly diffusing the dopants in the poly-Si while also forming a SiO_2 layer (10–25 nm) on the surface of the poly-Si. This SiO_2 layer forms the first part of the hard mask layer used for the nanostructure etch in the construction zone. The second part of the hard mask is a 35 nm Si_3N_4 layer. An 800 nm thick field oxide is subsequently deposited using low pressure chemical vapor deposition (CVD) with tetraethoxysilane (TEOS) (this step is done by high density plasma CVD for the ^{28}Si devices). The field oxide is planarized using chemical mechanical polishing (CMP) leaving approximately 500 nm over the silicon and 300 nm over the poly-Si. Vias are etched to the conducting poly-Si and n+ ohmics at the silicon surface. The vias are filled with Ti/TiN/W/TiN. The tungsten is a high contrast alignment marker for subsequent e-beam lithography steps. Large, approximately $100 \times 100\,\mu\text{m}^2$ windows aligned to the construction zones are then etched in the field oxide to expose the underlying hardmask and poly-Si construction zone for nanostructure patterning. The last processing step for the devices in the silicon foundry is a 450 °C forming gas anneal for 90 min.

Phase 2 (nano-micro fabrication facility): The wafers are removed from the silicon foundry and subsequently diced into smaller parts, leading to 10 mm × 11 mm die, each containing 4 complete QD devices. The nanostructures are patterned using electron beam lithography and a thinned ZEP resist. The pattern is transferred with a two-step etch process. First, the SiN and SiO_2 hard mask layers are etched with a CF_4 dry etch, and an O_2 clean then strips the resist *in-situ*. The second etch step is to form the poly-Si electrodes, which is done with an HBr dry etch in the same chamber. The poly-Si etch is monitored using end-point detection in a large scale etch feature away from the active regions of the device. Wet acetone and dry O_2 cleans are used to strip the residual resist after the poly-silicon nanostructure formation. After the wet strips of the tungsten vias, a lift-off process is used for aluminum formation of bond pads to contact the ohmics and poly-silicon electrodes. The last step is a 400 °C, 30 minute forming gas anneal. For devices that are implanted with donors near the QD region, a second e-beam lithography and implant step was done. After the implant step (parameters provided in the main text), the photoresist was stripped with acetone and then the metal and residual organics were stripped from the surface using peroxide and RCA cleans, and then a dopant activation anneal was performed with the parameters indicated in the main text. The device was subsequently metallized using an Al lift-off process.

Final material stack in the QD region is Si/35 nm SiO_2/200 nm poly-Si/10–25 nm SiO_2/35 nm Si_3N_4.

Measurements. Electrical characterization of the devices was performed in various crystats: a storage dewar dip-stick for 4 K measurements, a dry 2 K cryostat, and a dilution refrigerator for 200 mK measurements. The quantum dots were tuned by low noise voltage supplies, and the quantum dot current was measured by conventional lock-in techniques. The systematic noise floor imparted by Johnson noise, shot noise, and instrument noise are estimated using a nominal SET current of 500 pA, SET resistance of 500 kΩ, ohmic lever arm of 0.3 eV/V, enhancement gate lever arm of 0.2 eV/V, and instrument noise powers of $50\,\text{nV/Hz}^{1/2}$. The Johnson noise amplitude is calculated to be $3\,\text{neV/Hz}^{1/2}$ for the 4.1 K measurements and $1.5\,\text{neV/Hz}^{1/2}$ for the 0.2 K measurements (which also include contributions from 500 kΩ cold filter resistors on the gates). The shot noise is computed to be $2\,\text{neV/Hz}^{1/2}$. The instrument noise output was measured to be $50\,\text{nV/Hz}^{1/2}$ for 100–1000 Hz. Assuming the instrument noise remains white for lower frequencies, we calculate a instrument noise contribution of $20\,\text{neV/Hz}^{1/2}$. These estimates include contributions from only the ohmic line and SET enhancement gate, so we multiply by 2 to include all other gate contributions, which combines to a total systematic noise floor of $0.04\,\mu\text{eV}^2/\text{Hz}$.

References

1. Coish, W. A. & Loss, D. Singlet-triplet decoherence due to nuclear spins in a double quantum dot. *Phys. Rev. B* **72**, 125337 (2005).
2. Dial, O. *et al.* Charge noise spectroscopy using coherent exchange oscillations in a singlet-triplet qubit. *Phys. Rev. Lett.* **110**, 146804 (2013).
3. Eng, K. *et al.* Isotopically enhanced triple-quantum-dot qubit. *Sci. Advances* **1**, e1500214 (2015).
4. Zimmerman, N. M. *et al.* Why the long-term charge offset drift in si single-electron tunneling transistors is much smaller (better) than in metal-based ones: Two-level fluctuator stability. *J. Appl. Phys.* **104**, 033710 (2008).

5. Zimmerman, N. M., Yang, C.-H., Lai, N. S., Lim, W. H. & Dzurak, A. S. Charge offset stability in si single electron devices with al gates. *Nanotechnology* **25**, 405201 (2014).
6. Muhonen, J. T. *et al.* Storing quantum information for 30 seconds in a nanoelectronic device. *Nat. Nanotechnology* **9**, 986 (2014).
7. Harvey-Collard, P. *et al.* Coherent coupling between a quantum dot and a donor in silicon. *Nature Communications* **8**, 1029 (2017).
8. Rudolph, M. *et al.* Coupling MOS quantum dot and phosphorus donor qubit systems. *IEEE IEDM,* 34-1 (2016).
9. Harvey-Collard, P. *et al.* High-fidelity single-shot readout for a spin qubit via an enhanced latching mechanism. *Phys. Rev. X* **8**, 2 (2018).
10. Gorman, S. K. *et al.* Extracting inter-dot tunnel couplings between few donor quantum dots in silicon. *New J. Phys.* **18**, 053041 (2016).
11. Bielejec, E., Seamons, J. & Carroll, M. Single ion implantation for single donor devices using geiger mode detectors. *Nanotechnology* **21**, 085201 (2010).
12. Singh, M. *et al.* Electrostatically defined silicon quantum dots with counted antimony donor implants. *Appl. Phys. Lett.* **108**, 062101 (2016).
13. Tracy, L. A. *et al.* Observation of percolation-induced two-dimensional metal-insulator transition in a si mosfet. *Phys. Rev. B* **79**, 235307 (2009).
14. Meirav, U., Kastner, M. A. & Wind, S. J. Single-electron charging and periodic conductance resonances in gaas nanostructures. *Phys. Rev. Lett.* **65**, 771 (1990).
15. DiCarlo, L. *et al.* Differential charge sensing and charge delocalization in a tunable double quantum dot. *Phys. Rev. Lett.* **92**, 226801(2004).
16. Stewart, M. D. & Zimmerman, N. M. Stability of single electron devices: Charge offset drift. *Appl. Sci.* **6**, 187 (2016).
17. Fujiwara, A. *et al.* Single electron tunneling transistor with tunable barriers using silicon nanowire metal-oxidesemiconductor field-effect transistor. *Appl. Phys. Lett.* **88**, 053121 (2006).
18. Simoen, E. & Claeys, C. The hysteresis and transient behavior of si metal-oxide-semiconductor transistors at 4.2 K. (i) the kink-related counterclockwise hysteresis regime. *J. Appl. Phys.* **73**, 3068 (1993).
19. Simoen, E. & Claeys, C. The hysteresis and transient behavior of si metal-oxide-semiconductor transistors at 4.2 K. (ii) pre-kink clockwise hysteresis regime. *J. Appl. Phys.* **73**, 3074 (1993).
20. Machlup, S. Noise in semiconductors: spectrum of a two-parameter random signal. *J. Appl. Phys.* **25**, 341 (1954).
21. Beaudoin, F. & Coish, W. A. Microscopic models for charge-noise-induced dephasing of solid-state qubits. *Phys. Rev. B* **91**, 165432 (2015).
22. Freeman, B. M., Schoenfield, J. S. & Jiang, H. Comparison of low frequency charge noise in identically patterned si/sio_2 and si/sige quantum dots. *Appl. Phys. Lett.* **108**, 253108 (2016).
23. Schriefl, J., Makhlin, Y., Shnirman, A. & Schön, G. Decoherence from ensembles of two-level fluctuators. *New J. Phys.* **8**, 1 (2006).

Acknowledgements

The authors wish to acknowledge M.D. Stewart Jr. and Binhui Hu from NIST for useful discussion during the preparation of this manuscript. This work was performed, in part, at the Center for Integrated Nanotechnologies, an Office of Science User Facility operated for the U.S. Department of Energy (DOE) Office of Science. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525.

Author Contributions

M.R., N.M.Z. and M.S.C. conceived the experiment. M.R., B.S., R.M. and N.M.Z. conducted the experiment. M.R., B.S. and R.M. analyzed the results. All authors reviewed the manuscript.

Additional Information

Supplementary information accompanies this paper at https://doi.org/10.1038/s41598-019-43995-w.

Competing Interests: The authors declare no competing interests.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.