# *Fabrication of High-Speed and High-Density Single-Flux-Quantum Circuits at NIST*

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***Abstract*—The development of a fabrication process for single-flux-quantum (SFQ) digital circuits is a fundamental part of the NIST effort to develop a gigahertz waveform synthesizer with quantum voltage accuracy. This paper describes the current SFQ fabrication process used at NIST's Boulder Microfabrication Facility based on Josephson junctions with niobium superconducting electrodes and self-shunted niobium-doped silicon barriers. The planned circuits will be used to explore metrology for advanced computing and communications. We will also describe anticipated process changes and innovations aimed toward further increasing circuit density and clock frequency.**

***Keywords*—Josephson junctions, self-shunted junction, RSFQ, superconducting integrated circuit, superconductor electronics***

## I. Introduction

For over 20 years, researchers at NIST have been developing quantum-accurate waveform synthesizers for ac voltage metrology. These voltage sources are fundamentally accurate in voltage amplitude and have perfect signal purity (distortion free) [1]. State-of-the-art circuits made with series arrays of Josephson junctions (JJs) have generated waveforms with frequencies up to 1 MHz with rms amplitude up to 2 V **Error! Reference source not found.**. Semiconductor pulse generators have been used to bias the long arrays of overdamped, self-shunted, SNS Josephson junctions. The goal now is to extend quantum-accurate waveform synthesis to gigahertz frequencies to provide advanced calibration tools for the telecommunications industry. One approach to accomplish this is by using digital SFQ circuits to directly generate digitally synthesized waveforms because it allows faster clock rates that will in turn enable synthesis of higher-performance oversampled waveforms. The first SFQ circuits we are developing will synthesize waveforms at rf frequencies at amplitudes of a few millivolts.

New technology is needed to extend quantum-accurate waveform generation into the gigahertz regime. The digital synthesis that is presently done using semiconductor electronics, needs to be clocked faster by at least a factor of 10, preferably at least 100 GHz. This will be achieved by replacing those semiconductor components with faster superconducting SFQ digital electronics **Error! Reference source not found.**. SFQ signal processing and waveform synthesizer circuits will be fabricated on the same chip.

## II. Fabrication Process

The circuits are fabricated on three-inch silicon wafers covered with 150 nm of thermal oxide. The fabrication process of these circuits includes four niobium layers with partial planarization on the insulating layers below the third niobium layer, as shown schematically in Fig. 1. Either the bottom or top niobium layers may be utilized as the ground plane, as shown in Fig. 2. Wiring layers are made of niobium sputtered in argon and etched using sulphur hexafluoride reactive ion etching (RIE).

An important and distinctive feature of our fabrication process is the broad tunability of the electrical properties of our junctions. Our barriers, which consist of co-sputtered niobium and silicon, are adjusted by changing the sputter rate of the

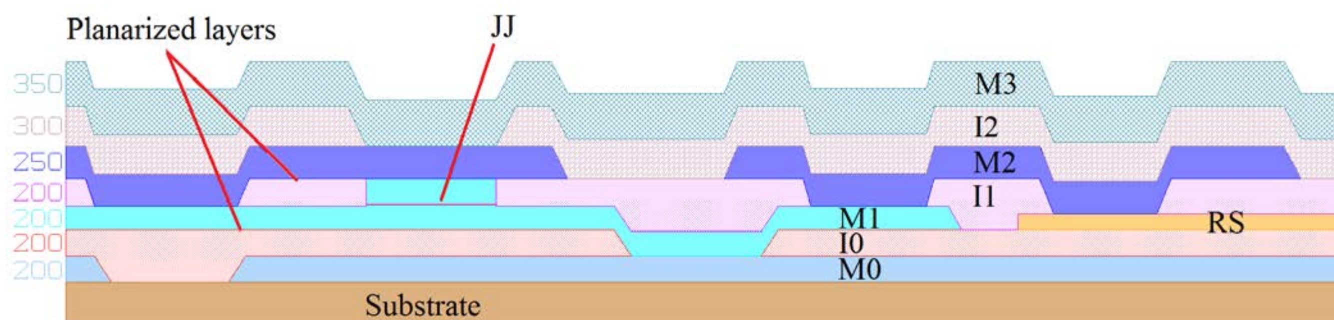


Fig. 1. Schematic of cross section of NIST SFQ digital fabrication process. M# designates niobium layers, I# designates insulator layers, RS is the resistors layer, JJ is the self-shunted junction with niobium silicide barrier.

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niobium and the barrier thickness. For waveform synthesizer applications, we tune the barrier so that the junctions are damped and their characteristic frequency allows for fast operation of digital SFQ circuits **Error! Reference source not found.**. Self-shunting of the junctions is critical for scaling future circuits to higher density because it avoids external shunt resistors that take significant chip area. It is also important for achieving faster circuits by eliminating the parasitic inductances associated with shunts. The current process yields junctions with a critical

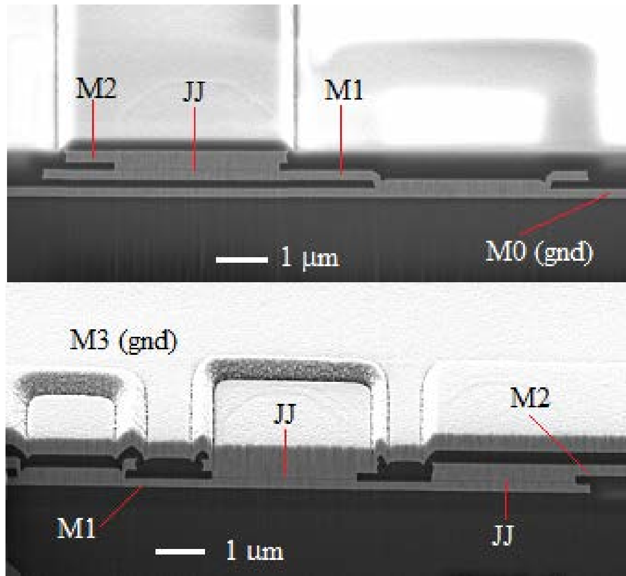


Fig. 2. Cross section images of junctions, top image shows JJ grounded to M0, bottom image shows JJ grounded to M3.

current density ($J_c$) of 4.2 kA/cm$^2$. This value of $J_c$ was chosen as the initial step to develop the cell library and the fabrication process.

Insulator layers consist of silicon oxide deposited by plasma enhanced chemical vapor deposition (PECVD). Back side helium flow during deposition ensures that the wafer temperature remains under 100 C. Planarization, which is done on insulating layers I0 and I1, primarily follows the typical caldera method **Error! Reference source not found.**. First, an oxide of 500 nm thickness is deposited to cover the patterned metal. This is covered with photoresist in areas around where the underlying metal has been etched. By timed etch of the oxide (200 nm), calderas are left over a flat surface. Next, chemical-mechanical polishing (CMP) removes 100 nm of the remaining oxide leaving a flat surface of (200 nm)-thick oxide over the metal and (400 nm)-thick oxide over the previous insulator, as shown in Fig. 3. Thickness accuracy after the process is +/- 20 nm.

Resistors made of palladium-gold alloy with sheet resistance of 2 Ω per square are e-beam evaporated on a bi-layer of lift-off resist and imaging resist. The contact pads are made with a second sputter deposition of palladium-gold. These pads

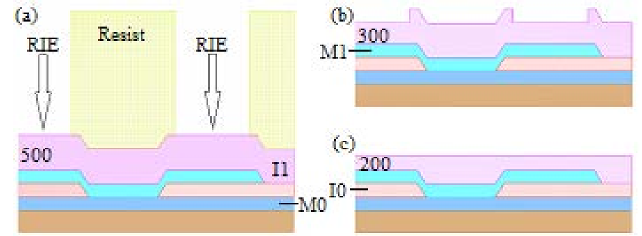


Fig. 3. Steps for planarization of insulator layers. (a) Extra thickness of insulator deposited, resist covering areas lower than surroundings, RIE. (b) After RIE calderas are etched. (c) CMP removes caldera protrusions and an additional 100 nm of oxide, leaving a flat surface.

are lifted off with a single layer resist because the size tolerances for these features are more relaxed. Table I shows the thicknesses and materials of each of the layers in the process.

## III. Process Developments

Towards the goal of producing quantized waveforms in the gigahertz frequency range, it will be necessary to make SFQ circuits clocked at hundreds of gigahertz. This requires maximizing the critical current density, $J_c$, of the junctions, since the operating speed of these circuits scales approximately as $\sqrt{J_c}$ for a fixed JJ damping **Error! Reference source not found.**.

TABLE I. Layers

| Layer | Thickness (nm) | Material | Minimum feature size (µm) |
|---|---|---|---|
| M0 | 200 | Niobium (sputtered) | 0.5 |
| I0 | 200 | SiOx (PECVD) | 0.75 |
| M1 | 200 | Niobium (sputtered) | 0.75 |
| JJ | 10 | Niobium silicide (cosputtered) | 1.0 |
| I1 | 200 | SiOx (PECVD) | 0.6 |
| RS | 135 | Palladium-gold (evaporated) | 0.75 |
| M2 | 250 | Niobium (sputtered) | 1.0 |
| I2 | 300 | SiOx (PECVD) | 1.0 |
| M3 | 350 | Niobium (sputtered) | 1.0 |
| PADS | 200 | Palladium-gold (sputtered) | 2.0 |

The process that aims to maximize circuit operating speeds will use junctions with $J_c$ = 100 kA/cm$^2$ and defined by electron-beam lithography. For this $J_c$, the JJ sizes need to decrease to deep submicrometer dimensions, which is beyond the capabilities of the stepper used in the current process, to maintain adequate critical current values.

SFQ circuits with self-shunted Nb-Si junctions and $J_c$ = 85 kA/cm$^2$ have already been demonstrated at NIST [7]**Error! Reference source not found.**. The maximum operating frequency of those circuits was 300 GHz. We believe that the maximum frequency of those circuits was limited by both the fabrication process and the design tools used at that time, neither of which were optimal for these circuits. For the following reasons, we anticipate better circuit performance with the new process, including better yield and an increase in the maximum operation frequency. New design tools have been implemented that have allowed circuit parameters to be optimized for higher speeds. A new e-beam writer, recently acquired by the Boulder Microfabrication Facility, has enabled smaller, more uniform features sizes that should translate into better control of JJ critical currents and better uniformity. Incorporation of CMP will allow for better contact to smaller junctions and increased current density of writing interconnects.

Future plans to increase circuit density include investigating the replacement of geometric inductors with the Josephson inductance of non-switching vertically stacked junctions [8]. A modified fabrication process would permit a switching junction and a stacked-JJ inductor to reside within the same vertical stack, almost eliminating all the area occupied by a geometric inductor. The combination of small, high-$J_c$, self-shunted junctions and stacked JJ inductors will enable a significant increase in SFQ circuit density.

Other planned improvements to the process include the introduction of stud vias, which will improve the connection between metal layers by decreasing parasitic inductance, and improving planarization, which will allow the addition of more metal layers as the circuits increase in complexity.

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