Scalable, High-Speed, Digital Single-Flux-Quantum Circuits at NIST

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***Abstract*—We have designed, fabricated, and tested niobium-based single-flux quantum (SFQ) digital and mixed-signal circuits based on intrinsically shunted Josephson junctions with tunable niobium-doped amorphous-silicon barriers. This process can be extended to demonstrate dense high-speed SFQ circuits. We have assembled a package of readily-available software design tools for designing, simulating, and optimizing circuits. We have developed a scalable fabrication process at NIST that includes four niobium metal layers and chemical-mechanical planarization of the insulating layers. Through our participation in IARPA's Cryogenic Computing Complexity (C3) program, we have built liquid-helium cryogenic probes and test systems with 40 and 80 input/outputs for characterizing advanced SFQ circuits at speeds up to 26 GHz. Test results of basic SFQ circuits agree with simulations and show large dc bias-current margins.**

Keywords—Rapid single flux quantum (RSFQ); Josephson junctions; Josephson logic; superconducting device fabrication; superconducting integrated circuits

I. INTRODUCTION

Superconducting digital logic and interconnects, with compatible cryogenic memories, are being investigated for their potential as an energy-efficient technology for large-scale computing [1]. Recent work has demonstrated significant improvements in the static power dissipation of high-speed single-flux-quantum (SFQ) circuits [2,3] and has quantified the energy efficiency of adiabatic quantum flux parametron (AQFP) circuits [4,5]. Advances in compatible cryogenic memories include switchable Josephson junctions (JJs) consisting of multi-layer barriers containing ferromagnetic materials [6,7], spintronic-based devices scaled to cryogenic temperatures [8-10], and larger arrays of traditional loop-based superconductor memories.

A significant challenge for realizing the potential of these technologies is the ability to geometrically scale the devices so that circuits with millions of JJs and sufficient memory capacity can be fabricated on a standard-sized (~1 cm^2) chip. Both circuit component size requirements and fabrication capabilities are presently limiting these SFQ circuit densities. Components such as shunt resistors for the Josephson junctions and niobium wire inductors contribute significantly to the size of the circuits.

Digital and mixed-signal SFQ circuits with cryogenic memory and based on the propagation of SFQ electrical pulses are of significant interest to NIST for metrology applications related to advanced computing, on-chip signal processing, rf waveform synthesis, and ac voltage standards [11-13]. Significant increases in circuit density will be required to achieve the circuit performance, functionality, complexity, and speed desired for these applications. SFQ circuit components, designs, and materials that are inherently scalable are critical to increasing these circuit densities.

NIST has developed new capabilities to design, simulate, optimize, and fabricate SFQ digital and mixed-signal circuits at the NIST Boulder Microfabrication Facility (BMF). The new fabrication process for these superconducting integrated circuits is an extension of the fabrication process used for our dc and ac voltage standard chips, containing over 265,000 JJs [12,13]. Through our participation on IARPA's Cryogenic Computing Complexity (C3) program, NIST has built cryogenic test infrastructure for measuring and evaluating SFQ circuits of moderate complexity with clock rates up to 26 GHz. This extended abstract describes the NIST SFQ circuit design, fabrication, and test capabilities in more detail.

II. CIRCUIT DESIGN

A. Design Flow

Figure 1 shows the design flow that NIST uses for the SFQ circuits fabricated at the BMF. Commercial electronic design automation (EDA) tools comparable in functionality to those used to design CMOS circuits are not available for designing SFQ circuits [14,15]. Instead, we assembled a package of inexpensive tools that are readily available and have been used by other researchers to successfully design, simulate, and optimize digital SFQ circuits with less than a few thousand Josephson junctions.

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First a circuit schematic is drawn and a pre-layout simulation is performed using tools specifically tailored for superconducting circuits. Circuit components are optimized to maximize the range of dc bias currents (margin) that give correct operation. This is followed by circuit layout and calculation (extraction) of the inductance of the wiring and other circuit components. Design rules specific to our fabrication process, for example the minimum allowable JJ diameter, are checked. The circuit is then simulated and

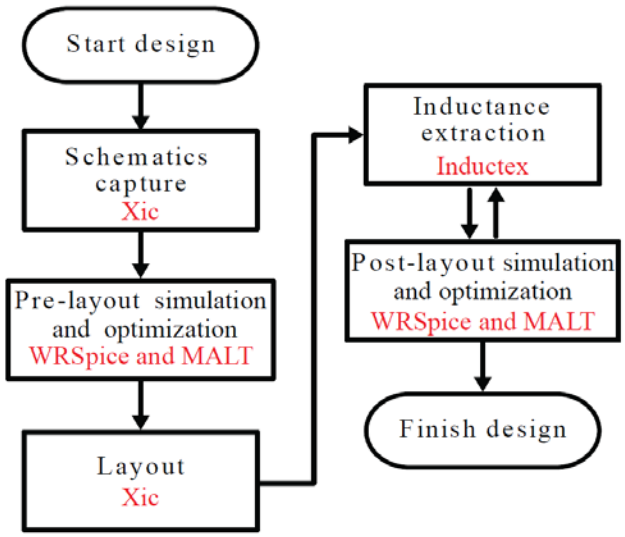

Fig. 1. Design flow for SFQ digital circuits fabricated at NIST.

re-optimized, using the extracted inductance values from the layout. If necessary, the inductance extraction and post-layout simulation cycle is repeated to confirm functionality and maximize current-bias margin. A final design rules check is then done.[1]

B. Design Details

Examples of simple rapid SFQ (RSFQ) circuits, such as a Josephson transmission line (JTL), SFQ-to-DC converter, DC-to-SFQ converter, T flip-flop (TFF), and D flip-flop (DFF), were taken from the literature [16]. These designs were modified for our fabrication process and then optimized, using published bias margins as a guide. We then fabricated and tested these circuits and the whole cycle was repeated to further optimize the design and layout for out fabrication process.

As explained below, our fabrication process uses self-shunted junctions, which allows for compact and dense circuits by eliminating the external shunt resistors required for damping junctions and the parasitic inductances associated with shunts. Our JJs are located between layers M1 and M2 (Fig. 2). Designating M3 as the ground plane, closer to the junctions, also reduces parasitic inductances and improves operating margins and operating frequencies [17].

[1]Commercial instruments and design tools are identified in this paper to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified are necessarily the best available for the purpose.

III. Fabrication

Circuits are fabricated on oxidized, three-inch silicon wafers. The process consists of four niobium metal layers with chemical-mechanical planarization of the silicon-oxide insulating layers below the third niobium layer. Process cycle time is seven days for one man-shift. More details of the process are given by D. Olaya et al. in a poster at this conference (ISEC 2017).

Our process uses superconductor-normal metal-superconductor (SNS) Josephson junctions with amorphous niobium-doped silicon barriers. These $Nb/Nb_xSi_{1-x}/Nb$ junctions do not require external shunt resistors for damping and proper SFQ circuit operation [18]. The composition and hence the shunt resistance (R_n) and critical current density (J_c) of the barriers can be tuned to selected values of JJ damping, critical current (I_c), area, and characteristic frequency (scaled by the I_cR_n product) as needed for a wide range of applications. The JJs using M1 as the bottom electrode have a targeted J_c of 4.2×10^7 A/m^2, area of ~ 3 μm^2, I_cR_n ~ 0.2 mV, and Stewart-McCumber damping parameter $\beta_c \sim 1$. Future work will target higher J_c, smaller areas, and higher JJ characteristic frequencies to enable higher-speed SFQ circuits.

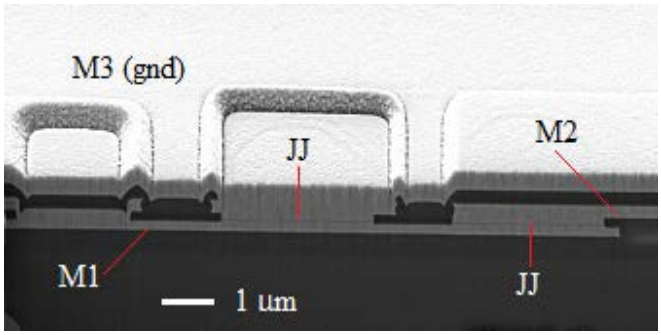

Fig. 2. FIB-SEM cross-sectional image of wafer from NIST's four-metal layer process. Josephson junctions (JJ) and Nb metal layers M1, M2, and M3 are indicated. M0 wiring layer is not shown. Nominal thicknesses are 200 nm, 250 nm, and 350 nm for M1, M2, and M3, respectively.

IV. Test Infrastructure and Results

NIST has built a cryogenic test infrastructure for measuring and evaluating high-speed superconducting digital and mixed-signal circuits. Since our laboratory has a helium recovery and liquefier system, we use immersion probes that are inserted into 100-liter liquid helium storage dewars. Our existing probe has 40 high-speed (26 GHz) input/outputs (I/O) and is capable of handling 5 mm x 5 mm chips. We are also constructing a second probe with 80 high-speed I/Os capable of handling chip or module sizes up to 32 mm x 32 mm.

The 40 I/O probe, as shown in Fig. 3, uses 40 lines of 0.047" semi-rigid coax, with SMA connectors at the room temperature (top) end of the probe and non-magnetic GPPO connectors at the cold end. We have found that preconditioning the coaxial cables by thermally cycling the cables to 200 C prior to installing the connectors is essential for improving the integrity and reliability of the coax-to-GPPO connections. A circular, flexible circuit board printed with forty 50-ohm coplanar waveguides is soldered to the GPPO connectors and

includes 40 pair of beryllium-copper spring fingers that provide press contacts to pads on the perimeter of the chip.

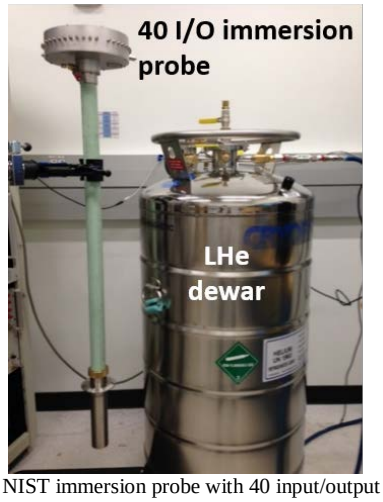

Fig. 3. NIST immersion probe with 40 input/output lines.

We have acquired electronics for low-noise dc and ac biasing of the chips, and high-speed pattern generators and bit error rate detectors for high-speed testing of digital circuits. Circuit functionality, bias margins, bit error rates, and power dissipation can be measured. We have also purchased a commercial electronic test system for biasing and low-speed (1 kHz to 500 kHz) characterization of logic functionality of superconductive circuits. Fig. 4 shows 4 K test results from some of our digital circuits using this low-speed system, comparing the simulated and measured range of dc bias current values for which the circuits work correctly. The horizontal axis is the deviation of the bias current (I) from the design bias value (I_b), normalized by I_b (i.e. $(I-I_b)/I_b$).

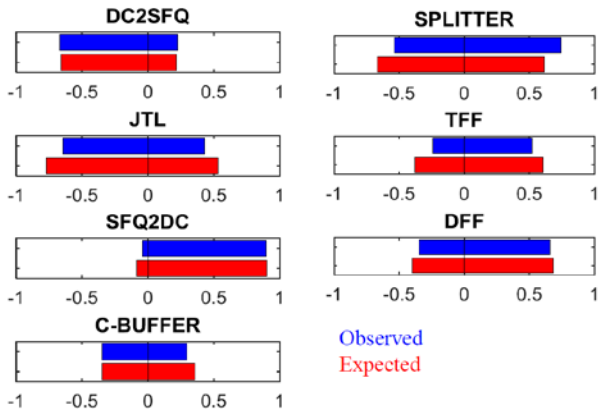

Fig. 4. Simulated vs. 4 K measured dc bias current margins (I-Ib)/Ib for our SFQ digital circuits. Measurements used 1 kHz clock rate.

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