Comprehensive Capacitance–Voltage Simulation and Extraction Tool Including Quantum Effects for High-k on Si_xGe_{1-x} and $In_xGa_{1-x}As$: Part I—Model Description and Validation

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***Abstract*— High-mobility alternative channel materials to silicon are critical to the continued scaling of MOS devices. The analysis of capacitance–voltage (C–V) measurements on these new materials with high-k gate dielectrics is a critical technique to determine many important gate-stack parameters. While there are very useful C–V analysis tools available to the community, these tools are all limited in their applicability to alternative semiconductor channel MOS gate-stack analysis since they were developed for silicon. Here, we report on a new comprehensive C–V simulation and extraction tool, called CV Alternative Channel Extraction (ACE), that incorporates a wide range of semiconductors and dielectrics with the capability to implement customized gate stacks. Fermi–Dirac carrier statistics, nonparabolic bands, and quantum mechanical effects are all implemented with options to turn each of these off as the user desires. Interface state capacitance (C_{it}) is implemented using a common model for systems like Si and Ge. A more complex C_{it} model is also implemented for III–Vs that accurately captures frequency dispersion in accumulation that arises from tunneling. CV ACE enables extremely fast simulation and extraction and can accommodate measurements performed at variable temperatures and frequencies to allow for a more accurate extraction of interface state density (D_{it}).**

***Index Terms*— III–V semiconductors, C–V Simulation, CV Alternative Channel Extraction (ACE), D_{it} extraction, quantum mechanical (QM) effects, thin oxides.**

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I. Introduction

FOR current and future MOSFET technology, various alternative semiconductor channel materials are used or being considered to improve device performance, including Si-Ge [1], germanium [2]–[4], and III–V compound semiconductors [5]–[7]. These high-mobility channel materials, used in conjunction with high-k dielectrics [8] and metal gates may provide important advantages, leading to increased device density and performance while driving down the cost of manufacturing and energy consumption. However, characterizing experimentally fabricated gate stacks on these new channel materials is challenging.

The analysis of MOS capacitance–voltage (C–V) measurements has been a critical technique to determine many important gate-stack parameters, such as the equivalent oxide thickness (EOT), substrate doping density, flat-band voltage, and the distribution and density of interface traps (D_{it}). C–V measurements are especially instrumental for new gate stacks since results can be obtained on MOS Capacitors (MOSCAPs) which are much simpler and quicker to fabricate compared to the full MOSFET. While there are very useful C–V analysis tools available to the community, most notably the ubiquitous North Carolina State University (NCSU) CVC code in [9], these tools all have certain characteristics that limit their applicability to alternative semiconductor channel MOS gate-stack analysis since they were developed for silicon where quantum effects are less prevalent compared to higher performance materials.

It is well established that the potential well at the semiconductor-oxide interface confines the free carriers normal to the interface and creates a 2-D electron or hole gas [10]. Carrier confinement in strong inversion and accumulation splits the classically continuous energy bands into discrete sub-bands where the energy level of the first sub-band does not coincide with the conduction or valence band edges. Additionally and importantly when considering capacitance, the carrier centroid is shifted away from the semiconductor-dielectric interface compared to the classical carrier density depth profile [11]. This leads to an additional quantum capacitance in series with the oxide capacitance. The total effect of the quantization is a reduction in the carrier density in the semiconductor as compared to the classical model.

Quantum effects are generally much more important in advanced devices based on alternative materials compared to historical silicon devices for two reasons. First, scaling has reduced EOT and increased channel doping density. As a result, the electric field at the oxide-semiconductor interface has significantly increased, increasing the depth of the well and the quantum mechanical (QM) repelling of the charge carriers away from the interface. Second, the improved performance of alternative materials is often linked to the lower effective mass. While lighter effective mass particles usually travel faster, they inevitably also suffer more from quantum confinement effects, becoming important at lower electric fields.

Several methods have been used to model and simulate the QM effects of thin dielectrics and high doping density semiconductors. These methods can be divided into two categories: 1) the self-consistent solution of the Schrödinger and Poisson (SP) equations [12]–[15] and 2) modification of the classical calculation to account for the QM effects [9], [11], [16]–[23]. Solving the SP equations self-consistently is certainly the more comprehensive and accurate technique for calculating the charge in the MOS gate-stack. However, this method of simulation is computationally intensive and time-consuming and is primarily a forward model; i.e., it is hard to use in the extraction of gate-stack parameters from experimental data. Modifying the classical method of calculation is computationally much cheaper compared to a self-consistent SP solver and can be used to extract experimental data. Unfortunately, methods of the second kind are limited, especially for alternative materials.

QM corrections to the classical method have been performed previously in a variety of ways. Hänsch *et al.* [16] proposed a reduction in the silicon density of states to account for the charge centroid shift. There, the density of states is reduced near the surface and gradually returned to the proper value in the bulk. Hänsch's model is simple, but the splitting of the bands into discrete energy levels and the resultant bandgap change was not taken into consideration making this model incomplete. The model proposed in [11] includes both the displacement of the charges away from the semiconductor-dielectric interface as well as the splitting of the bands. The discrete sub-bands are calculated under the assumption that the potential well has a triangular shape and the total QM effects can be accounted for by modifying the surface potential as follows:

$$\psi_s^{\mathrm{QM}} = \psi_s^{\mathrm{CONV}} + \frac{13}{9}\Delta\epsilon \tag{1}$$

where $\frac{13}{9}\Delta\epsilon$ is the change in surface potential due to the combination of both the change in effective bandgap and the shift in charge centroid, which is deduced from an empirical fit to silicon experimental data. The expression for $\Delta\epsilon$ derived by van Dort is

$$\Delta\epsilon \approx \beta(\epsilon_s/4qk_BT)^{\frac{1}{3}} \times \max(E_s(0),0)^{\frac{2}{3}} \tag{2}$$

where, E_s is the electric field perpendicular to the surface of silicon and β is the proportionality factor used for accurate fitting of the model to experimental data.

The van Dort model harbors a singularity, and Hareland *et al.* [20] modified the van Dort equations to better fit at low doping densities

$$\Delta\epsilon = \begin{cases} \beta\left(\dfrac{\epsilon_s}{4qk_BT}\right)^{\frac{1}{3}}(\mid E_s \mid -10^5)^{\frac{2}{3}}, & \text{for } E_s > 10^5 \text{ kV/cm} \\ 0, & \text{for } E_s < 10^5 \text{ kV/cm.} \end{cases} \tag{3}$$

However, the models of van Dort *et al.* [11] and Hareland *et al.* [12], [20] were developed only for inversion in silicon-based devices. Accurate modeling of the accumulation capacitance is also necessary to obtain valuable information about the gate-stack, including the flat-band voltage, EOT, D_{it}, and in some cases border trap density [24]. Therefore, QM effects in accumulation are arguably more important for data extraction in traditional MOSCAP C–V measurement and analysis than inversion. It should also be noted that in weak accumulation and depletion, the electric field is very small and no quantum well is formed rendering QM effects negligible in those operating conditions.

Hareland *et al.* [21] did propose a QM correction for accumulation which is similar to that of the one for inversion, with the addition of doping density-dependent parameters. Hauser and Ahmed [9] proposed a van Dort-like surface potential correction model targeting silicon-based MOS devices in the accumulation region

$$\Delta\epsilon = (\hbar^2/2m^*)^{\frac{1}{3}}\left(\frac{9}{8}\pi q E_s\right)^{\frac{2}{3}} \tag{4}$$

using m^*, the carrier effective mass, as the comparatively simpler fitting parameter. However, all of the methods discussed thus far, utilized a physical grid to simulate the surface electric field to apply the QM corrections, which is computationally expensive. Vogel *et al.* [25] combined the two methods proposed by Hareland *et al.* [12], [20], [21] and developed a model to simulate the C–V profile for silicon in both accumulation and inversion without the use of a physical grid. In that method, to calculate the field, the effective change in bandgap needs to be calculated. However, the effective widening of the bandgap is dependent on the electric field hence requiring a simultaneous solution of two interdependent equations.

In this paper, we combine aspects of all of those prior models, achieving a rapid C–V simulation and extraction tool that does not require a physical grid nor the solution of the aforementioned interdependent equations. As a result, the computational time is reduced tremendously. Moreover, as will be shown in the later sections, the model proposed here can be applied to any bulk semiconductor (Si, Ge, Si_xGe_{1-x}, GaAs, $In_xGa_{1-x}As$, and so on), once the proper QM corrections are benchmarked and applied [32]. The software, which we call C–V Alternative Channel Extraction (ACE), is developed using C++ programming language. The program can simulate a forward model in less than 50 ms, which is orders of magnitude faster than fully solving the SP equations, which can take anywhere from minutes to several hours depending upon the level of complication.

In Section II, the classical theory with the proposed QM corrections is discussed. In Section III, the QM correction factors that are used in the proposed model are extracted by benchmarking the model to the solution from an SP solver developed at UT-Dallas utilizing multiple EOTs and doping densities. In Section IV, a short comparison of the model to experimental C–V curves is demonstrated. A summary and conclusion are presented in Section V. In part II [33], detailed analysis of experimental C–V data using ACE, in particular the extraction of interface state density (D_{it}), will be presented.

II. Description of Model

A. Classical Method

1) Computing Charge: Our method starts with calculating the number of both holes and electrons for a wide range of Fermi level positions ($\phi_s = (E_F - E_i)/q$) using the Fermi–Dirac (FD) integral of order 1/2 taking nonparabolic bands into account (important for alternative channel materials, especially III–V semiconductors)

$$n = N_C \Im_{\frac{1}{2}}(\eta_c) \quad \text{and} \quad p = N_V \Im_{\frac{1}{2}}(\eta_v) \tag{5}$$

where

$$N_C = 2\left(\frac{2\pi m_0 m_e k_B T}{h^2}\right)^{3/2} \tag{6a}$$

$$N_V = 2\left(\frac{2\pi m_0 m_h k_B T}{h^2}\right)^{3/2} \tag{6b}$$

$$\Im_{\frac{1}{2}}(\eta) = \frac{2}{\sqrt{\pi}} F_{\frac{1}{2}}(\eta) \tag{7}$$

where the $F_{(1/2)}(\eta)$ is the Fermi integral [not to be confused with the FD integral used in (5)] of order 1/2

$$F_{\frac{1}{2}}(\eta) = \int_0^\infty \frac{(1+2\xi\alpha)\sqrt{\xi(1+\xi\alpha)}d\xi}{1+e^{\xi-\eta}} \tag{8}$$

$$\eta_C = \frac{E_F - E_C}{k_B T} \quad \text{and} \quad \eta_V = \frac{E_V - E_F}{k_B T} \tag{9}$$

where

m_0 $=9.11 \times 10^{-31}$ kg, rest mass of electron;
m_e =electron effective mass in conduction band;
m_h =hole effective mass in valence band;
E_C =conduction band edge energy measured from the intrinsic energy E_i;
E_V =valence band edge energy measured from E_i;
α =nonparabolicity factor which we use for III–V semiconductor band structures and α calculated in the usual manner [26]

$$\alpha = \frac{(1-m_e)^2}{E_g}. \tag{10}$$

2) Computing Surface Potential and Flat-Band Voltage: The Fermi level in the bulk is determined by

$$p - n + N_d - N_a = 0 \tag{11}$$

where

$$N_d = N_{\text{dop}}/(1 + 2e^{(E_F - E_C - E_g/2)/(k_B T)}) \tag{12}$$

$$N_a = N_{\text{dop}}/(1 + 4e^{(-(E_V - E_F) - E_g/2)/(k_B T)}) \tag{13}$$

where, N_{dop} is the magnitude of the bulk doping density. The bulk potential is determined from E_F, which is found by solving (11)

$$\phi_B = E_{F,\text{bulk}}/q. \tag{14}$$

The surface potential is calculated from the initial Fermi level position and the calculated bulk Fermi level position

$$\psi_s = \phi_s - \phi_B. \tag{15}$$

The surface electric field is calculated by integrating the number of carriers with respect to the potential from the semiconductor bulk to the surface

$$E_s = \sqrt{\left|\frac{-2q}{\epsilon_s \epsilon_0}\int_{\text{Bulk}}^{\text{Surface}} (p - n + N_d - N_a)d\phi\right|}. \tag{16}$$

The semiconductor charge is calculated using

$$Q_s = -\text{sign}(\psi_s)\epsilon_s \epsilon_0 E_s \tag{17}$$

and the substrate capacitance is

$$C_s = \frac{dQ_s}{d\psi_s}. \tag{18}$$

The work function difference between the semiconductor and the gate metal is

$$\phi_{\text{ms}} = \phi_m - \left(\chi_s + \frac{E_g}{2} - \phi_B\right) \tag{19}$$

where, χ_s is the electron affinity of the semiconductor. The flat-band voltage is calculated using

$$V_{\text{fb}} = \phi_{\text{ms}} - \frac{Q_{\text{ox}}}{C_{\text{ox}}} \tag{20}$$

where, Q_{ox} is the oxide charge density.

TABLE I
SEMICONDUCTOR PARAMETERS USED IN ACE

	x	ϵ_s	$\chi_s(eV)$	$E_g(eV)$	m_e	m_h
Si_xGe_{1-x}	0.0	16.20	4.00	0.66	0.56	0.34
	0.5	13.95	4.05	0.92	1.06	0.58
	0.6	13.50	4.05	0.96	1.06	0.62
	0.75	12.83	4.05	1.02	1.06	0.63
	1.0	11.70	4.05	1.12	1.08	0.81
$In_xGa_{1-x}As$	0.0	12.90	4.07	1.42	0.063	0.51
	0.2	13.23	4.24	1.14	0.055	0.49
	0.53	13.90	4.51	0.75	0.041	0.46
	0.7	14.30	4.65	0.59	0.034	0.44
	1.0	15.15	4.90	0.35	0.023	0.41

3) Interface State Charge and Capacitance: For the interface state defect density, the charge is calculated using the FD distribution

$$Q_{it} = q\int_{-\infty}^{\infty} \frac{D_{it}dE}{1+e^{(E-\phi_s)/k_BT}}. \tag{21}$$

And the capacitance due to interface states is calculated

$$C_{it} = \frac{dQ_{it}}{d\psi_s}. \tag{22}$$

4) Total Capacitance and Gate Voltage: Including the interface state response, the gate voltage and total capacitance is calculated by

$$V_g = V_{fb} + \psi_s - \frac{Q_s}{C_{ox}} + \frac{Q_{it}}{C_{ox}} \tag{23}$$

$$C = \left(\frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}/(1+\omega^2\tau^2)}\right)^{-1} \tag{24}$$

where, τ is the time constant of the interface states and $\omega = 2\pi f$, is the angular frequency of the ac signal during measurement.

For device parameter extraction, a nonlinear least squares curve fitting algorithm [27] is employed. The semiconductor parameters that are used in the classical simulation are given in Table I.

B. Quantum Mechanical Correction

To correct the classical calculations for QM effects, the surface potential is modified according to the following equation:

$$\psi_s^{QM} = \psi_s^{CONV} + \Delta\epsilon/q. \tag{25}$$

The correction to the surface potential ($\Delta\epsilon/q$) due to QM effects depends on the transverse electric field as follows:

$$\Delta\epsilon = \beta\left(\frac{\epsilon_s\epsilon_0}{300\times 4qk_B}\right)^{\frac{1}{3}}[f(E_s)]^{\gamma} \tag{26}$$

where

$$f(E) = \left(\frac{(E)^2}{ae^{-(|E|/\sigma)^2} + |\ E\ |^{4/3}}\right)^{3/2}. \tag{27}$$

In our approach, instead of directly using E_s, we use a function $f(E)$. This function, first used in [28], eliminates the flat-band singularity at $E_s = 0$ while retaining the asymptotic nature of the term E_s^{γ}. In the function $f(E)$, a and σ are adjustable parameters dependent on the semiconductor material and independent of doping type or magnitude of doping density. β and γ have different values in accumulation and inversion and are also different for p-type and n-type semiconductors but do not depend on the magnitude of doping density. It should be noted that the a, σ, γ, and β terms do not have any physical significance. They are fitting parameters that enable us to map the classical C–V simulations to quantum mechanically correct C–V simulations empirically.

The conventionally calculated surface potential (ψ_s^{CONV}) in (17) and (18) is substituted with the modified surface potential (ψ_s^{QM}). The rest of the equations, (19)–(24) are used to complete the simulation.

C. Self-Consistent Schrödinger–Poisson Solver

To find the QM correction factors, we first solve the SP equations self-consistently to generate a fully quantum mechanically correct C–V curve. We then empirically map the simulation described in sections II-A and II-B to that S-P solution. For this purpose, we have developed a self-consistent SP solver. We account for holes and electrons and take our simulation region in the semiconductor large enough to encompass the depletion region so that the capacitance in accumulation, depletion, and inversion can be calculated quantum mechanically. Similar to the classical method, the band offset between the semiconductor and the dielectric is not considered, i.e., the bandgap of the dielectric is considered infinite (the exception to this is for D_{it} extraction in III–V devices where tunneling into defects located in the dielectric impacts the C–V response, which will be discussed in detail in the second part of this paper). The Schrödinger equation is solved for each inequivalent valley invoking the effective mass approximation. We denote the x-direction as the direction in which the electric field is applied and the y-z direction as the two perpendicular directions. The valleys whose axes align to the xyz-direction, such as the X-valleys in a (100) oriented wafer, are given their respective masses along the different directions. If the valleys do not align with the axes, e.g., for the L-valleys in a (100) oriented wafer, the mass tensor is projected on the xyz-directions. The Schrödinger equation is uniformly discretized in the x-direction using the finite difference method and solved using a sparse-eigenvalue solver. The charge is computed by integrating over k_y and k_z weighing each wave function with the FD distribution and by accounting valley and spin degeneracy. Electrons and holes present a negative and positive contribution to the charge density, respectively.

Poisson's equation is discretized on the same grid as the Schrödinger equation. In the bulk, Neumann boundary conditions are applied while at the oxide-semiconductor interface, mixed boundary conditions are applied to account for the gate bias and the potential drop over the oxide, where the wave function penetration into the oxide layer is not considered.

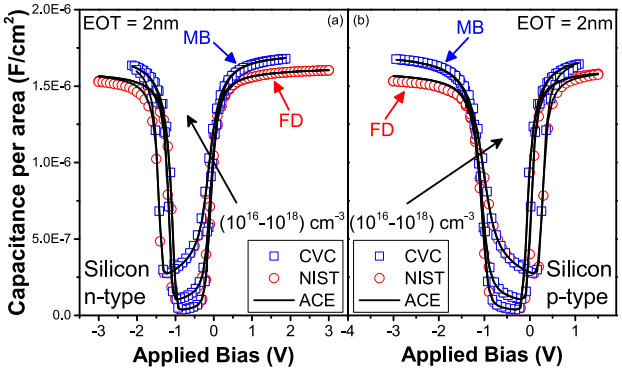

Fig. 1. Comparison between CVC (NCSU) [9], NIST [25], and ACE for classically calculated EOT of 2 nm with three different doping densities (10^{16}, 10^{17}, and 10^{18} cm^{-3}) for (a) n- and (b) p-type doped Si. ACE matches these other accepted codes for both MB and FD distribution functions.

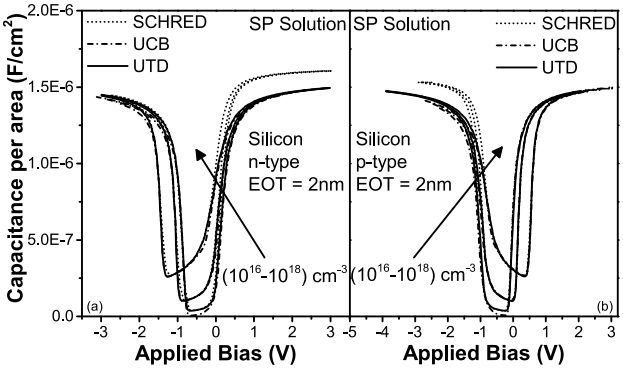

Fig. 2. Comparison between different SP solvers UCB [30], SCHRED [31], and UTD for 10^{16} cm^{-3} to 10^{18} cm^{-3}. (a) n- and (b) p-type doped Si with 2-nm EOT is used in the simulations. The UTD code compares favorably with the other SP solvers.

The error introduced in this assumption leads to a discrepancy between the physical and simulated capacitance up to 3% making the impact on the analysis of our extracted parameters minimal. The Schrödinger equations for different valleys are solved self-consistently with Poisson's equation using Broyden's method [29]. Obtaining the charge from the SP equation for two biases $V - \delta V/2$ and $V + \delta V/2$, the capacitance can be calculated as

$$C(V) = \frac{(Q(V + \delta V/2) - Q(V - \delta V/2))}{\delta V}. \tag{28}$$

While an improved bandstructure method like k.p or tight binding would improve the accuracy of our calculations, we have chosen to use a multiple-valley effective mass approach. In this way, we can maintain a uniform simulation methodology in inversion, accumulation, and depletion while maintaining a reasonable simulation time.

III. Model Validation

A. Classical Simulation

Fig. 1 shows the resultant C–V profiles obtained from CV ACE simulations using both FD and Maxwell–Boltzmann (MB) distribution functions and compares the output to the CVC and the National Institute of Standards and Technology (NIST) simulations for different doping densities without using any QM corrections. The NCSU CVC code utilizes MB statistics while the NIST code uses full FD statistics. Differences between the calculations using the two different distribution functions are observed in both accumulation and inversion as expected. Importantly, CV ACE is in excellent agreement with both CVC (MB) and NIST (FD) except in the negative bias range for the NIST code, i.e., in accumulation for p-type and inversion for n-type silicon. This difference originates from the differing values of the valence band density of states used by the two different simulators; 1.2×10^{19} cm^{-3} in the NIST simulator and 1.8×10^{19} cm^{-3} in CV ACE. If the value of valence band density of states is set to 1.2×10^{19} cm^{-3} in CV ACE, it fits identically to the data simulated by the NIST simulator. So, for all doping densities simulated and over a wide range of EOTs (not shown), the CV ACE classical calculation is validated with other accepted codes for both types of distribution functions. From here on, the simulations and extractions for CV ACE use FD statistics.

B. Self-Consistent Schrödinger–Poisson Solver

To validate the UTD SP solver, we compare our SP solver to other available SP solvers. Fig. 2 shows the UTD SP solution compared to the same gate-stack simulated using a code from University of California Berkeley [30] and SCHRED [31]. The UTD program produces nearly identical C–V profiles to the UCB code. In inversion and depletion, SCHRED also matches the UTD SP closely but SCHRED C–V profiles have higher capacitance in accumulation compared to the UTD and UCB codes as it does not solve the Schrödinger equation in accumulation. As a result, in the accumulation region for both n- and p-type semiconductors, SCHRED shows classical C–V profiles. The slight difference between the solvers comes from the different values of silicon parameters used in the solvers. In this paper, the semiconductor parameter values are the same for both the QM simulations and classical simulations, which are given in Table I.

C. QM Correction Factor Extraction Using SP Solver

We extract the QM correction parameters used in (25), using a nonlinear least squares method fitting the corrected C–V simulation data to the full UTD SP solutions for a variety of gate stacks on the various semiconductors. There are 10 parameters to characterize the QM corrections in a material: a, σ, $\beta_{\mathrm{acc/inv},n/p}$, and $\gamma_{\mathrm{acc/inv},n/p}$ as already described in (26) and (27). However, σ has the same value (10^{10}) for all the semiconductors described in this paper and can therefore be considered a constant. These parameters for individual semiconductors are extracted by empirically fitting to the SP solver data.

In Figs. 3 and 4, the results of the QM corrected classical C–V simulations fit to the full SP solver calculations are shown for various semiconductors with a wide range of doping densities and oxide thicknesses. All the fits have

TABLE II
QM CORRECTION FACTORS FOR DIFFERENT SEMICONDUCTORS

	n-type				*p*-type				
	β_{inv} (eV.cm)	γ_{inv}	β_{acc} (eV.cm)	γ_{acc}	β_{inv} (eV.cm)	γ_{inv}	β_{acc} (eV.cm)	γ_{acc}	a ((V/cm)$^{4/3}$)
Silicon	-4.39×10^{-8}	0.64	4.60×10^{-8}	0.63	5.75×10^{-8}	0.62	-3.6×10^{-7}	0.65	2.38×10^{6}
Germanium	-5.02×10^{-8}	0.66	7.01×10^{-8}	0.60	4.23×10^{-8}	0.63	-6.44×10^{-8}	0.65	1.38×10^{5}
$Si_{0.5}Ge_{0.5}$	-3.81×10^{-8}	0.64	1.18×10^{-8}	0.57	1.89×10^{-8}	0.69	-8.57×10^{-8}	0.59	1.88×10^{6}
$Si_{0.6}Ge_{0.4}$	-4.04×10^{-8}	0.64	1.17×10^{-7}	0.57	1.99×10^{-8}	0.69	-8.95×10^{-8}	0.59	1.93×10^{6}
$Si_{0.75}Ge_{0.25}$	-4.39×10^{-8}	0.64	1.17×10^{-7}	0.58	1.72×10^{-8}	0.70	-1.18×10^{-7}	0.57	2.09×10^{6}
GaAs	-5.36×10^{-8}	0.63	9.15×10^{-8}	0.57	4.16×10^{-8}	0.63	-1.14×10^{-7}	0.58	3.52×10^{5}
$In_{0.2}Ga_{0.8}As$	-1.47×10^{-8}	0.76	1.57×10^{-7}	0.54	5.93×10^{-8}	0.60	-5.02×10^{-8}	0.67	1.22×10^{5}
$In_{0.53}Ga_{0.47}As$	-9.26×10^{-8}	0.60	3.15×10^{-8}	0.65	2.96×10^{-8}	0.65	-1.54×10^{-7}	0.56	4.81×10^{6}
$In_{0.70}Ga_{0.30}As$	-1.59×10^{-8}	0.70	3.11×10^{-7}	0.51	3.45×10^{-8}	0.67	-1.01×10^{-7}	0.56	3.82×10^{5}
InAs	-2.55×10^{-9}	0.92	1.28×10^{-8}	0.75	1.22×10^{-8}	0.76	-3.44×10^{-9}	0.90	3.47×10^{2}

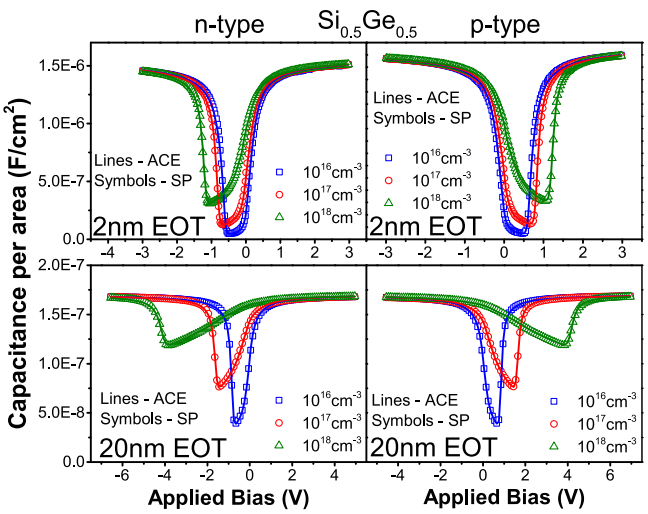

Fig. 3. Comparison between QM corrected ACE simulations (lines) with SP solution (open symbols) for n- and p-type $Si_{0.5}Ge_{0.5}$ with different doping densities and EOTs. ACE errors are less than 1%.

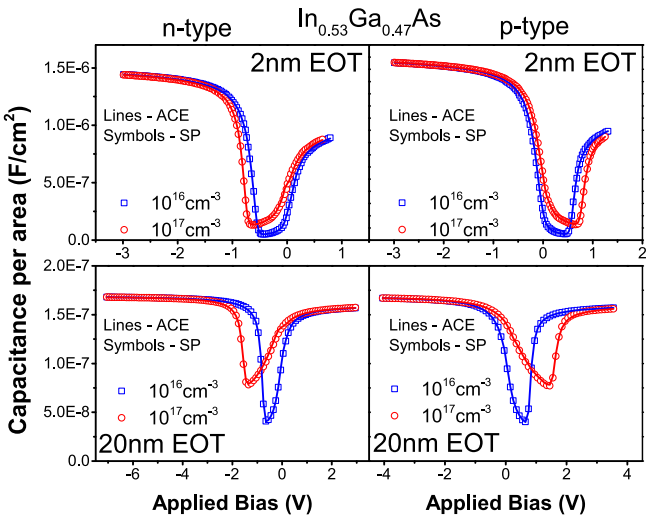

Fig. 4. Comparison between QM corrected ACE simulations (lines) with SP solution (open symbols) for n- and p-type $In_{0.53}Ga_{0.47}As$ with different doping densities and EOTs. ACE errors are less than 1%. The 2-nm simulations were truncated at positive biases since the QM corrections to the *X*- and *L*-valleys are not currently calculated.

a root-mean-squared (RMS) error of less than 1% and the extracted correction factors are given in Table II. As stated before, these fitting parameters are empirical parameters that do not have any real physical significance other than that they accurately capture the QM calculated capacitance. It can be seen from Figs. 3 and 4 that the correction factors for a specific semiconductor with a specific type of dopant, are valid over the full range of EOTs and doping densities of interest.

For III–V semiconductors (GaAs, $In_{0.2}Ga_{0.8}As$, and $In_{0.53}Ga_{0.47}As$), only the Γ-valley is used for extraction of the quantum correction parameters. For the *X*- and *L*-valleys, the energy gap and effective masses are different than those of the Γ-valley and a more complex model would be required for quantum correction. The SP simulations and our initial fits to them to extract the QM correction factors use a quasi-static (intrinsic) *C–V* with no D_{it} considered at all. For analysis and extraction from experimental data, we use the frequency-dependent small signal C_{it} response that incorporates multiple frequencies, where the inversion response is considered negligible, which is the same assumption made in NCSU CVC [9] for Si.

It should be noted that, when considering nonparabolicity of the conduction band in III–V semiconductors, ACE treats the nonparabolicity separately from the QM corrections. The validity of this approach was checked by comparing the ACE QM plus nonparabolic simulation to the SP solution in [34] that utilized nonparabolic bands in their self-consistent calculation (and accurately fits experimental *C–V* curves). The error between ACE (that combines the QM and NP separately) and [34] (that considers them simultaneously) is less than 2%. The error is much larger (∼15%) when ACE simulations are compared to the tight-binding simulation in [26]. We also note that in ACE, the user can input their own quantum corrections to the classical solution. Therefore, if the user has

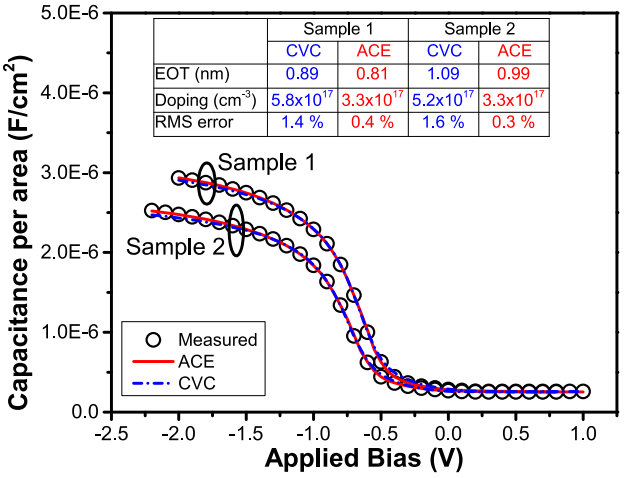

Fig. 5. Fits to two high-frequency Si experimental C–V curves with different dielectric thicknesses using ACE and CVC. Both models show excellent fits, although ACE shows lower fitting error compared to CVC for these samples. EOTs extracted using ACE are lower for both samples than the values extracted using CVC due to a more accurate benchmarking methodology.

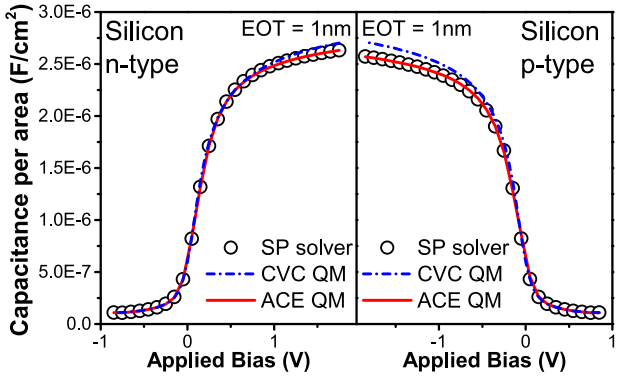

Fig. 6. Simulated C–V curves for n- and p-type Si with 10^{17} cm^{-3} doping and 1-nm EOT. ACE matches the SP data but CVC overestimates the capacitance in accumulation due to difference in benchmarking methodology.

a tight-binding model, for example, that they believe to be more accurate, that user can "map" the QM fitting parameters to it instead of using our SP solution fitting parameters.

IV. Comparison to Experimental C–V

ACE can be used to analyze C–V data from MOS devices based on a multitude of semiconductors. In part I of this paper, to show the viability of this quantum correction model, a couple of select silicon-based MOS devices are analyzed using ACE. In part II [33], MOS devices from alternative channel semiconductors (germanium and $In_xGa_{1-x}As$) will be analyzed in detail using ACE.

Two silicon samples were fabricated by our SEMATECH collaborators on p-type silicon with chemically grown SiO_2 and atomic layer deposition deposited HfO_2 with a metal gate. The measured high-frequency C–V profiles are analyzed in both CVC and ACE and the fits are shown in Fig. 5. From the fits, it can be seen that both ACE and CVC have very good fits to the experimental C–V profiles obtained from both samples. Comparing to the NCSU model, ACE actually has a better fit to the experimental data (<0.5% RMS error). In both cases, extracted EOTs using ACE are lower than the extracted EOTs using the NCSU model. This difference in extracted values originates from the fact that in CVC, the QM correction factors were obtained by mapping the model to experimental data, and hence, has an inherent uncertainty in the measured dielectric thickness. Conversely in ACE, the QM corrections are benchmarked to SP solver data, which is free from the uncertainty that exists in physical measurements. Fig. 6 shows the disparity between the simulated C–V profiles from CVC with QM corrections and from the SP solution, where CVC shows higher capacitance in accumulation compared to both the SP solver and ACE for a given EOT = 1 nm for both n- and p-type doping. From this difference it can be concluded that for a specific C–V profile, CVC would slightly overestimate the thickness of the dielectrics.

V. Conclusion

In conclusion, we have developed a new C–V simulation and extraction code to enable fast QM corrections to C–V data for a wide variety of semiconductors which accurately captures quantum effects in accumulation and inversion. We have benchmarked the model to full SP solutions, extracted the QM correction parameters, and showed that these correction parameters are valid for a wide range of EOTs and doping densities for both n- and p-type doping. We have developed a software package in C++ programming language called ACE to quickly and accurately simulate C–V profiles for various semiconductors using the developed model. In addition to forward modeling, ACE enables gate-stack parameter extraction capabilities from measured C–V data of fabricated MOSCAPs on Si, Ge, Si_xGe_{1-x}, and $In_xGa_{1-x}As$, among other semiconductors. The model includes nonparabolic bands, QM effects in strong accumulation and inversion, multitemperature and multifrequency measurements, and multiple valleys as appropriate.

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