Josephson Arbitrary Waveform Synthesis With Multilevel Pulse Biasing

Justus A. Brevik, Nathan E. Flowers-Jacobs, Anna E. Fox, Evan B. Golden, Paul D. Dresselhaus, and Samuel P. Benz, *Fellow, IEEE*

***Abstract*—We describe the implementation of new commercial pulse-bias electronics that have enabled an improvement in the generation of quantum-accurate waveforms both with and without low-frequency compensation biases. We have used these electronics to apply a multilevel pulse bias to the Josephson arbitrary waveform synthesizer and have generated, for the first time, a quantum-accurate bipolar sinusoidal waveform without the use of a low-frequency compensation bias current. This uncompensated 1 kHz waveform was synthesized with an rms amplitude of 325 mV and maintained its quantum accuracy over a 1.5 mA operating current range. The same technique and equipment was also used to synthesize a quantum-accurate 1 MHz sinusoid with a 1.2 mA operating margin. In addition, we have synthesized a compensated 1 kHz sinusoid with an rms amplitude of 1 V and a 2.7 mA operating margin.**

***Index Terms*—Digital-analog conversion, Josephson arrays, quantization, signal synthesis, standards, superconducting device measurements, superconducting integrated circuits, voltage measurement.**

I. Introduction

THE pulse-driven Josephson arbitrary waveform synthesizer (JAWS) has become an important instrument for ac voltage [1], [2] and impedance [3] metrology. Recent advances have allowed quantum-accurate audio-frequency waveforms to be synthesized at a record 2 V rms amplitude using this system [4]. Over the past 20 years, the primary challenge in optimizing the performance of the JAWS system has been to provide a stream of uniform bipolar current-bias pulses to all the dissipative superconducting Josephson junctions, which are distributed in series within multiple arrays. The high-speed pulses have been created by either binary [1] or ternary [5], [2] pattern generators, which have pulse density and other nonlinear performance limitations. Their multilevel signals have sometimes been combined with a continuous wave (CW) microwave signal [6] to improve pulse-bias uniformity and to excite the ternary pulse states of the junctions, namely quantized pulses of either polarity or no pulse (null state). Recent advances in high-speed RF arbitrary waveform generators (RF-AWG) have now made it possible to tailor pulse shapes consisting of many levels within the analog bandwidth of the RF-AWG. The use of multiple levels allows the construction of pulses that have zero average current, if integrated over the entire pulse duration, but enough peak instantaneous power to drive a flux quantum through the Josephson junction.

The JAWS system can achieve quantum accuracy only when each junction in an array pulses and passes a single flux quantum through its barrier for each current-bias pulse of the bitstream. In previous work [7], a finite impulse response (FIR) filter was used to shape pulses to compensate for the distortion of the transfer function and dispersion occurring between the generator and the Josephson array. However, this system relied on a two-level bitstream. In this work, the bias pulses are shaped using both a multilevel bias output and FIR filters to utilize the nonlinearity of the junctions in novel ways. Two different pulse-shaping methods were recently demonstrated in [6] and [8] that created pulse-bias sequences with zero average current and eliminated the need for compensation bias signals at the frequencies of interest. In particular, Zhou *et al*. [8] were able to generate positive flux quanta by adding negative pulses of half the amplitude immediately before and after each positive bias pulse to achieve zero average bias currents.

In this paper, we describe the synthesis of quantum-accurate waveforms through the delivery of a stream of multilevel high-speed pulses to the JAWS system using a new commercial 65 gigasamples-per-second (GSa/s) 8-bit AWG. We present three example waveforms that have unprecedented performance: a low-frequency compensated waveform, a low-frequency uncompensated waveform, and a high-frequency uncompensated waveform.

II. Low-Frequency Compensated Waveform Synthesis

The ac-coupled bipolar pulse-bias technique has been described in detail elsewhere [9]–[11]. Until recently, the best performance was achieved when the ternary quantized pulse states of the Josephson junctions were produced using a bias constructed from three separate signals for each array: a two-level digital bitstream, a CW microwave signal, and a low-frequency compensation bias current. The digital bitstream is nonreturn-to-zero clocked at twice the microwave frequency, and the maximum pulse repetition frequency is chosen to be on the order of the characteristic frequency of the Josephson junctions. The microwave and digital signals are combined such

Manuscript received November 22, 2016; revised January 23, 2017; accepted January 24, 2017. Date of publication February 1, 2017; date of current version March 9, 2017. This paper was recommended by Associate Editor O. Mukhanov.

The authors are with the National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: justus.brevik@nist.gov).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TASC.2017.2662708

that two sequential bits, over a single CW period, excite one of three junction states, $n = 0, -1, or +1$, which represent the number of integer flux quanta passing through each junction for each CW period. This combined high-frequency signal is ac coupled to the arrays using inner/outer dc blocks that have a typical high-pass cutoff frequency of 150 MHz. This removes common-mode signals at the synthesis frequency from the termination resistors, allowing multiple arrays to be connected in series. However, this filtering method also attenuates the low-frequency fundamental in the high-speed pulse signal and produces an undesirable time-dependent offset in the pulse-bias signal at the array. For large amplitude waveforms, where the pulse density exceeds about 5%, the offset is so great that the junctions do not correctly pulse in correspondence with the bias. In order to eliminate the offset and to properly synthesize large-amplitude voltage waveforms that have robust operating margins (with respect to the largest range of bias amplitudes), a corresponding low-frequency compensation signal at the synthesis frequency must be reapplied to the arrays through dedicated current bias leads.

III. Pulse-Bias Circuits

At the National Institute of Standards and Technology (NIST), the ABG-2 custom bitstream generator was developed to fulfill the need for a ternary pulse pattern generator capable of synthesizing waveforms with a robust operating margin [6]. Recently, a commercial instrument has become available that can achieve comparable performance in biasing Josephson arrays as the ABG-2. The Keysight M8195A[1] is a 65 GSa/s RF-AWG with built-in FIR filters and 8 bits of resolution for each output channel [12]. This high output resolution allows a natural implementation of custom pulse shapes that can be optimized to bias the junction arrays. As explained in detail in [7], the integrated FIR filters can be used to partially compensate for nonlinearities in the output stages and amplifiers, and for bandwidth limitations in the microwave path, thereby significantly improving performance of the JAWS system.

The room-temperature electronics used in this experiment included a two-channel RF-AWG, two microwave amplifiers, a two-channel low-frequency AWG, a custom four-channel differential amplifier module for biasing the arrays, and a low-distortion digitizer for measuring the synthesized waveforms. The 1 V peak-to-peak output amplitude of the RF-AWG channels was insufficient to bias the junction arrays. Therefore, the amplitude of each of the pulse-bias outputs was increased by an amplifier that had a maximum 7.5 V peak-to-peak output amplitude, useable bandwidth up to 50 GHz, and an adjustable eye-crossing level. A single source was used to apply the low-frequency compensation and the dither biases to all four arrays. In previous experiments, these biases were provided by two current bias outputs on the ABG-2, but for this experiment a commercial two-channel AWG was used. One channel provided the low-frequency compensation current bias and allowed for high-precision adjustment of the voltage and phase of the compensation waveform. The other AWG channel provided a triangle-wave current signal, at a frequency around 100 times lower than the synthesis frequency, to measure the operating margin. The two AWG outputs were combined using a custom isolation amplifier and divided among the four junction arrays. This stage was necessary to maintain the electrical isolation between the low-frequency biases to each array. The compensation and dither gains were adjusted for each array in the amplifier, but a common phase was used for all four arrays.

In this experiment, we used chips that include the improvements to the JAWS circuit described in [13]. Namely, this circuit design includes a pair of on-chip Wilkinson power dividers that split two high-frequency pulse signals among four junction arrays [14], [15]. The dividers have a designed center frequency of 26 GHz and useful bandwidth up to 35 GHz. The design also includes on-chip inner/outer dc blocks to maintain electrical isolation between arrays, so that their output voltages can be summed in series. The blocks are located between the dividers and arrays, and high-pass filter the pulse-bias signal with a 3 dB cutoff around 150 MHz. This circuit also includes an array design that uses 4270 Josephson junction stacks, each stack containing three self-shunted junctions, for a total of 12 810 junctions per array. Each array has a pair of on-chip voltage and current taps, with integrated low-pass filters that decouple the high-frequency signals from the bias lines. The independent current leads allow an optimized low-frequency compensation bias to be applied to each array, as explained above. The voltage outputs of the arrays are connected in series using on-chip superconducting leads.

The combined voltage output of the arrays was measured with a National Instruments 5922A[1] digitizer. The RF-AWG, low-frequency AWG, and digitizer all shared a common 10 MHz reference clock. This reference maintained synchronization between the optimized phase of the low-frequency compensation bias, the pulse playback of the RF-AWG, and the recording of the waveform by the digitizer. The pulse-bias experiments were performed by installing the chip in a cryogenic probe, which was cooled to 4 K in a Dewar of liquid helium. The junctions in the arrays of this chip had a nominal critical current (I_c) of 11 mA and 3 mΩ resistance (R).

IV. 1 Volt Compensated Synthesis

A compensated 1 kHz sinusoid, with an rms amplitude of 1 V and an operating current margin of 2.8 mA, was recently demonstrated using the NIST JAWS system, with the chip cooled in liquid helium [13]. By combining the output voltages of two such 1 V circuits installed in a cryocooler, a record rms amplitude of 2 V and a 1.6 mA operating margin was also demonstrated. As in that reference, the operating margins in this paper were determined from the dc bias current range over which the total harmonic distortion in the output spectra was independent of current bias.

We have demonstrated the functionality of the new pulse-bias electronics by synthesizing a 1 kHz sinusoid, with an rms

[1]Commercial instruments are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified is necessarily the best available for the purpose.

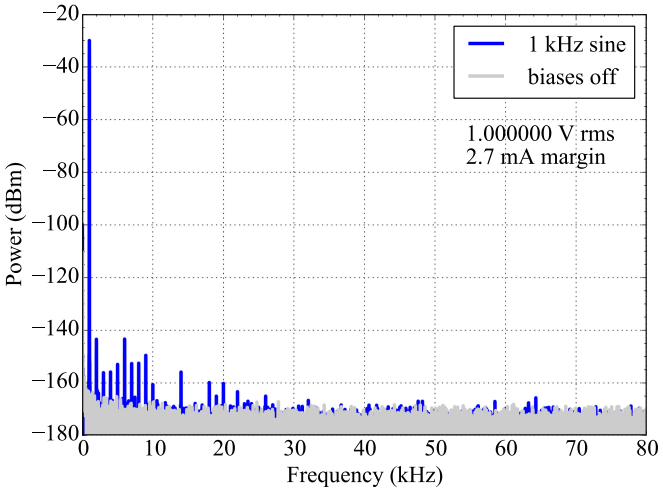

Fig. 1. Digitally-sampled spectral measurement of the 1 kHz, 1 V rms sinusoid synthesized with all four arrays of the JAWS chip with a compensation bias. The digitizer was set to 1 MΩ input impedance, +/−5 V input range, and 1 megasample-per-second (MSa/s) sampling rate. The spectra were calculated with 10 Hz resolution bandwidth and no averaging. The blue data show the synthesized sinusoid. The gray data were acquired with the bias signals turned OFF, to show the digitizer noise floor at −141 dBc and the spurious signals.

amplitude of 1 V, using a compensation current bias. This waveform maintained its quantum accuracy over a 2.7 mA operating range. Fig. 1 shows the spectrum of the 1 kHz sinusoid where the largest harmonic, at 2 kHz, is −115 dBc (decibels relative to the fundamental [carrier]). All the measured harmonics have been attributed to the nonlinear response of the digitizer, as explained in previous work [16].

For this experiment, the RF-AWG was set to two-channel mode with the sample rate divided by two, which provided 32 FIR filter coefficients. To directly compare the performance of the RF-AWG to previous measurements, its output sampling rate was set to the typical 28.8 GHz used by the ABG-2. The operating margin was optimized by an automated procedure that iteratively tuned the output amplitude of the RF-AWG, the eye-crossing level of the amplifiers, the phase and amplitude of the compensation bias, and finally, the 32 filter coefficients. The coefficients were serially tuned, beginning with the outermost taps and converging on the innermost taps, by adjusting the coefficient of each tap to maximize the margin before moving on to the next tap.

The 2.7 mA operating margin obtained for this waveform and chip is comparable to the 2.8 mA margin obtained in [13]. We note that the maximum $n = 1$ constant voltage step for the combined arrays, which was obtained during CW microwave testing of this chip, was substantially smaller than the step measured for the arrays in [13]. Thus, we suspect that an improvement in the step size utilization has been achieved with the new pulse-bias electronics over the previous ABG-2 electronics. Two different chips were used in the two experiments, but both were performed in liquid helium using four-array chips that had an identical circuit design, with the improvements described above. In addition, FIR filters were used in both experiments to modify the pulse bias to optimize the operating margin.

V. Zero-Compensation Synthesis

Current biasing of junction arrays generates an undesired voltage signal by driving the distributed inductance of the arrays. This error signal is described by the equation $V_L = I\omega L$, where V_L is the out-of-phase voltage component, I is the total current through the array at the radial frequency ω of the fundamental signal, and L is the inductance of the array. The inductive voltage error adds in quadrature to the desired output voltage and its amplitude scales linearly with the frequency of the synthesized waveform. The total inductive voltage error is the vector sum of the above error, produced by the compensation bias, and the error produced by any remaining low-frequency components of the pulse bias (both in the code and that produced by the output drivers) that remain after being attenuated by the dc blocks. Alternative "zero-compensation" bias methods have been developed to reduce this error. These methods are critical for the synthesis of useful calibration waveforms at frequencies above 10 kHz.

In order to produce robust quantized output states and accurate voltages without a low-frequency compensation signal, the low-frequency components in the digital code must be substantially reduced. Reduction of the fundamental in the pulse-bias signal is accomplished by pairing each current pulse that excites a junction pulse with an adjacent cancelation pulse or pulses, so that the instantaneous time-average of each pulse bias block is zero. These cancelation pulses are of the opposite sign and have sufficient amplitude to null the mean amplitude of the pulse bias block, but have low enough amplitude so as not to excite junction pulses of the opposite polarity. Thus, the dc blocks no longer induce a time-dependent offset in the pulse bias at the arrays, since there is substantially less low-frequency signal to be removed, and it is no longer necessary to apply a compensation bias to the arrays. Two zero-compensation bias techniques have already been demonstrated in [6] and [8]. However, these existing methods are limited to creating unipolar waveforms that contain an inherent and undesirable dc offset, as well as output amplitudes that are limited to one-fourth and one-third, respectively, of the full-scale amplitude obtainable through bipolar compensated synthesis at the same pulse sampling rate.

The first zero-compensation method was developed for use with the ABG-2 [6]. Two consecutive bits of a two-level digital signal, [+1,−1] or [−1,+1], are combined with a single period of a CW microwave bias to create pulse blocks that each have a zero average, as shown in Fig. 2(a). A small positive dc current bias is then applied so that each [+1,−1] block excites the +1 state and generates a positive output junction pulse, while each [−1,+1] block remains in the 0 state and does not generate a negative junction pulse.

This implementation of zero-compensation bias has several limitations. It requires an additional dc bias to be applied to each array and it creates only unipolar waveforms, since only the $n = 0$ and +1 quantized states are produced. Furthermore, due to the details of the bit sequence, the pulse density cannot exceed 50%. Therefore, waveform amplitudes are limited to 25% of the full-scale amplitude obtained with compensated bipolar synthesis. The output also has an undesirable dc offset

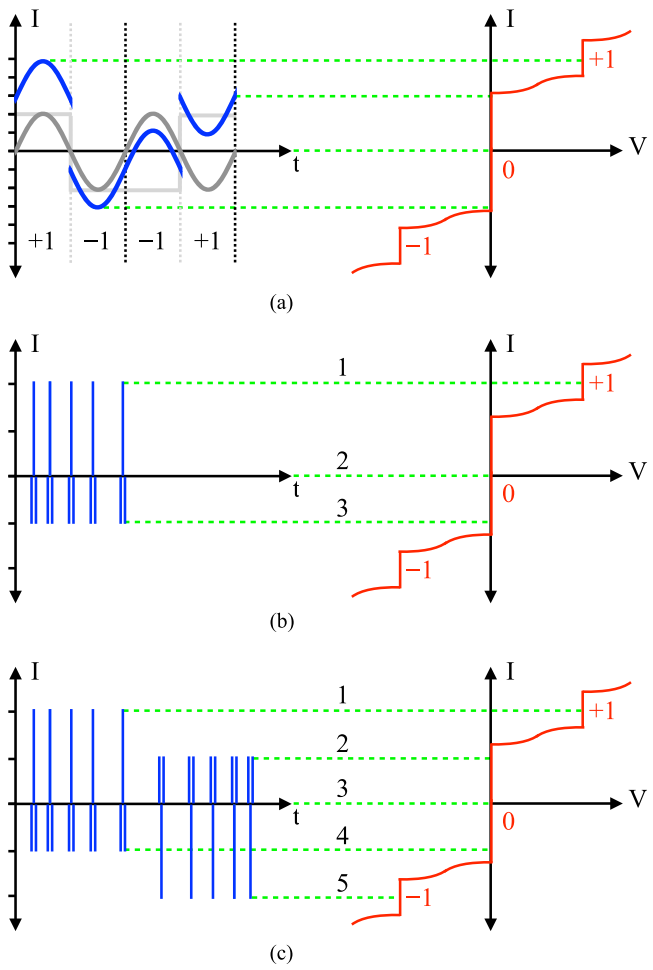

Fig. 2. Simplified diagram of three zero-compensation bias methods. (a) The unipolar zero-compensation method presented in [6], which creates zero-average pulse blocks by combining 2 bits of a two-level digital code, [+1,−1] or [−1,+1], (light solid gray, square lines) with a single period of a CW microwave bias (dark solid gray, sinusoid). When combined with a dc offset (blue solid) these blocks excite the +1 and 0 states, respectively. (b) The unipolar zero-compensation method presented in [8], which uses a three-level digital code and pairs each quantized bias pulse ($n = 1$) with bracketing half-amplitude cancelation pulses. (c) The new bipolar zero-compensation method described in this paper, which produces the $n = 0$, +1, and −1 quantized states using a five-level digital code and both polarities of bracketing cancelation pulses.

that must be canceled by combining identical junction arrays in series, each driven by different pulse sequences that produce identical in-phase waveforms, but with opposite dc offset voltages. To date, a sinusoid with an rms output amplitude of 128 mV and a 1 mA operating margin has been demonstrated using this technique [16].

The second zero-compensation method was developed to eliminate the need for an additional dc bias current by using a ternary pulse pattern generator [8]. The ternary generator allows the main bias pulses, which generate quantized junction pulses, and their accompanying cancelation pulses to be independently adjusted. It also eliminates the need for a synchronized CW bias signal. A three-level delta-sigma modulated pattern is created and each +1 bias pulse is replaced by a block of three pulses [−0.5,+1,−0.5], such that the average of each pulse block is zero, as shown in Fig. 2(b). The magnitude of the +1 bias pulses is adjusted so that each of them generates a single positive output junction pulse. The −0.5 pulse magnitude is adjusted to ensure that the cancelation pulses do not generate negative junction pulses, yet they properly average the mean amplitude of each pulse block to zero.

Although this method eliminates the need to inject a dc current bias, it still produces strictly unipolar waveforms with half-scale amplitude and a dc offset voltage. Additionally, the maximum pulse density of the bitstream is limited to two-thirds to allow the insertion of two half-amplitude cancelation pulses between adjacent excitation pulses. Thus, waveforms are limited to one-third of full scale using this technique. An 8 kHz sinusoid with a 1 mV rms amplitude was demonstrated using this method, with no report of the operating margin [8].

The 8-bit output resolution of the RF-AWG readily enables the extension of the second zero-compensation method from a three-level pulse pattern, which results in unipolar waveforms, to a five-level pattern capable of generating bipolar waveforms. This method has the immediate advantages that it doubles the waveform amplitude and eliminates the output voltage offset, yet it still obviates the requirement for an additional dc bias current. We implemented bipolar zero-compensation by first generating a three-level digital code with a delta-sigma modulation algorithm. The individual +1 and −1 bias pulses were then replaced by three-pulse, zero-average signal blocks of the form [−0.5,+1,−0.5] or [+0.5,−1,+0.5], as shown in Fig. 2(c). As in the second zero-compensation method, the maximum pulse density is limited to two-thirds to accommodate the cancelation pulses. However, since the waveforms are bipolar, this zero-compensation method can theoretically produce output amplitudes that are up to two-thirds of full scale, which is double the maximum amplitude of the second, unipolar, zero-compensation method.

Using this new bipolar zero-compensation technique, we have synthesized a 1 kHz sinusoid with an rms amplitude of 325 mV, while achieving a 1.5 mA operating margin. The measured spectrum of the sinusoid is shown in Fig. 3, where the harmonics are no more than −114 dBc and are again due to the digitizer nonlinearity. This experiment was performed in liquid helium with the same four-array chip that was used in the compensated synthesis. We used a pulse code with a maximum pulse density that was 32.5% of the code used to obtain 1 V rms with four arrays, thereby obtaining an rms amplitude of 325 mV. The operating margin was optimized in the same manner that was described above, by tuning the RF-AWG output amplitude, the amplifier eye-crossing level, and the FIR filter coefficients.

We have found that as we increase the waveform amplitude and pulse density, the operating margin decreases to zero. So far, the highest pulse density that we have achieved, while still obtaining an operating margin greater than 1 mA, is around one-third of the 1 V pulse density. We have not yet reached the theoretical two-thirds maximum pulse density limit. The likely reason is that the zero-compensation codes contain more power at higher frequency than the compensated codes, due to the increased repetition rate of the cancelation pulses. As the maximum pulse density increases, the signal power is shifted to higher frequency. The bandwidth of the pulse code is limited by the microwave path to the chip, which includes the amplifier, cabling, and the on-chip Wilkinson dividers. As discussed in

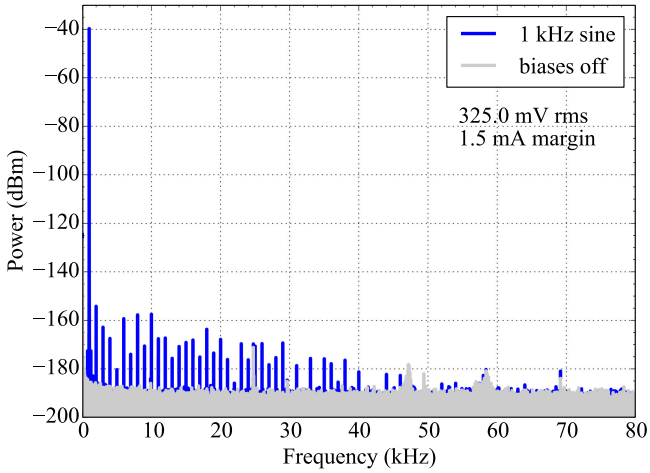

Fig. 3. Digitally-sampled spectral measurement of the 1 kHz, 325 mV rms sinusoid synthesized with all four arrays of the JAWS using the bipolar zero-compensation bias method. The digitizer was set to 1 MΩ input impedance, +/−1 V input range, and 200 kilosamples-per-second sampling rate. The spectra were calculated with a 1 Hz resolution bandwidth and no averaging. The blue data show the synthesized sinusoid. The gray data were acquired with the bias signals turned OFF, and show the digitizer noise floor at −150 dBc and the spurious signals.

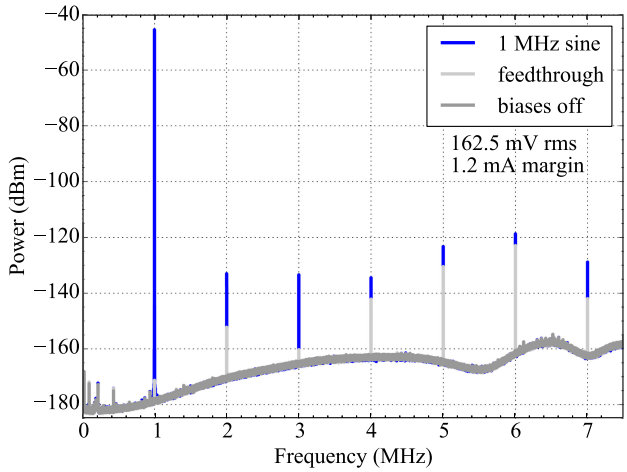

Fig. 4. Digitally-sampled spectral measurement of the 1 MHz, 162.5 mV rms sinusoid synthesized with two arrays of the JAWS using the bipolar zero-compensation bias method. The digitizer was set to 1 MΩ input impedance, +/−1 V input range, and 15 MSa/s sampling rate. The spectra were calculated with 50 Hz resolution bandwidth and 100 averages. The blue data show the synthesized sinusoid, the light gray data show the inductive voltage signal from the residual feedthrough signal, and the dark gray data show the digitizer noise floor.

[7], an FIR filter in the high-frequency bias path can partially compensate for some of the bandwidth limitations by increasing power at higher frequencies. Despite the benefit of the FIR filters, the high-frequency information in the zero-compensation signal is still being degraded, particularly by the dividers. We have an on-going effort to improve the bandwidth of the signal path to obtain higher amplitude bipolar zero-compensation waveforms.

VI. High-Frequency Zero-Compensation

Generating waveforms without compensation bias is critical for calibration applications that use signal frequencies over 10 kHz. As described previously, the amplitude of the inductive voltage error scales linearly with the frequency of the synthesized waveform. At 1 kHz, the magnitude of the inductive error signal is about 1 part in 10^6 of the desired output signal. However, the signals add in quadrature, which results in a magnitude error that is usually less than 1 part in 10^8 [4]. To demonstrate the effectiveness of this new zero-compensation method, we synthesized a 1 MHz sinusoid with an rms amplitude of 162.5 mV and achieved a 1.2 mA operating margin, using only two arrays. We then measured the inductive error signal produced by the residual feedthrough signal.

To perform the measurements, a series of 250 MHz inner-only dc blocks was added to the microwave transmission line at the input to the cryoprobe to increase the attenuation of the fundamental in the pulse code. A single 500 MHz inner/outer block was also added to prevent coupling of high-frequency signals from the RF-AWG to the array. This experiment was performed with a new 1 MHz code that had the same 32.5% maximum pulse density as before, but with only two of the arrays in the JAWS circuit, thereby yielding a 162.5 mV rms amplitude.

After synthesizing the 1 MHz sinusoid, we measured the error caused by the remaining "feedthrough" voltage signal by adding a 6 dB attenuator to the dc blocks at the cryoprobe. This linearly reduced the output power of the pulse code to the array and prevented pulsing of the junctions, but still allowed a measurement of the inductive error from the residual unblocked fundamental in the code. We also measured the signal with the RF-AWG turned OFF to measure the noise floor of the digitizer.

Fig. 4 shows the measured spectra of the 1 MHz sinusoid and feedthrough signal, and the noise floor. The second harmonic of the 1 MHz tone was −88 dBc and was caused by the digitizer, which is more nonlinear and produces more distortion at 1 MHz than at 1 kHz. A small inductive feedthrough signal at 1 MHz was detected −120 dB relative to the 1 MHz tone, after accounting for the 6 dB of attenuation required to prevent the junctions from pulsing. Thus, at 1 MHz the inductive error signal added no more than 1 part in 10^6 vectorially to the output signal, although we did not measure the phase relative to the fundamental. The feedthrough spectrum shows detectable higher-order harmonics, with the second harmonic at −107 dBc below the 1 MHz tone. The origin of these harmonics has not been identified and is under further investigation, but they will not significantly contribute to the rms output voltage. Using this zero-compensation technique, the stray capacitive signal and transfer function of the voltage output leads will become much more important than the parasitic inductive error voltage. This is the first 1 MHz signal to be synthesized that has the potential for practical RF calibration applications, since all the bias-related systematic errors are less than 1 part in 10^6. This systematic error contribution will be further investigated in future research efforts.

VII. Conclusion

A new commercially-available high-resolution RF-AWG has enabled us to implement a five-level digital code and synthesize

the first bipolar uncompensated waveform. This waveform was synthesized with a record rms amplitude of 325 mV at 1 kHz, and had an operating range of 1.5 mA. Furthermore, a 1 MHz sinusoid was synthesized with an rms amplitude of 162.5 mV over a 1.2 mA operating margin. Using our newly-implemented bipolar zero-compensation method we detected an inductive error signal of only 1 part in 10^6, demonstrating that the technique and pulse-bias electronics are capable of significantly reducing errors generated by the pulse and compensation bias signals.

The RF-AWG was also demonstrated for compensated waveform synthesis through the generation of a sinusoid with a 1 V rms amplitude and a 2.7 mA operating margin. The compensated synthesis has demonstrated a likely improvement in the utilization of the maximum quantized voltages of the junction arrays, and hence operating margin, over the existing custom ABG-2 pulse-bias electronics.

The 8-bit output resolution and user-defined FIR filters provide the level of control and adjustment needed to optimize the uniformity of the pulse bias to achieve quantum states with larger operating margins in Josephson junction arrays. We anticipate further improvements in the performance of synthesized waveforms by implementing more advanced JAWS circuits and through the implementation of custom patterns with the new pulse-bias electronics.

ACKNOWLEDGMENT

The authors would like to thank S. Waltman for the development of the custom isolation amplifier used in these experiments, J. Underwood for technical discussions, and the National Institute of Standards and Technology Boulder Microfabrication Facility for fabrication expertise. This work is a contribution of the U.S. government and is not subject to U.S. copyright.

REFERENCES

[1] S. P. Benz and C. A. Hamilton, "A pulse-driven programmable Josephson voltage standard," *Appl. Phys. Lett.*, vol. 68, pp. 3171–3173, May 1996.

[2] O. F. Kieler, R. Behr, R. Wendisch, S. Bauer, L. Palafox, and J. Kohlmann, "Towards a 1 V Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Jun. 2015, Art. no. 1400305.

[3] F. Overney *et al.*, "Josephson-based full digital bridge for high-accuracy impedance comparisons," *Metrologia*, vol. 53, no. 4, pp. 1045–1053, Jun. 2016.

[4] N. E. Flowers-Jacobs, A. Rüfenacht, A. E. Fox, P. D. Dresselhaus, and S. P. Benz, "2 Volt pulse-driven Josephson arbitrary waveform synthesizer," in *Proc. Conf. Precis. Electromagn. Meas.*, Ottawa, Canada, 2016, pp. 1–2.

[5] E. Houtzager, S. P. Benz, and H. E. van den Brom, "Operating margins for a pulse-driven Josephson arbitrary waveform synthesizer using a ternary bit-stream generator," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 4, pp. 775–780, Apr. 2009.

[6] S. P. Benz and S. B. Waltman, "Pulse-bias electronics and techniques for a Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 23, no. 6, Dec. 2014, Art. no. 1400107.

[7] N. E. Flowers-Jacobs, S. B. Waltman, A. E. Fox, P. D. Dresselhaus, and S. P. Benz, "Josephson arbitrary waveform synthesizer with two layers of Wilkinson dividers and an FIR filter," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 6, Sep. 2016, Art. no. 1400307.

[8] K. Zhou, J. Qu, and S. P. Benz, "Zero-compensation method and reduced inductive voltage error for the AC Josephson voltage standard," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 5, Oct. 2015, Art. no. 1400806.

[9] S. P. Benz, C. A. Hamilton, C. J. Burroughs, and T. E. Harvey, "AC and DC bipolar voltage source using quantized pulses," *IEEE Trans. Appl. Instrum. Meas.*, vol. 48, no. 2, pp. 266–269, Apr. 1999.

[10] S. P. Benz, C. J. Burroughs, T. E. Harvey, and C. A. Hamilton, "Operating conditions for a pulse-quantized ac and dc bipolar voltage source," *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 3306–3309, Jun. 1999.

[11] S. P. Benz, C. J. Burroughs, and P. D. Dresselhaus, "AC coupling technique for Josephson waveform synthesis," *IEEE Trans. Appl. Supercond.*, vol. 11, no. 1, pp. 612–616, Mar. 2001.

[12] "Keysight M8195A arbitrary waveform generator revision 2," Keysight Technologies Deutschland GmbH, Böblingen, Germany, Jul. 2016.

[13] N. E. Flowers-Jacobs, A. E. Fox, P. D. Dresselhaus, R. E. Schwall, and S. P. Benz, "Two-volt Josephson arbitrary waveform synthesizer using Wilkinson dividers," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 6, Sep. 2016, Art. no. 1400207.

[14] M. M. Elsbury, P. D. Dresselhaus, N. F. Bergren, C. J. Burroughs, S. P. Benz, and Z. Popovic, "Broadband lumped-element integrated N-Way power dividers for voltage standards," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 8, pp. 2055–2063, Aug. 2009.

[15] M. M. Elsbury, "Broadband microwave integrated circuits for voltage standard applications," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. Colorado Boulder, Boulder, CO, USA, 2010.

[16] S. P. Benz *et al.*, "One-Volt Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 1, Feb. 2015, Art. no. 1300108.

Justus A. Brevik received the B.S. degree in physics from the University of Washington, Seattle, WA, USA, in 2002, and the Ph.D. degree in physics from the California Institute of Technology, Pasadena, CA, USA, in 2012, for his work on the measurement of cosmic microwave background polarization using the BICEP2 telescope.

He joined the National Institute of Standards and Technology (NIST) Boulder, CO, USA, as a National Research Council Fellow in 2012, where he worked on transition edge sensor detectors and the microwave superconducting quantum interference device multiplexer for astrophysics applications. In 2014, he joined a startup company attempting to launch thermal rockets into space using beamed microwave power generated by gyrotrons. He returned to NIST-Boulder in 2015 to work in the Quantum Voltage Project, where he is developing a Josephson arbitrary waveform synthesizer capable of creating quantum-accurate waveforms in the gigahertz regime for telecommunications and quantum information applications.

Nathan Edward Flowers-Jacobs was born in Urbana, IL, USA, on June 15, 1979. He received the B.S. degree in physics from the California Institute of Technology, Pasadena, CA, USA, in 2001, and the Ph.D. degree in physics from the University of Colorado Boulder, Boulder, CO, USA, in 2010, for his work on a quantum-limited detector of nanomechanical motion based on electron tunneling across an atomic point contact.

He was with Massachusetts Institute of Technology Lincoln Laboratory, modeling radar cross sections for two years, before joining the Graduate School at JILA and the University of Colorado Boulder. From 2010 to 2014, he was a Postdoctoral Associate with Yale University, New Haven, CT, USA, working on nanomechanical displacement measurements at the quantum limit using optical cavities. In 2014, he joined the Quantum Voltage Project, National Institute of Standards and Technology, Boulder, CO, USA, where he has been working on development, characterization, and applications of the Josephson arbitrary waveform synthesizer, which is an ac Josephson voltage standard based on pulse-biased arrays of Josephson junctions.

Anna E. Fox received the Ph.D. degree in electrical engineering from Drexel University, Philadelphia, PA, USA, in 2009.

From 2009 to 2010, she was a National Research Council Postdoctoral Researcher with the Optoelectronics Division, National Institute of Standards and Technology (NIST), Boulder, CO, USA, fabricating superconducting transition-edge sensors (TES) for use at optical wavelengths. She continued her work in TES fabrication with the NIST Quantum Sensors Project, where she fabricated arrays of TES bolometers for cosmic microwave background detection. Since 2013, she has been with the NIST Quantum Voltage Project, working toward the design and fabrication of voltage standard devices, such as the programmable Josephson voltage standard and the ac Josephson voltage standard.

Dr. Fox received the 2016 IEEE Council on Superconductivity Van Duzer Prize.

Evan B. Golden was born in Boston, MA, USA, on March 31, 1993. He recently received the B.S. degree in engineering physics with a focus on electrical engineering from the University of Colorado Boulder, Boulder, CO, USA.

In 2016, he joined the Quantum Voltage Project at the National Institute of Standards and Technology (NIST), Boulder, CO, USA, as a Professional Research Experience Program Undergraduate. He has been working on the testing and measurement of Josephson voltage standard devices.

Paul D. Dresselhaus was born in Arlington, MA, USA, on January 5, 1963. He received the B.S. degree in physics and electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1985, and the Ph.D. degree in applied physics from Yale University, New Haven, CT, USA, in 1991.

In 1999, he joined the Quantum Voltage Project, the National Institute of Standards and Technology, Boulder, CO, USA, where he has been developing novel superconducting circuits and broadband bias electronics for precision voltage waveform synthesis and programmable voltage standard systems. He was with Northrop Grumman for three years, where he designed and tested numerous gigahertz-speed superconductive circuits, including code generators and analog-to-digital converters. He also upgraded the simulation and layout capabilities at Northrop Grumman to be among the world's best. He has also been a Postdoctoral Assistant at The State University of New York, Stony Brook, NY, USA, where he worked on the nanolithographic fabrication and study of Nb–AlO_x–Nb junctions for single-electron and single- flux-quantum applications, single-electron transistors and arrays in Al–AlO_x tunnel junctions, and the properties of ultrasmall Josephson junctions. Since 2015, he has been the Project Leader of the Quantum Voltage Project, NIST.

Dr. Dresselhaus received two U.S. Department of Commerce Gold Medals for Distinguished Achievement and the IEEE Council on Superconductivity Van Duzer Prize in both 2006 and 2016.

Samuel P. Benz (M'01–SM'01–F'10) was born in Dubuque, IA, USA, on December 4, 1962. He received the B.A. (*summa cum laude*) degree in physics and math from Luther College, Decorah, IA, USA, in 1985, and the M.A. and Ph.D. degrees in physics from Harvard University, Cambridge, MA, USA, in 1987 and 1990, respectively. He received the R. J. McElroy Fellowship during 1985–1988 for the Ph.D. degree.

In 1990, he joined the National Institute of Standards and Technology (NIST), Boulder, CO, USA, as an NIST/National Research Council Postdoctoral Fellow and became a permanent Staff Member in January 1992. He has been the Project Leader of the Quantum Voltage Project, NIST, since October 1999, and Group Leader of the Superconductive Electronics Group since 2015. He has worked on a broad range of topics within the field of superconducting electronics, including Josephson junction array oscillators, single-flux-quantum logic, ac and dc Josephson voltage standards, Josephson waveform synthesis, and noise thermometry. He has more than 220 publications, and he is the holder of three patents in the field of superconducting electronics.

Dr. Benz is a Fellow of the NIST and the American Physical Society. He is a member of Phi Beta Kappa and Sigma Pi Sigma. He received three U.S. Department of Commerce Gold Medals for Distinguished Achievement, the 2016 IEEE Joseph F. Keithley Award, and the IEEE Council on Superconductivity Van Duzer Prize in both 2006 and 2016.