Chapter 10

Measurement of active nanoelectronic devices

10.1 Applications of radio frequency nanoelectronics

The preceding chapters have described a variety of measurement methods for the characterization of radio frequency (RF) nanoelectronics. For example, we have described how on-wafer measurement and de-embedding techniques can be extended to devices and circuits that incorporate nanoscale building blocks. We went on to discuss how local microwave microscopy techniques enable us to characterize defects, interfaces, and the constituent materials inside a device. Taken together, this suite of techniques provides a comprehensive picture that relates overall device performance to intradevice circuit and material parameters. In a nanoelectronic world in which the placement of each individual atom can impact device performance, this capability has potentially powerful implications for RF nanoelectronic design, fabrication, and operation. However, the full impact of these measurement techniques will only be realized when they are applied to state-of-the-art technological challenges, both within the field of nanoelectronics and beyond. To that end, the final five chapters of this book are dedicated to application of the measurement techniques that we have introduced. These chapters not only demonstrate the relevance of these methods to contemporary research and engineering, but also serve as practical examples of how the general RF and microwave measurement techniques can be adapted and extended to specific measurement problems.

Many of the most promising applications of nanomaterials involve active, nanoelectronic devices. For example, the intrinsic transport properties of single-walled, carbon nanotubes (CNTs) enable field effect transistors (FETs) that allow higher current densities and lower distortion than their conventional counterparts [1]. In addition, CNTFETs offer the tantalizing possibility of field effect transistors (FETs) with cutoff frequencies in the terahertz range, at least in theory. Given that a typical, 100 nm-long CNT has a capacitance on the order of $C = 4$ aF and a quantized resistance as small as $R = 6.25$ kΩ, a rough calculation of the RC time constant of such a nanotube is on the order of 160 fs, corresponding to a frequency of about 6 THz [2]. Early measurements of the transconductance in CNT transistors also suggested potential cutoff frequencies well into the terahertz regime [3]. However, in practice, the extrinsic cutoff frequencies of realizable CNTFETs have been on the order of tens of gigahertz [4]-[6]. The realization of CNTFETs with terahertz-scale, extrinsic cutoff frequencies faces significant, potentially insurmountable challenges. For instance, materials-science challenges include the isolation of large numbers of uniform, semiconducting CNTs. Also, while the intrinsic properties of CNTs favor high cutoff frequencies, optimization of the extrinsic cutoff frequency requires minimization of contact reactance and other parasitics. These fabrication challenges are also intimately tied to the need for impedance matching. Moreover, quantum mechanical effects such as kinetic inductance and quantum capacitance can play significant roles in device performance, depending upon the intended application and desired operating frequency [2], [7]. Ultimately, the cutoff frequencies of CNTFETs appear unlikely to surpass those of less expensive,

conventional FETs. However, the unique properties of CNTs may yet be leveraged for specialized applications such as high-linearity amplifiers and mixers [1].

Building upon efforts to produce CNT-based, RF nanotransistors, the field of carbon-based nanoelectronics has naturally extended to include graphene-based, RF nanotransistors. In fact, following the experimental demonstration of ambipolar field effects and high electron mobility in graphene [8], [9], significant progress has been made in the fabrication and optimization of graphene-based FETs. Notably, graphene is not a natural choice for transistor applications as it lacks a band gap, though a band gap may be opened by patterning a graphene sheet into nanoribbons. The lack of a band gap makes it difficult to achieve a high on/off ratio with graphene nanotransistors, thus limiting their effectiveness as switches. As in the case of CNTFETs, extrinsic cutoff frequencies of graphene FETs have reached, but not exceeded tens of gigahertz [10], [11]. Recent advances in graphene transistor technology include the engineering of FETs based heterostructures such as graphene-boron nitride [12] and graphene-fluorographene [13]. An example of a graphene-fluorographene heterostructure FET is shown in Fig. 10.1. Like graphene, transition metal dichalcogenides (TMDs) are two-dimensional materials, but unlike graphene, TMDs have an intrinsic band gap, making them more suitable for transistor-based applications [14]. In particular, TMD-based transistors display high on/off ratios on the order to 10^8 [15].

Figure 10.1. **A graphene-fluorographene heterostructure field effect transistor**. (a) A schematic (side view) of a field effect transistor based on a lateral graphene (Gr) / fluorographene (GrF) / graphene (Gr) heterostructure. (b) A scanning electron microscope image (top view) of the fabricated transistor. © 2013 IEEE. Reprinted, with permission from J. S. Moon, et. al., *IEEE Electron Device Lett.* **34** (2013) pp. 1190-1192.

In Chapters 4, 5, and 6, we introduced RF measurement techniques for simplified, passive nanoelectronic devices. While these structures serve as useful, introductory examples, a more comprehensive approach is required for quantitative, broadband characterization of nanotransistors and other active devices. Here, building upon established measurement methods and equivalent circuit models for traditional FETs, we review systematic techniques for characterization of RF nanotransistors that are extendable to other active nanoelectronic devices. Below, after a brief review of modeling and measurement of conventional transistors, we illustrate the measurement methodology and device modeling through a specific example of a GaN nanowire-based FET. The methods are enabled by on-wafer calibration procedures, accurate equivalent circuit models, calibration structures for extraction of parasitic reactance, and numerical optimization processes for parameter extraction.

10.2 Modeling and measurement of active devices

10.2.1 Small-signal models of conventional transistors

Throughout this book, we have introduced a large number of models of RF and microwave systems, including broadband, two-port nanoscale devices and a variety of different local microwave probe-sample configurations. By and large, our motivation for introducing these models has been to extract estimates of physical and material parameters from broadband measurements. In commercial applications such as wireless communications, circuit designers develop and rely upon active device models to maintain efficient design cycles and minimize time to market. [16] These models may take on a variety of forms and often take advantage of the computational capabilities of commercial finite-element solvers, computer-aided design software, circuit simulators, and multi-physics packages. Physical models attempt to describe not only the electromagnetic properties of constituent materials and circuit elements, but also thermal and mechanical effects within a device. Given the complexity of state-of-the-art FETs and other active devices, comprehensive physical models can be both elaborate and computationally intensive. By contrast, compact circuit models strive to capture the fundamental behavior of a device, often sacrificing some measure of detailed understanding and insight for computational efficiency. Compact circuit models may be based on the designer's knowledge of the operational principles or they may be purely phenomenological. Though a great deal of work has been done in the field of FET modeling, the ongoing push to incorporate new materials and to operate at higher frequencies implies that work in this area is far from complete. Here, we will focus on compact, equivalent circuit models of a field-effect transistor operating in the small-signal regime. We will assume that the reader is familiar with the core concepts of transistors and their operation.

Several important assumptions underlie equivalent circuit models and the measurement techniques that rely upon them. For instance, though the values of some equivalent circuit parameters may be determined from DC or low-frequency measurements, use of these values in high-frequency models implicitly assumes that these circuit parameters are frequency-independent. As we will illustrate below, parasitic elements are often obtained from "cold" state measurements in which the device is not biased. If these "cold" state parameters are subsequently carried over to models of active states, then the underlying assumption is that the parasitic elements do not depend on the application of a bias to the device. Note that while the parasitic elements may not explicitly depend on the bias, in certain cases they may indirectly be affected by the bias through effects such as device heating. Finally, keep in mind that though individual circuit elements are often represented as lumped elements, they may represent effective behaviors that incorporate an aggregation of distributed, non-local effects. The relationship between equivalent circuit model elements and physical parameters of interest is likely to be complex. Thus, the most accurate determination of physical and material parameters from active device measurements will be determined by use of detailed, physical models.

Fig. 10.2 shows a typical small-signal equivalent circuit model. Fig. 10.2 shows only the intrinsic transistor, excluding parasitic elements, such as those related to contact impedance, the host structure, or measurement fixtures. The modulated current I_m flows in the active region of the device. The coupling between the drain, source and gate are described by three resistive elements (R_{gs}, R_{gd}, and R_{ds}) and three capacitive elements (C_{gs}, C_{gd}, and C_{ds}). Below, we will use this model of the intrinsic transistor as the foundation for a specialized model of a nanowire FET.

Figure 10.2. **Equivalent circuit model for an intrinsic FET.** I_m is the modulated current. R_{gs} (C_{gs}), R_{gd} (C_{gd}), and R_{ds} (C_{ds}) are the gate-source, gate-drain, and drain-source resistances (capacitances), respectively.

10.2.2 Microwave measurements of conventional transistors

There are long-standing methods for measurement and characterization of conventional transistors. The field of RF transistor measurements is vast, incorporating a wide variety of characterization techniques, including noise measurements, pulsed scattering parameter measurements, and load-pull techniques. Here, we focus on methods that are based on calibrated, small-signal scattering parameter measurements, as such methods will provide a foundation for our discussion of RF characterization of nanotransistors. However, a more comprehensive approach complements scattering parameter measurements with DC current and voltage measurements. While microwave measurements are closer to the central topic of this book, DC electrical measurements are widely used to characterize the intrinsic and extrinsic properties of transistors. Further, DC measurements can also be relevant to characterization of microwave performance, providing methods to predict RF output power and noise. Moreover, full modeling of transistor behavior, including nonlinearites and large signal behavior, requires accurate measurements of the DC voltage-current relationships. Note that DC measurements can also be used to establish equivalent circuit parameters such as the gate, source, and drain resistances. Detailed descriptions of DC characterization of conventional transistors are available in the literature. For example, Reference [17] provides a systematic approach to determination of the basic properties of a GaAs FET, including the effective gate length, channel thickness, and gate length, from DC measurements.

Microwave measurements of transistors and other active devices require reliable calibration and de-embedding techniques. As we noted in the early chapters of this book, there are a number of reliable calibration techniques that enable the de-embedding of complex scattering parameter measurements in guided-wave, fixtured, and on-wafer environments. As in the case of passive devices, extension of these methods to nanoelectronic systems requires careful consideration of the underlying assumptions about the device and the propagating modes, in particular. In Chapter 5, we showed through measurements, numerical simulation, and validation that the on-wafer, multiline thru-reflect-line (TRL) calibration was extendable to coplanar-waveguide-based nanoelectronic devices. We will take advantage of the portability of multiline TRL in an example measurement below. In general, a variety of calibration techniques are applicable to microwave and RF characterization of transistors and other active devices. These include short-open-load-thru (SOLT) and line-reflect-reflect-match (LRRM). Calibrated measurements of RF transistors often face an additional challenge in that the devices are often embedded in coaxial or other guided-wave fixtures that facilitate the measurement. The effects of the fixtures must be removed from the measurements. This is done by measurements where possible, and simulations as necessary.

Even after the effects of the test platform, on-wafer probes, and fixtures have been removed through calibration, the challenge of separating parasitic effects from intrinsic properties

remains. Unfortunately, even relatively simple, compact circuit models often incorporate ten or more unknown circuit elements. The determination of a large number of circuit elements from a single measurement of two-port, complex scattering parameters presents a complicated, potentially insurmountable optimization problem. Broadly speaking, the optimization problem can be simplified by performing additional measurements that ideally correspond to a subset of the unknown circuit elements. For example, measurement of a simpler device that excludes the active element(s) can allow independent determination of some parasitic impedances. However, this strategy requires the fabrication of another device (in addition to any calibration devices required for the preceding de-embedding step). Another strategy is to determine parasitic elements from scattering parameters that are measured under so-called "cold bias" conditions in which the drain is unbiased [18]. Effectively, measurement of both "cold bias" and active, biased scattering parameters provides more inputs into the optimization process. Even with these strategies in place, determination of the unknown circuit parameters requires non-trivial numerical optimization. Where possible, estimated circuit values should be validated by alternate approaches, including complementary DC measurements and finite-element modeling.

10.3 Determination of equivalent circuit parameters for a nanotransistor

The ongoing challenge of de-embedding of intrinsic device characteristics from scattering parameters is heightened for active, RF nanoelectronic devices. As with the case for passive devices, significant measurement challenges arise in large part from the inherent impedance mismatch between commercial test equipment and many nanoelectronic devices. Furthermore, given the unique properties of nanoscale materials, the development of accurate physical and circuit models of devices remains a work in progresss. Naturally, the models for active devices are more complex than the models presented earlier in this book for passive devices. Fortunately, in the case of nanotransistors, we can build upon an extensive, pre-existing body of knowledge, as described above. In particular, we will use traditional, semiconductor field-effect transistor (FET) equivalent circuits as a starting point and introduce appropriate corrections as needed for the specialized case of nanoelectronic transistors.

In order to describe the de-embedding strategy, we will follow References [19] and [20]. As an illustrative example, we will apply the technique to a metal semiconductor field effect transistor (MESFET) that incorporates an individual GaN nanowire. Fig. 10.3(a) shows an illustration of a planar, nanowire MESFET with a double-finger gate incorporated into a coplanar waveguide (CPW). The CPW host structure was fabricated by use of standard photolithography techniques and the individual nanowires were aligned within the device by use of dielectrophoresis [21], [22]. The photolithographic fabrication process was refined such that the drain and source contacts to the nanowire are ohmic while the gate contacts are Schottky contacts. The device wafer also included a set of calibration devices for a multiline thru-reflect-line (TRL) calibration [23] and several empty, nanowire-free devices. Thus, the wafer layout followed the schematic first introduced in Figure 6.3, but with the passive, nanowire bridge devices replaced by active, nanowire MESFETs.

Figure 10.3. **Planar, dual-gate nanowire MESFET.** (a) A schematic of a planar nanowire MESFET. The dual-gate structure, including the active GaN nanowire (NW) element, is incorporated into a coplanar waveguide. (b) The DC current (I_{ds}) vs voltage (V_{ds}) characteristics of a typical GaN nanowire MESFET. From bottom to top, the curves correspond to gate biases ranging from V_{gs} = -4 V to V_{gs} = 0 V, in 0.5 V steps. The insets show top-view, optical images of the device [20].

An equivalent circuit model of the nanowire MESFET is shown in Fig. 10.4. Note that in the example presented here, parasitic elements are determined from scattering parameters under "cold bias" conditions [18], but the model in Fig. 10.4 corresponds to the MESFET in an active, biased state. The circuit parameters in this model that can be conceptually separated into three groups, corresponding to the intrinsic transistor, the contacts, and the host structure. The first group corresponds to the intrinsic transistor, specifically the active nanowire element in the MESFET. The part of the circuit model that represents the intrinsic transistor is comparable to the more general case shown in Fig. 10.2. Here, the modulated current I_m flows in the active, nanowire element. The capacitive couplings between the drain, source and gain (C_{gs}, C_{gd}, and C_{ds}) also remain. The gate-drain and gate-source resistances (R_{gs} and R_{gd}) are negligible in the GaN nanowire MESFET and have been removed. The drain-source resistance R_{ds} has been re-cast as the channel resistance R_c to highlight the fact that this resistance is associated with the active conduction channel within the nanowire element. The next group of parameters is related to the properties of the leads and Schottky contact. The lead and contact parasitics are represented by five circuit parameters, three of which encapsulate the inactive and dynamic properties of the Schottky gate: the gate resistance R_g, the Schottky resistance R_{sch}, and the Schottky capacitance C_{sch}. R_s and R_d are the contact resistances for the source and drain, respectively. The final group of circuit elements is associated with the host structure and includes three parasitic capacitances. C_{id} is the parasitic capacitance associated with the interdigitated fingers that provide contacts to the nanowire. C^R_{tp} and C^L_{tp} correspond to the tapered CPW segments on the right and left sides of the device, respectively. In order to determine all of the circuit parameters, our strategy will be to sequentially consider the host structure parasitics, followed by the lead and contact parasitics, and lastly the active nanowire element. Finally, we note that based upon inspection of the device symmetry, C_{gs} and C_{gd} are expected to be of the same order. Likewise, the values of C^R_{tp} and C^L_{tp} should be close.

Figure 10.4. **Equivalent circuit model for a nanowire MESFET.** The complete equivalent circuit model, including the host structure parasitic elements, is shown. *P1* and *P2* correspond to Ports 1 and 2, respectively. The symbols for the individual circuit elements are defined in the text [20].

As a first step, calibrated, on-wafer measurements are made in order to extract the complex scattering parameters of the calibration structures, nanowire transistors, and empty transistors. In the particular case of GaN nanowire MESFETs, multiline TRL was chosen as the calibration method as it enables calculation of the CPW propagation constant, and in turn, the translation of the reference planes to positions near to the device, as illustrated in Fig. 10.1. However, alternate on-wafer approaches may be used in place of TRL, with the choice depending upon the device layout as well as the availability of calibration structures, among other factors. Initially, measurements of the empty devices and MESFETs are carried out in the cold state with the gate and drain unbiased. As GaN is photoconductive, the devices were measured only in a dark state after prolonged isolation from any optical illumination. The two-port, calibrated scattering parameters of the empty device in the cold state are $S_{ij}{}_{meas}^{empty}$, where i and j indicate the port indices (i = 1,2; j = 1,2). Similarly, the two-port, calibrated scattering parameters of the transistor device in the cold state are $S_{ij}{}_{meas}^{cold}$. Subsequently, the MESFETs are measured in the active state of normal operation with the devices biased accordingly. The two-port, calibrated scattering parameters of the transistor device in the active state are $S_{ij}{}_{meas}^{active}$. In the analysis below, the scattering parameters $S_{ij}{}_{meas}^{empty}$, $S_{ij}{}_{meas}^{cold}$, and $S_{ij}{}_{meas}^{active}$ are transformed to admittance matrix elements ($Y_{ij}{}_{meas}^{empty}$, $Y_{ij}{}_{meas}^{cold}$, and $Y_{ij}{}_{meas}^{active}$) and impedance matrix elements ($Z_{ij}{}_{meas}^{empty}$, $Z_{ij}{}_{meas}^{cold}$, and $Z_{ij}{}_{meas}^{active}$), as needed.

With the calibrated, on-wafer measurements complete, the next step is the determination of the parasitic capacitances associated with the host structure. These parameters can be determined from the scattering parameters $S_{ij}{}_{meas}^{empty}$. In Chapters 4 and 6, we introduced an analagous "empty device" method for characterization of passive, two-port devices. Here, the method is extended to include three parasitic capacitive terms: C_{id}, $C^{R}{}_{tp}$, and $C^{L}{}_{tp}$. The equivalent circuit shown Fig. 10.4 can be modified to represent an empty device by removing all circuit elements related to the active nanowire, the leads, and the contacts. This leaves the three parasitic capacitances - C_{id}, $C^{R}{}_{tp}$, and $C^{L}{}_{tp}$ - configured in a pi-network. Thus, C_{id}, $C^{R}{}_{tp}$, and $C^{L}{}_{tp}$ are given by [20]

$$C_{id} = -\frac{1}{2\omega}\left[\Im\left(Y_{12}{}_{meas}^{empty}\right) + \Im\left(Y_{21}{}_{meas}^{empty}\right)\right] \quad , \qquad (10.1a)$$

$$C^{R}{}_{tp} = \frac{1}{\omega}\Im\left(Y_{22}{}_{meas}^{empty}\right) - C_{id} \quad , \qquad (10.1b)$$

$$C^{L}{}_{tp} = \frac{1}{\omega}\Im\left(Y_{11}{}_{meas}^{empty}\right) - C_{id} \quad , \qquad (10.1c)$$

where ω is the radial frequency. We use the notations $\Re(X)$ and $\Im(X)$ to represent to the real and imaginary parts of a complex variable X, respectively. The pi-model of the empty device can then be expressed as an admittance matrix $\boldsymbol{Y}_{\boldsymbol{model}}^{\boldsymbol{empty}}$ in the form

$$\boldsymbol{Y}_{\boldsymbol{model}}^{\boldsymbol{empty}} = \begin{bmatrix} j\omega\left(C^{L}{}_{tp} + C_{id}\right) & -j\omega C_{id} \\ -j\omega C_{id} & j\omega\left(C^{R}{}_{tp} + C_{id}\right) \end{bmatrix} . \qquad (10.2)$$

The calibrated admittance parameters of the transistor ${Y_{ij}}_{meas}^{cold}$, and ${Y_{ij}}_{meas}^{active}$ can now be corrected to remove the host structure parasitic elements by

$$\boldsymbol{Y_{meas}^{cold-corr} = Y_{meas}^{cold} - Y_{model}^{empty}} \qquad (10.3a)$$

and

$$\boldsymbol{Y_{meas}^{act-corr} = Y_{meas}^{act} - Y_{model}^{empty}} \quad . \qquad (10.3b)$$

The simple algebraic form of Equations (10.3) relies on the assumption that the network of host structure parasitic elements is in parallel with the rest of the device. Note that this is assumption may not be valid for all device configurations and ideally should be verified by both measurements and numerical modeling.

Having corrected the calibrated measurements by removing the parasitic effects of the host structure, we turn now to the isolation of the circuit elements associated with the active nanowire element. This requires removing the parasitic effects of the leads and contacts. Above, the measurement of the empty transistor device enabled the isolation of the host structure's parasitic circuit elements from the rest of the circuit model. Unfortunately, there is no analogous reference device or measurement strategy for isolating the parasitic effects of the leads and contacts.

As a first step, consider the group of circuit elements associated with the leads and contacts. Since these elements form a tee-network, the equivalent circuit can be naturally expressed as an impedance matrix:

$$\boldsymbol{Z_{model}^{lead}} = \begin{bmatrix} R_g + R_S + \frac{R_{sch}}{1+j\omega R_{sch} C_{sch}} & R_S \\ R_S & R_d + R_S \end{bmatrix} \quad . \qquad (10.4)$$

Next, consider the group of circuit elements associated with the internal nanowire element. Since this group of elements forms a pi-network, an admittance matrix representation is most suitable:

$$\boldsymbol{Y_{model}^{nw}} = \begin{bmatrix} j\omega\left(C_{gs} + C_{gd}\right) & -j\omega C_{gd} \\ -j\omega C_{gd} & \frac{1}{R_{ds}} + j\omega\left(C_{ds} + C_{gd}\right) \end{bmatrix} \quad . \qquad (10.5)$$

It is vital to note that while the contributions of C_{gs}, C_{gd}, and C_{ds} are often negligible for thin-film-based MESFETs, in the case of the nanowire MESFET example, they can't be neglected. The admittance matrices $\boldsymbol{Z_{model}^{lead}}$ and $\boldsymbol{Z_{model}^{nw}}$ can be combined to model to combination of the leads and the nanowire elementL: $\boldsymbol{Z_{model}^{cold-corr}}$ ($\boldsymbol{Z_{model}^{nw}}$ is the impedance matrix that corresponds to $\boldsymbol{Y_{model}^{nw}}$). Initial estimates of R_g, R_s, and R_d are determined from the high-frequency behavior of the corrected cold device measurements $\boldsymbol{Z_{meas}^{cold-corr}}$ [20]:

$$R_S \approx \frac{\Re\left({Z_{12}}_{meas}^{cold-corr}\right) + \Re\left({Z_{21}}_{meas}^{cold-corr}\right)}{2} \quad , \qquad (10.6a)$$

$$R_g + R_s \approx \Re\left({Z_{11}}_{meas}^{cold-corr}\right) \quad , \qquad (10.6b)$$

$$R_d + R_s \approx \Re\left(Z_{22}{}_{meas}^{cold-corr}\right) \quad . \tag{10.6c}$$

In a similar fashion, initial estimates of R_{sch}, R_c, C_{gd}, C_{gs}, and C_{gd} are determined from the low-frequency behavior of $\boldsymbol{Z}_{\boldsymbol{meas}}^{\boldsymbol{cold-corr}}$ [20]

$$R_g + R_s + R_{sch} + \left(\frac{C_{gd}}{C_{gd}+C_{gs}}\right)^2 R_c \approx \Re\left(Z_{11}{}_{meas}^{cold-corr}\right) , \tag{10.7a}$$

$$R_s + \frac{C_{gd}}{C_{gd}+C_{gs}} R_c \approx \frac{1}{2}\left(\Re\left(Z_{12}{}_{meas}^{cold-corr}\right) + \Re\left(Z_{21}{}_{meas}^{cold-corr}\right)\right) , \tag{10.7b}$$

$$R_g + R_s + R_c \approx \Re\left(Z_{22}{}_{meas}^{cold-corr}\right) , \tag{10.7c}$$

in conjunction with an initial estimation that all of the capacitive elements are 1 fF. These initial estimates are subsequently used as seed values for a numerical fitting procedure that optimizes all of the parameters such that the differences between the model $\boldsymbol{Z}_{\boldsymbol{model}}^{\boldsymbol{cold-corr}}$ and the experimental data $\boldsymbol{Z}_{\boldsymbol{meas}}^{\boldsymbol{cold-corr}}$ are minimized. The numerical optimization routine interfaces with a commercial circuit simulator that calculates the scattering parameters from the circuit model. The resulting values of the parasitic circuit elements R_g, R_s, R_d, R_{sch}, and C_{sch} are now fixed and used to calculate the $\boldsymbol{Z}_{\boldsymbol{model}}^{\boldsymbol{lead}}$. However, the estimates of the nanowire circuit elements R_c, C_{gd}, C_{gs}, and C_{gd} are discarded.

The final values of R_c, C_{gd}, C_{gs}, and C_{gd} are determined from the active state measurements. The admittance matrix of the active nanowire element can be de-embedded from the original measurements by

$$\boldsymbol{Y}_{\boldsymbol{meas}}^{\boldsymbol{NW}} = \boldsymbol{Y}_{\boldsymbol{meas}}^{\boldsymbol{act-corr}} - \boldsymbol{Y}_{\boldsymbol{model}}^{\boldsymbol{lead}} = \boldsymbol{Y}_{\boldsymbol{meas}}^{\boldsymbol{act}} - \boldsymbol{Y}_{\boldsymbol{model}}^{\boldsymbol{empty}} - \boldsymbol{Y}_{\boldsymbol{model}}^{\boldsymbol{lead}} \quad . \tag{10.8}$$

Comparison of $\boldsymbol{Y}_{\boldsymbol{meas}}^{\boldsymbol{NW}}$ to Equation (10.5) leads to simple expressions for the unknown nanowire parameters:

$$C_{gd} = \frac{-\Im\left(Y_{12}{}_{meas}^{NW}\right)}{\omega} , \tag{10.9a}$$

$$C_{gs} = \frac{\Im\left(Y_{12}{}_{meas}^{NW}\right)+\Im\left(Y_{11}{}_{meas}^{NW}\right)}{\omega} , \tag{10.9b}$$

$$C_{ds} = \frac{\Im\left(Y_{12}{}_{meas}^{NW}\right)+\Im\left(Y_{22}{}_{meas}^{NW}\right)}{\omega} , \tag{10.9c}$$

and

$$R_c = \frac{1}{\Re\left(Y_{22}{}_{meas}^{NW}\right)} \quad . \tag{10.9d}$$

Typical equivalent circuit values for a GaN nanowire device such as the one shown in Fig. 10.1 are [19]: $C^{L}{}_{tp}$ = 11.6 fF; $C^{R}{}_{tp}$ = 11.3 fF; C_{id} = 1.5 fF; C_{sch} = 3.5 fF; R_{sch} = 16000 Ω; C_{ds} = 0.0 fF; C_{gs} = 5.5 fF; C_{gd} = 2.2 fF; R_g = 3680 Ω; R_d = 108 Ω; and R_s = 270 Ω.

Two additional transistor metrics can be directly obtained from $\boldsymbol{Y}_{\boldsymbol{meas}}^{\boldsymbol{NW}}$: the transconductance g_m and the transit time τ. The transconductance is defined by

$$g_m \equiv \left.\frac{\delta I_{ds}}{\delta V_{gs}}\right|_{V_{ds}=constant} \quad . \qquad (10.10)$$

Thus, larger values of transconductance correspond to an increased sensitivity of the source-drain current I_{ds} to the gate-source voltage V_{ds}. The transconductance is related to the admittance parameters of the active nanowire element through [20]

$$g_m = \left\{\Re\left(Y_{21}{}_{meas}^{NW}\right)^2 + \left[\Im\left(Y_{21}{}_{meas}^{NW}\right) - \Im\left(Y_{12}{}_{meas}^{NW}\right)\right]^2\right\}^{1/2} \quad . \qquad (10.11)$$

The modulated current is related to the transconductance as follows:

$$I_m = g_m V_i e^{-j\omega\tau} \quad , \qquad (10.12)$$

where V_i is the voltage across C_{gs}, ω is the operating frequency, and τ is the transit time. The transit time quantifies the inherent response delay of a field-effect transistor. It is the governing factor in determination of the cut-off frequency and can be determined from [20]

$$\tau = \frac{\cos^{-1}\left[\Re\left(Y_{21}{}_{meas}^{NW}\right)/g_m\right]}{\omega} \qquad (10.13)$$

Typical values for a GaN nanowire MESFET are g_m = 16.6 μS and τ = 9.8 ps with a drain-source voltage V_{ds} of 5 V [20].

It is important to notice that we have made a broad, simplifying assumption that all of the equivalent circuit parameters are independent of bias voltage. While this may be a reasonable assumption for some of the parameters, such as the host structure parasitic capacitances, it is almost certainly untrue for the elements associated with the active nanowire element. A more complete characterization would necessarily require calibrated measurements of $S_{ij}{}_{meas}^{active}$ under varying bias conditions and subsequent re-calculation of the voltage-dependent circuit elements for each bias condition.

The uncertainties in the calibrated, small-signal scattering parameters of the nanotransistor can be calculated following the analysis presented in Chapter 6. The uncertainty of the admittance parameters is calculated from

$$\Delta Y_{ij}{}_{meas}^{cold-corr} = \sqrt{\left(\Delta Y_{ij}{}_{meas}^{empty}\right)^2 + \left(\Delta Y_{ij}{}_{meas}^{active}\right)^2 + \left(\Delta Y_{ij}^{M-M}\right)^2} \quad , \qquad (10.14)$$

Where $\Delta Y_{ij}{}_{meas}^{empty}$ and $\Delta Y_{ij}{}_{meas}^{active}$ are the uncertainties in the admittance matrices of the empty device and the nanowire device in the active state, respectively. Uncertainties in the admittance matrices Y_{ij} are determined from the uncertainties in the measured scattering parameters S_{kl} through

$$\Delta Y_{ij} = \sqrt{\sum_{k,l}\left(\frac{\delta Y_{ij}}{\delta S_{kl}} S_{kl}\right)^2} \quad . \qquad (10.15)$$

ΔY_{ij}^{M-M} is the difference between the modeled and measured admittances for the empty device. Statistical (Type A) uncertainties are neglected in in Equation (10.14) as they are significantly smaller than the systematic errors. In general, additional contributions to the uncertainty may arise from the device fabrication process, which may lead to variability in material properties and feature geometry from device to device. Here, these contributions were found to be negligible compared to the uncertainty terms included in Equation (10.14), which is not surprising given that all of the nanotransitors, empty devices, and calibration structures were fabricated on the same wafer. Measured and modeled scattering parameters for the MESFET device are shown in Fig. 10.5, along with calculated uncertainties. As we saw with a passive nanowire device in Chapter 6, the magnitude of the uncertainties approaches the magnitude of the measured transmission. For example, the values of $|S_{21}|$ and $|S_{12}|$ on a linear scale at 4 GHz, are 0.0017 (+0.0011, -0.0007) and 0.0011 (+0.0003, -0.0009). While this prototype device is suitable for demonstration of measurement methods, the low signal values preclude most practical applications. Increased transmission in nanowire- and nanotube-based FETs can be facilitated by use of multiple nanowires in parallel [24] or aligned arrays of nanotubes [25].

Figure 10.5. **Scattering parameters of a GaN nanowire MESFET.** The measured (open shapes) and simulated (dashed lines) scattering parameters of the MESFET are shown for (a) forward transmission, S_{21} and (b) reverse transmission, S_{12}. The simulation is based on the equivalent circuit model shown as an inset in (a). Estimated uncertainties are shown in gray. Note that the scale has been adjusted to allow a detailed comparison on the simulated and measured values. As a result, the shaded uncertainty bands extend past the edge of the graphs [20].

In summary, several broader lessons and strategies are revealed by the case study of the GaN nanowire MESFET. First, as was the case for passive nanoelectronic devices, calibration and de-embedding play a critical role in the characterization of active nanoelectronic devices. This is true both for on-wafer devices as well as devices embedded in fixtures. Calibration and de-embedding enable us to distinguish intrinsic behavior from the overall device response. Moreover, the accuracy and reproducibility of the calibrated measurements will depend not only on the chosen method, but also on practical issues such as the skill of the user, the quality of the test platform, and the stability of the measurement environment. Another lesson from this case study is that the choice of equivalent circuit model directs certain aspects of the measurement strategy. Here, we saw that the equivalent circuit model could be modularized into three groups of circuit elements. As a result, the measurement process sequentially addressed each circuit element group. We also observed that specialized calibration structures can play an important role in determining parasitic elements. Here, the empty device served as a calibration structure and enabled the determination of several parasitic capacitances, thus reducing the number of unknown elements in the circuit model. Though we did not take advantage of DC measurements in this particular example, DC measurements can also play an important role in determining circuit models as well as large-

signal and nonlinear effects. Finally, we saw that numerical simulations and optimization are often necessary for full characterization and validation of active device measurements.

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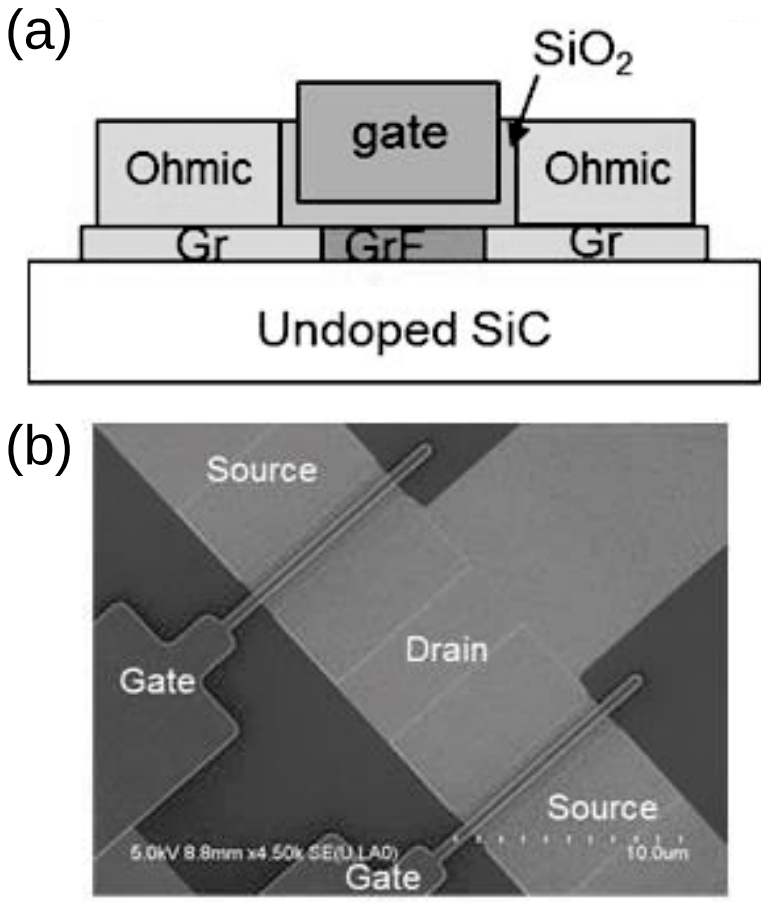
(a)
SiO_2
gate
Ohmic
Ohmic
Gr
GrF
Gr
Undoped SiC
(b)
Source
Drain
Gate
Source
Gate
5.0kV 8.8mm x4.50k SE(U,LA0)
10.0um

Figure 10.1

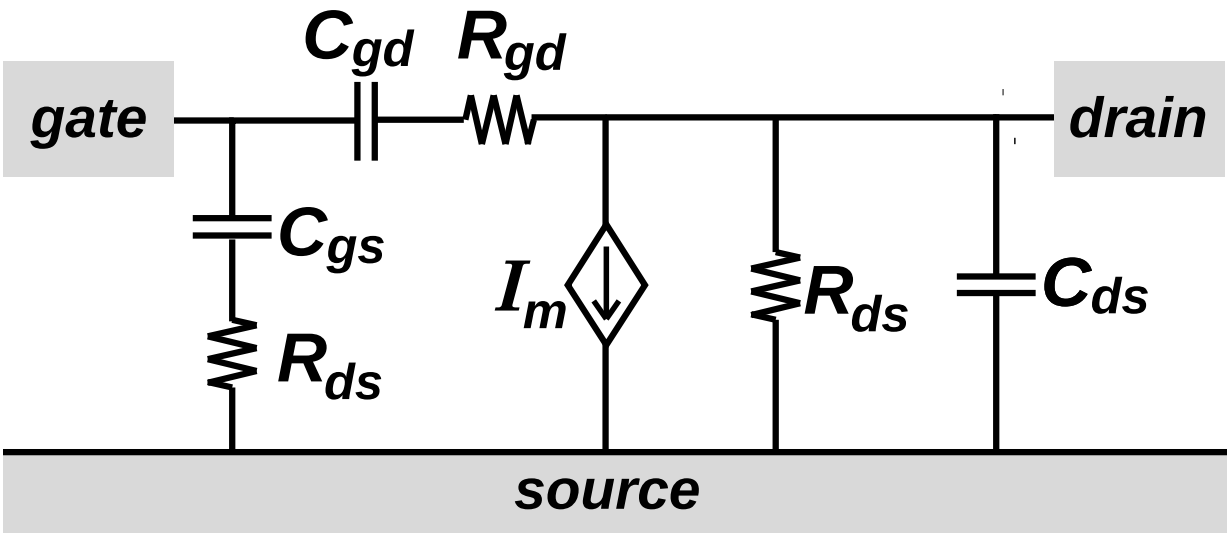

Figure 10.2

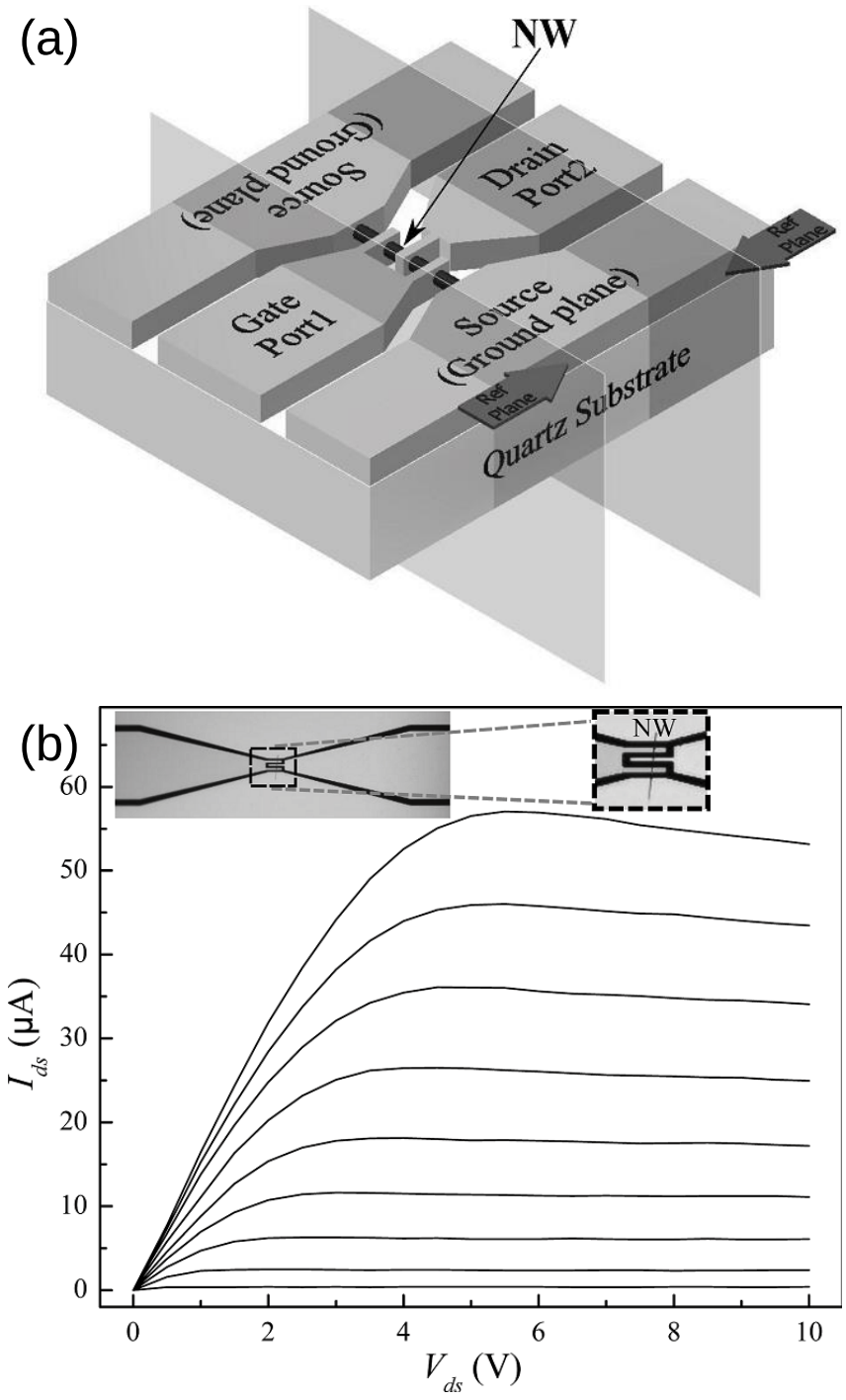
(a)
NW
Source
(Ground plane)
Drain
Port2
Gate
Port1
Source
(Ground plane)
Ref
Plane
Ref
Plane
Quartz Substrate
(b)
NW
60
50
40
30
20
10
0
I_{ds} (μA)
0
2
4
6
8
10
V_{ds} (V)

Figure 10.3

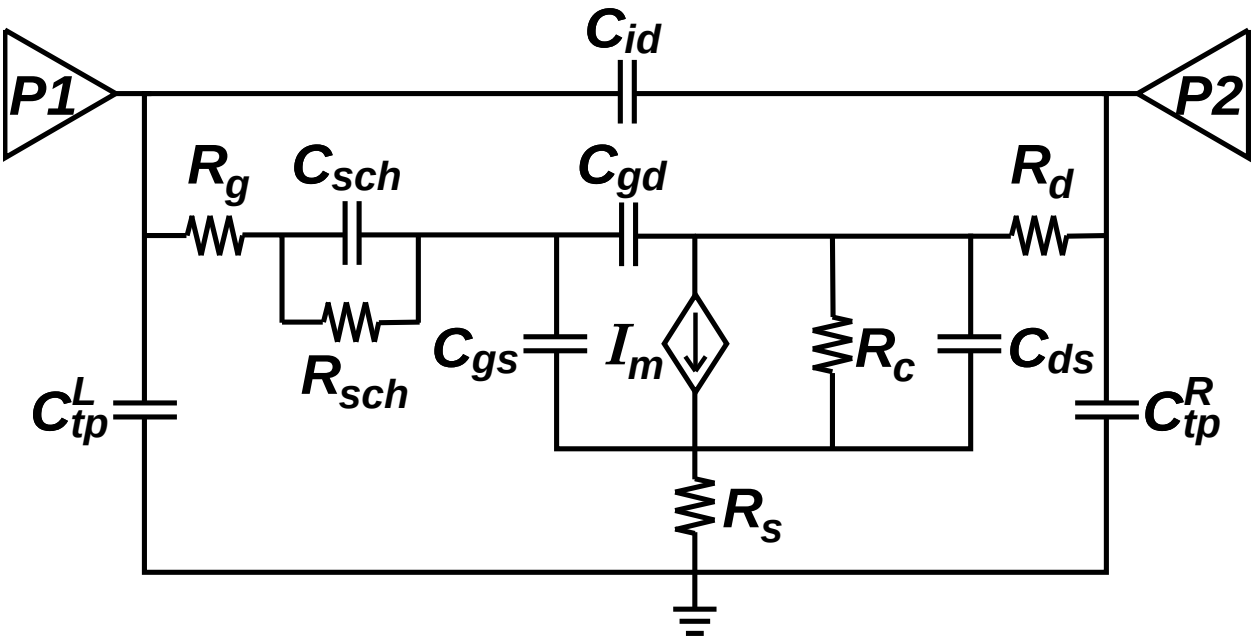

Figure 10.4

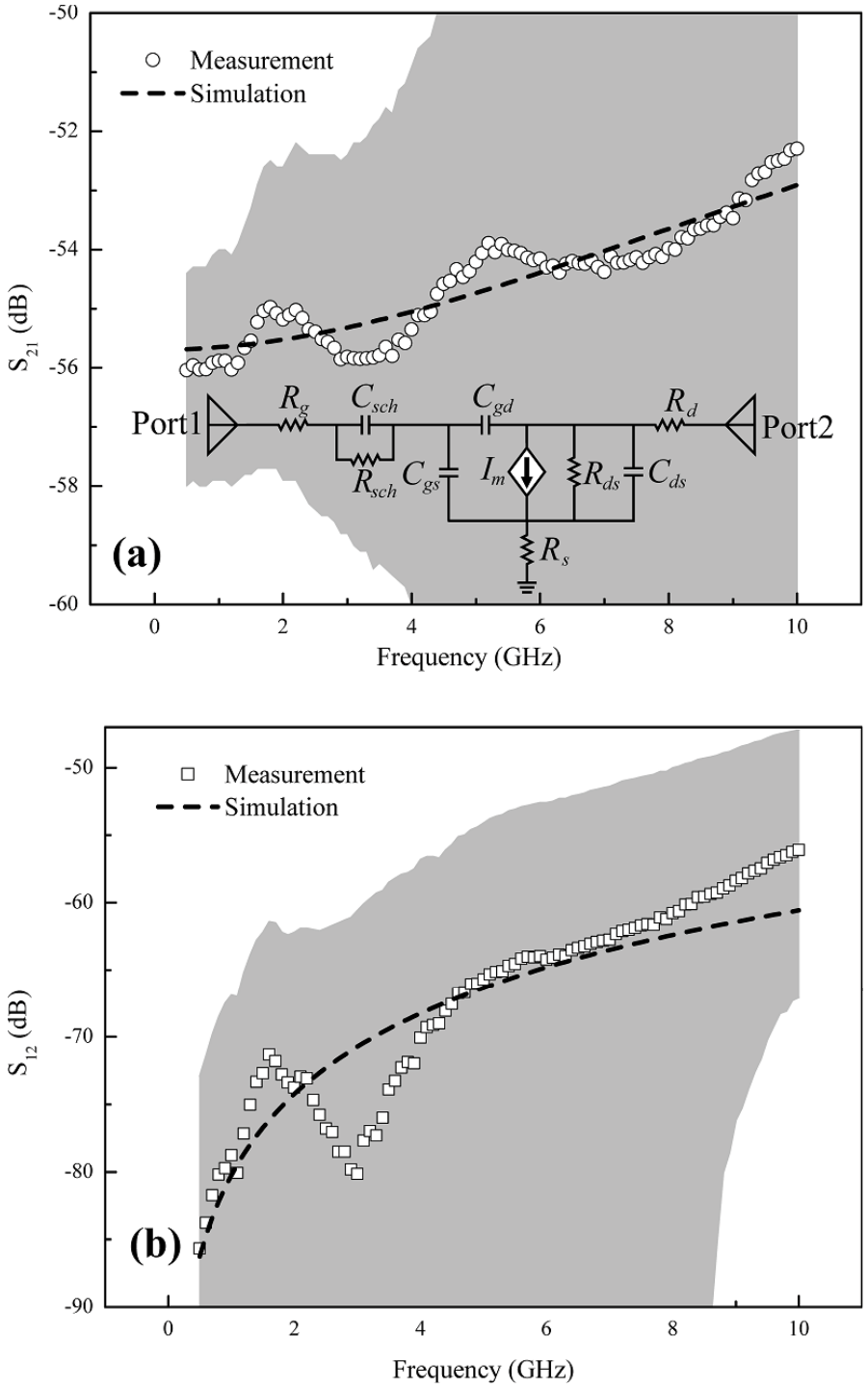
Measurement
Simulation
S21 (dB)
Frequency (GHz)
Port1
Port2
Rg
Csch
Cgd
Rd
Rsch
Cgs
Im
Rds
Cds
Rs
(a)
Measurement
Simulation
S12 (dB)
Frequency (GHz)
(b)

Figure 10.5