# Chapter 4
# On-wafer measurements of RF nanoelectronic devices

## 4.1 Broadband characterization of RF nanoelectronic devices

The preceding chapters have introduced the core concepts and techniques of microwave measurements, in general, and techniques for microwave measurements of extreme impedance devices, in particular. Here, we narrow the focus further to on-wafer, microwave measurements of RF nanoelectronic devices. In this chapter, the term "nanoelectronic devices" refers to electronic, charge-based devices that incorporate nanoscale elements or nanomaterials, such as carbon nanotubes, semiconducting nanowires, or graphene. For now, discussion will be further limited to characterization of passive devices (Characterization of active devices will be discussed in Chapter 10). In a device development environment, *a priori* knowledge of the electronic properties of such nanoscale building blocks may be limited. Further, physical properties of nanoscale material systems may vary strongly from building block to building block and consequently, performance may vary strongly from device to device. As a result, fundamental device properties such as device impedance or cutoff frequency may be unknown and broadband measurements will be required to determine them.

The development of such broadband metrology is but one piece of a comprehensive measurement framework of RF nanoelectronic devices. The first element of such a framework is nanofabrication. It is only through considerable advances in the fabrication of nanomaterials and devices over recent years that RF nanoelectronic devices have become realizable. In the context of characterizing such devices at RF, the integration of nanoscale building blocks into RF-compatible structures such as coplanar waveguides (CPWs) is a necessary step. While a comprehensive discussion of nanofabrication is outside the scope of this book, clear understanding of nanofabrication techniques is an asset in the design and execution of nanoelectronic device metrology. The second aspect of the measurement framework is the suite of specific measurement techniques for RF nanoelectronic devices, as described in this chapter and the literature referenced herein. Third, appropriate circuit models need to be developed in order to extract physical, material and electrical parameters from broadband measurements. Finally, the measurement framework must be validated by comparison to modeling and simulation. In Chapter 5, comprehensive modeling, parameter extraction and finite element simulation will be discussed, completing the measurement framework for broadband characterization of RF nanoelectronic devices. Within this measurement framework, the following objectives are realized: (a) calibrated measurements of the frequency-dependent scattering parameters and impedance of the nanoelectronic device are obtained, (b) the intrinsic properties of the nanoelectronic device are de-embedded from contact properties and other parasitic effects, including the stray capacitance (c) circuit models that describe the nanoscale element and its contacts are developed and fully validated (d) estimates of quantitative values of circuit parameters are extracted from the measurements. By realizing these objectives, the measurement framework may inform development and design of emerging RF nanoelectronics applications.

The focus of the present chapter is the measurement of de-embedded, complex scattering parameters of a two-port, passive nanoelectronic device over a broad bandwidth, typically from tens of megahertz to tens of gigahertz. Presently, most nanoelectronic devices are

implemented on wafer. The on-wafer measurement environment presents new challenges that are not present in the guided-wave measurement environment, including radiative loss and parasitic coupling between measurement probes. For RF nanoelectronic devices, these challenges are further augmented by the inherent impedance mismatch with commercial test equipment as well as design and fabrication challenges associated with integrated nanoscale building blocks into on-wafer, RF host structures.

In order to address these challenges, several strategies have been developed. Because of the inherent challenges of the on-wafer measurement environment, the user must observe best practices in order to obtain meaningful, on-wafer measurements. A number of such practical considerations are reviewed in the following section. To address the specific measurement problems presented by RF nanoelectronic devices, several different approaches have been developed, including the on-wafer application of the techniques described in the previous chapter on extreme impedance measurements. Below, three additional approaches to broadband, on-wafer measurements of nanoelectronic devices are discussed. The first approach is based on the integration of the nanoscale element into a Wheatstone bridge structure. The second approach augments traditional on-wafer calibration with the measurement of an additional, "empty" reference device. The third approach is based on fabrication of many nanostructures in parallel in order to produce an impedance-matched on-wafer device.

### 4.2 Practical considerations for on-wafer measurements

In order for RF nanolectronic applications to become widely deployed in the near future, they must be compatible with existing electronics technology. More specifically, they must be compatible with the engineering and fabrication of silicon-based CMOS devices. As a result, many prototype RF nanoelectronic devices are presently implemented on-wafer. A variety of fabrication techniques have been developed to integrate nanostructures such as nanowires, nanotubes, and two-dimensional materials into processes that are compatible with standard lithographic patterning of planar electronics. Though there are examples of nanostructures implemented in non-planar geometries, such as carbon nanotube composites for shielding applications, our discussion will focus upon on-wafer measurements of the complex scattering parameters of RF nanoelectronic devices. In Chapter 2, we reviewed the core concepts and underlying theory of calibration and de-embedding, in general, and the on-wafer, multi-line through-reflect-line (TRL) technique, in particular. Here, we review practical aspects of a typical on-wafer test platform, from the network analyzer and cables, through the probes, and onto the device under test (DUT) itself. For any application, the on-wafer measurement environment has historically been a challenging one [1], requiring appropriate methodology, sound theory [2], as well as a skilled, practiced user. In the case of nanoelectronic devices, these challenges are further compounded, particularly with respect to measurement sensitivity and repeatability.

A schematic of a typical on-wafer test platform is shown in Fig. 4.1. A stable measurement environment, free from both significant mechanical noise as well as fluctuations in temperature and humidity, is a necessity. The vector network analyzer (VNA) is the heart of any test platform for scattering parameter measurements of coaxial, waveguide, or on-wafer DUTs. Broadband cables provide a signal path from the VNA to the probes, which in turn connect to the on-wafer DUT. As the probes will need to be re-positioned throughout the measurement, flexible cables are usually required. Cables should be chosen to minimize

temperature-, humidity-, and flexure-related changes in phase. In order to verify that the VNA and cables are in good working order, it is best practice to maintain a coaxial verification kit that consists of multiple, well-characterized DUTs that benchmark the measurement platform in different ways. A typical two-port verification kit might include a two-port attenuator, a two-port mismatch standard (also known as a Beatty standard), a one-port matched load, and a one-port flat short circuit. Before connecting the on-wafer contact probes, measurement of each of these verification standards at the coaxial reference planes with a calibrated system will establish that there are no systematic problems with the VNA or cabling.

Figure 4.1. **Schematic of an on-wafer test platform**. Key components include a vector network analyzer, broadband cabling, and contact probes. The device under test (DUT) is illustrated here as a coplanar waveguide.

Before discussing on-wafer microwave probes, which effectively transform a guided-wave measurement platform into an on-wafer platform, it useful to briefly review the properties of microwave and RF coaxial connectors, as most of the off-wafer interfaces in the test platform will be coaxial. In general, as the dimensions of a coaxial connector decrease, its operational frequency range will increase. Specific examples of precision connectors (and their nominal frequency cutoff) include 3.5 mm (33 GHz), 2.4 mm (50 GHz), and 1.0 mm (110 GHz). The increased frequency range of smaller connectors comes with an important tradeoff: smaller connectors are mechanically more fragile and require delicate handling by skilled, experienced users to avoid rapid degradation or damage. Use of an appropriate torque wrench is an absolute requirement for repeatable measurements that do not damage connectors. Additionally, consistent use of the same connector type throughout the off-wafer measurement platform will improve the quality of measurements and the ease of de-embedding. Excessive use of intertype adapters introduces extra interfaces and unwanted impedance mismatches along the signal path. Finally, the connector life and measurement repeatability will both be maximized by regular inspection and cleaning of connectors.

Microwave probes provide a signal path from the cabling to the on-wafer DUT. On one side, a probe connects to the connectorized environment via a standard coaxial or waveguide interface. On the other side, the probe has sharp metallic points that are electrically connected to the ground and signal lines. Signal transmission to the on-wafer environment is achieved by bringing these points into direct mechanical contact with the signal and ground lines on a planar guided-wave structure, such as a co-planar waveguide (CPW). Note that the probe points are generally designed to skate laterally along the DUT as they make mechanical contact. Typical lateral skate distances are on the order of ten to fifty micrometers. For CPW measurements, a ground-signal-ground (GSG) configuration of the probe points is required. Other configurations, such as ground-signal (GS), are available to accommodate alternative device geometries. The probe pitch is determined by the distance between the ground and signal connections, with typical values of the pitch in the range from tens of micrometers to millimeters. Clearly, the on-wafer device geometry must be designed to match available probes.

Commercial on-wafer probe stations provide mechanical support for the test platform and motion control in order to control the position and orientation of components. The DUT wafer is generally held in place on the smooth surface of a vacuum chuck. Probes are generally mounted on a three-axis (XYZ) translation stage as well as a goniometer. Further,

the DUT wafer is usually also on a translation stage, so that once the probe orientation is optimized, access to different DUTs can be achieved by moving the wafer, with minimal re-positioning of the probes. Given the mechanical dimensions, an optical microscope is necessary for relative positioning of both DUTs and probes.

Microwave measurements are particularly sensitive to the quality and repeatability of the mechanical interface between a microwave probe and the DUT. Two issues are critical: planarization and repeatable lateral positioning. If the points of the probe are not aligned in the plane of the device, the quality of contacts can differ between points, and in the worst case, one or more of the points may fail to contact the DUT surface, leading to stray capacitance and measurement errors. In practice, probe planarization can be checked by contacting a metal surface on the DUT wafer and examining the mechanical scratches in the metal surface that result from the probe points skating on the surface. Scratches of equal length and depth indicate proper planarization of the probe. In order to achieve repeatable measurements, it is also necessary to position the probes at the same position on all comparable DUTs for every measurement. In particular, the distance that the probes skate after contact must be consistent. One strategy to achieve this is to use an automated, programmable probe positioner. When automated positioning is not available, appropriate fiduciary marks can be incorporated into the DUT design, as shown in Fig. 4.2.

Figure 4.2. **Photograph of a coplanar waveguide**. Note the alignment marks at the side of the structure, which are used to improve the repeatability of the probe contact position and the distance that the probes skate during repeated measurements. Photograph by N. Orloff, NIST.

With all of the elements of the test platform in place, including the VNA, cabling, and microwave probes, informed choices can be made with respect to the design of the DUT wafer. Ideally, any necessary calibration structures will be fabricated on the same substrate as the DUTs. While calibration methods exist for situations where the calibration structures are on separate substrates [3], the introduction of additional uncertainty by use of such methods presents an unwanted complication to sensitive measurements of RF nanoelectronics. Repeated measurements of both calibration standards and DUTs present an additional strategy for reducing statistical uncertainties. If possible, the implementation of a verification standard, such as an on-wafer mismatch standard, on the same wafer is also highly desirable.

## 4.3 Wheatstone bridge approach

### *4.3.1 The Wheatstone bridge*

In Chapter 3, interferometric methods were introduced to measure the scattering parameters of extreme impedance DUTs. While implementation of these methods in an on-wafer environment is possible in principle, experimental demonstration of such an on-wafer implementation is challenging to achieve. Note that a fully on-wafer implementation of such a method would require integration of the DUT as well as a well-known reference impedance $Z_{ref}$ with an on-wafer power splitter or on-wafer hybrid coupler. Alternately, a connectorized splitter or hybrid coupler could be used, with the DUT and the reference impedance device (or multiple reference impedance devices) remaining on the wafer. A set of calibration structures would also be needed, ideally on the same wafer substrate.

A host device architecture, based on a Wheatstone bridge, provides an alternative approach to on-wafer measurements of high-impedance nanoelectronic systems, such as carbon nanotubes [4,5]. Like the interferometric methods, the bridge-based method effectively reduces the impedance mismatch between the nanoelectronic device and the test equipment. This method reduces measurement error, though it requires that the nanoelectronic device be integrated into a specific test structure and enough wafer area must be available for the fabrication of the bridge structure as well as several bridge-based calibration structures. Before describing this method in detail, we will review the basic concepts of a Wheatstone bridge.

Figure 4.3. **Schematic of a Wheatstone bridge**. The bridge consists of a detector and four impedances: $Z_1$, $Z_2$, $Z_3$, and $Z_L$. The circuit is driven by an RF oscillator (*Osc*).

A schematic of a Wheatstone bridge is shown in Fig. 4.3. The bridge consists of a detector and four impedances, one in each of the four branches of the bridge: $Z_1$, $Z_2$, $Z_3$, and $Z_L$. The circuit is driven by an RF oscillator. One useful feature of this structure is that it can be used to measure an unknown impedance in one arm of the bridge, provided that the other three impedances are known. In general, the ratio of the detector signal, *Vdet*, to the input signal *Vosc*, is given by

$$\frac{V_{det}}{V_{osc}} = \left(\frac{Z_3}{Z_2+Z_3} - \frac{Z_L}{Z_1+Z_L}\right) \quad . \tag{4.1}$$

If the signal at the detector is zero, the bridge is said to be balanced and the unknown impedance is given by

$$Z_L = \frac{Z_1}{Z_2} Z_3 \quad . \tag{4.2}$$

Ideally, the general strategy for impedance measurement with a Wheatstone bridge is implemented with a variable impedance in one of the arms of the bridge. Then, the variable impedance is tuned so that the signal at the detector is zero and the unknown impedance can be determined from Equation (4.2). In an on-wafer environment, it is much simpler to implement a fixed impedance than a variable impedance. As a result, an alternative measurement strategy will be developed below.

*4.3.2 Bridge-based measurement of a nanoelectronic device*

The Wheatstone bridge is the basis for an elegant approach to measurement of an individual nanofiber such as a nanowire or carbon nanotube (CNT) [4,5]. In order to extend the Wheatstone bridge-based approach to an individual nanowire, nanotube, or other nanoscale building block, the nanoscale element must be integrated into an on-wafer Wheatstone bridge. Schematics and a signal flow diagram of such a measurement structure are shown in Fig. 4.4. As shown in Fig. 4(a), the nanoelectronic DUT is connected across one branch of the bridge, while resistors are connected across each of the other branches of the bridge. For the measurement of a nanoscale element with an impedance on the order of the resistance quantum (12.9 kΩ) such as an individual, single-wall CNT, the bridge resistance $R_{br}$ should be on the order of 1 kΩ. This reduces the impedance mismatch

between the bridge structure and commercial test equipment. On-wafer resistors can be fabricated by use of photolithographic patterning of thin metal films such as NiCr or PdAu.

The Wheatstone bridge structure acts as a directional coupler. To see this, it is useful to insert the values for the bridge impedances shown in Fig. 4.4(a) into Equation (4.1):

$$\frac{V_{det}}{V_{osc}} = \frac{1}{2} - \frac{Z_L}{R_{br}+Z_L} \quad . \tag{4.3}$$

If we define the measured reflection coefficient as $\Gamma_M = V_{det}/V_{osc}$ and define the reflection coefficient of the unknown load with respect to a reference impedance $R_{br}$ as $\Gamma_L$, then Equation (4.3) can be rewritten as

$$\Gamma_M = \frac{1}{2}\left(\frac{R_{br}-Z_L}{R_{br}+Z_L}\right) = -\frac{1}{2}\Gamma_L \quad . \tag{4.4}$$

From Equation (4.4), we see that an ideal Wheatstone bridge acts as an impedance transformer. In practice, the actual bridge structure will be non-ideal, but it can be represented with a general, bilinear transform,

$$\Gamma_M = e_{00} + \frac{e_{01}e_{10}\Gamma_L}{1-e_{11}\Gamma_L} \quad , \tag{4.5}$$

where $e_{00}$ is directivity, the product $e_{10}e_{01}$ is tracking, and $e_{11}$ is the port match, as originally introduced in Chapter 2.

Figure 4.4. **Wheatstone bridge for measuring RF nanoelectronic devices**. (a) The bridge has resistors $R_{br}$ in three of the branches and the nanoelectronic device with impedance $Z_L$ in the fourth branch. The voltage supplied by the oscillator is $V_{osc}$ and the voltage measured across the detector is $V_{det}$. (b) A schematic of a direction coupler with coupling factor $\alpha$. (c) A signal flow graph representing a three-term error model for a one-port network. The measured reflection coefficient is $\Gamma_M$, the device reflection coefficient is $\Gamma_L$, and the error terms are $e_{00}$, $e_{10}e_{01}$, and $e_{11}$. Adapted from L. Nougaret, G. Dambrine, S. Lepillett, H. Happy, N. Chimot, and J.-P. Bourgoin, *Appl. Phys. Lett.* **96** (2010) art. no. 042109, with permission from AIP Publishing.

Equation (4.5) can alternatively be introduced by considering Equation (4.3) in several special cases [4]. When the bridge is balanced, $Z_L = R_{br}$ and the detector signal is zero. When a short circuit is present at the unknown arm of the bridge, $Z_L = 0$ and $V_{det}/V_{osc} = ½$. Finally, when an open circuit is present at the unknown arm of the bridge, $1/Z_L = 0$ and $V_{det}/V_{osc} = -½$. These special cases suggest that the bridge structure acts as a directional coupler. An ideal direction coupler is shown in Fig. 4.4(b). Suppose that the unknown load of impedance $Z_L$ and corresponding reflection coefficient $\Gamma_L$ is connected to an ideal directional coupler. The measured output signal $M$ is related to the incident signal $a_1$ and the coupling factor $\alpha$ by:

$$M = a_1 \Gamma_L \alpha \quad . \tag{4.6}$$

Again, the actual bridge structure will be non-ideal, but it can be represented as an equivalent one port network. The ideal coupler shown in Fig. 4(b) can be represented by the signal flow graph shown in Fig. 4.4(c), which is a three-term error model for a one port network. Following the methods summarized in Chapter 2, analysis of the signal flow graph leads directly to Equation (4.5).

As with other one port calibrations, three standards must be measured in order to determine the three error terms. For the Wheatstone bridge-based technique, the three standards are a balanced bridge ($Z_L = Z_{br}$), and open circuit ($1/Z_L = 0$), and a short circuit ($Z_L = 0$), as shown in Fig. 4.5(a). Note that we have used the bridge-balancing impedance $Z_{br}$ in place of the simple resistance $R_{br}$, as the non-ideal fabricated structure may have some non-zero reactance. Values of the error terms $e_{00}$, $e_{10}e_{01}$ and $e_{11}$ can be determined from measurements of these standards by use of Equation (4.5). This technique utilizes a differential measurement to measure each standard as well as any DUT. With a ground signal ground probe connected to the device, two sets of scattering parameters are measured. Two scattering parameters, $S_{p1}$ and $S_{p2}$, are measured with a high impedance probe connected to the bridge, first at point *p1* and then at point *p2*, as labeled on the balanced bridge structure in Fig. 4.5(a). A high impedance probe is used here to minimize its perturbation of the bridge circuit, but the signal from the high impedance probe must be amplified to compensate for the signal attenuation in the probe. The differential measurement is calculated by:

$$\Gamma_M = S_{p1} - S_{p2} \quad . \tag{4.7}$$

Figure 4.5. **Wheatstone bridge standards and carbon nanotube device**. (a) Three standards used in the Wheatstone bridge approach. From left to right: a balanced bridge ($Z_L = Z_{br}$), and open circuit ($1/Z_L = 0$), and a short circuit ($Z_L = 0$). The contact points for the high impedance probe during the differential measurement are indicated in the image of the balanced bridge standard as *p1* and *p2*. The center conductor contact point for the ground-signal-ground probe is indicated by *GSG*. (b) Image of the single-wall CNT device with a schematic of the differential measurement setup. Adapted from L. Nougaret, G. Dambrine, S. Lepillett, H. Happy, N. Chimot, and J.-P. Bourgoin, *Appl. Phys. Lett.* **96** (2010) art. no. 042109, with permission from AIP Publishing.

An example of a single-wall CNT device that has been measured by this approach [4] is shown in Fig. 4.5(b). In this device, an individual, single-wall CNT supported by a silicon oxide layer serves as the nanoscale element in the Wheatstone bridge. Once the CNT device has been measured by use of the differential measurement described above, the impedance of the CNT, $Z_{CNT}$, may be determined from:

$$Z_{CNT} = Z_{brC} \frac{\Gamma_M + 1}{\Gamma_M - 1} \quad , \tag{4.8}$$

provided that the bridge-balancing impedance $Z_{br}$ is known. The impedance $Z_{CNT}$ represents to total impedance of the entire branch of the bridge, including the CNT itself, the contacts to the CNT, and the electrical leads. In order to separate the contributions of the CNT from

those of the contacts and the leads, further measurements as well as modeling and simulation are required.

### 4.4 Empty device approach

Many on-wafer measurement approaches, including the bridge-based method discussed above, require the integration of the nanoscale DUT into a specialized structure that enables the approaches to both measurement and calibration. As a matter of practice, it may not be feasible or efficient to integrate the nanoscale DUT into such a structure. Moreover, if the objective is to develop practical devices such as transistors and amplifiers in a device package, the design, fabrication, and optimization of a separate measurement host structure may be inconvenient. In this case, an alternative calibration approach must be developed to de-embed nanoscale devices from the measurement platform while simultaneously accounting for parasitic reactance in the extreme impedance device. Particularly in the early stages of device development, parasitic coupling in the device such as stray capacitances, may dominate the measured response. Here, we develop a calibration approach that augments established on-wafer calibration algorithms with the measurement of empty devices to account for and estimate parasitic effects. Measurement of an empty device, which is identical to the nanoscale DUT, except for the exclusion of the nanoscale building block, provides a reasonable approach to estimating the magnitude of stray capacitive coupling. The measurement of empty devices in order to estimate stray capacitive effects in nanometer-scale devices is reminiscent of similar approaches that historically were used to deal with stray capacitive coupling in microelectronic devices on Si substrates [6].

Here, we will base our approach on the extension of the multiline thru-reflect-line (TRL) calibration method [7], introduced in Chapter 2. The empty-device approach is more broadly applicable and may also be used with other on-wafer calibration methods. Note that emerging calibration approaches may be more suitable for a given nanoscale DUT or other extreme impedance device, but established methods such as TRL represent a practical starting point. The robustness of established on-wafer calibration methods has been confirmed through inter-laboratory comparisons as well as the development of reference coplanar waveguide calibration artifacts by measurement standards laboratories. By use of such reference samples, one may compare calibrated on-wafer measurements to those performed at the measurement standards laboratories and thus gain confidence in calibration methods and measurements. Further validation of this particular approach through simulation and modeling, as well as in-depth discussion of the limitations of this approach are included in the next chapter.

Consider an individual nanowire that has been integrated into an on-wafer, RF-compatible device (We present a nanowire as the nanoscale device element in this discussion, but it is straightforward to extend it to any nanoscale building block.) One relatively straightforward option is to integrate the nanowire into a CPW [8]. The intrinsic properties of the contacted nanowire are de-embedded from the parasitic, stray capacitive effects as follows. The calibrated scattering parameters of the nanowire device $S^{dev}_{ij}$ ($i$ = 1,2; j = *1,2* where 1 and 2 correspond to ports 1 and 2, respectively) are obtained by use of the multiline TRL technique. Then, the calibrated scattering parameters of an empty, nanowire-free device $S^{gap}_{ij}$ are also measured with the multiline TRL technique. As part of the calibration procedure, the reference planes may be translated as close to the nanowire as needed in

order to remove the response of the host structure from the calibrated measurements. The objective is to isolate the scattering parameters of the nanowire and contacts, $S^{nw}_{ij}$. The response of the nanowire device is modeled as the parasitic coupling across the gap in parallel with the response of the contacted nanowire while the transmission through the empty device is modeled as due purely to parasitic coupling, as illustrated in Fig. 4.6. If the scattering parameters are transformed to an admittance parameter representation, this can be expressed in a simple algebraic form:

$$Y_{ij}^{nw} = Y_{ij}^{dev} - Y_{ij}^{gap} \quad , \tag{4.9}$$

where $Y^{dev}_{ij}$ and $Y^{gap}_{ij}$ are the calibrated measurements of the nanowire and empty device, respectively, transformed to an admittance representation. The intrinsic admittance of the nanowire $Y^{nw}_{ij}$ can subsequently be found by simple algebra. It is important to remember that all of the terms in Equation (4.9) are complex valued. The chosen admittance representation not only leads to the simple algebraic form of Equation (4.9), but also is a natural representation given that nanowires are often represented by equivalent circuits with a pi structure, as we will discuss in Chapters 5 and 6.

Figure 4.6. **Comparison of a two-port nanowire device to an empty reference device.** (a) Conceptual illustration of a nanowire device integrated with a coplanar waveguide (CPW) host structure. (b) Conceptual illustration of an "empty," nanowire-free device. The circuit model of the nanowire device includes the properties of the host structure, the intrinsic admittance of the nanowire $Y^{nw}_{ij}$, and the parasitic capacitance $Y^{gap}_{ij}$. By comparison, the circuit model for the empty device excludes $Y^{nw}_{ij}$. Any supporting structures that are present in the nanowire device, such as the dielectric labeled in (b), must also be present in the empty device. 

Historically, this "empty device approach" was developed by a number of groups pursuing broadband characterization of CNT and nanowire devices [10]. Early work by Li, *et. al.* described the fabrication and one-port broadband measurement of single-walled CNT transistors [11]. Later, Bethoux, *et. al.* introduced a calibration procedure analogous to that described above in order to determine the cutoff frequency of a transistor consisting of a large number of single-wall CNTs [12]. Zhang, et. al. utilized a similar strategy to perform broadband, two-port transmission measurements of multiple CNTs [13]. Researchers at Intel extended two-port measurements to individual and bundled CNTs, placing particular emphasis on the potential application of CNTs as high-frequency interconnects [14]. More recently, Vandenbrouck, *et. al.* employed a similar strategy to perform broadband electrical characterization of a GaN/AlN/AlGaN transistor device [15].

The empty device approach has several limitations. For example, Equation (4.9) implies that the introduction of a nanoscale building block does not substantially alter the parasitic reactance beyond the introduction of a contact impedance. This is not always the case. For example, the welding of a multi-walled CNT into a host structure may alter the parasitic reactance of the host device by damaging or otherwise altering metallization layers in the host structure [16]. Furthermore, care must be taken to ensure that $S^{dev}_{ij}$ and $S^{gap}_{ij}$ are measured under controlled, identical conditions, as the parasitic coupling may depend

sensitively upon a number of experimental variables, including temperature, optical illumination, and exposure to different gas environments. Finally, given that the uncertainties in on-wafer scattering parameter measurements are larger than those for connectorized on-wafer measurements, $Y^{dev}_{ij}$ and $Y^{gap}_{ij}$ may be equivalent within the experimental uncertainty, particularly if the resistance of the nanoscale element is extremely high. An alternative approach is to use modeling to extract an estimate of the effective parasitic capacitance from the measurements of the empty device, which can subsequently be used as an input into a model of the nanoelectronic device, as described in the next chapter.

### 4.5 Fabrication of impedance-matched on-wafer devices

One strategy that has emerged in the development of broadband, nanofiber-based devices is the use of massively parallel arrays of nanofibers. For instance, a massively parallel array of hundreds of single-wall CNTs results in an impedance close to 50 Ω without compromising the highly desirable qualities of CNTs that make them well-suited to RF interconnect and transistor applications [17, 18]. Fig. 4.7 illustrates such an array of single-wall CNTs integrated into a one-port coplanar waveguide (CPW). The 1.2 nm to 1.4 nm diameter CNTs were deposited in solution on the 1 µm gap in a lithographically defined host structure and then aligned by use of dielectrophoresis. After alignment, the CNTs are secured by depositing another lithographically defined layer on top of them. A nanowire density on the order of ten wires per micrometer, yields devices with an impedance close to 50 Ω. For the measurements described in Reference [17], all of the CNTs would be metallic in the ideal case, but in practice the ensemble of tubes included some semiconducting CNTs. Nonetheless, measurements of these massively parallel devices offer insight into the fundamental physics of CNTs at RF, namely that the effects of kinetic inductance are negligible below about 200 GHz (Kinetic inductance will be discussed in further detail in Chapter 5).

Figure 4.7. **50 Ω nanoelectronic device based on a massively parallel array of single-wall carbon nanotubes**. (a) Schematic of an RF probe contacted to the coplanar waveguide host structure. (b) Scanning electron microscope images of the massively parallel array aligned in the gap region (width 100 µm, length 1 µm). (c) An AFM image of several aligned carbon nanotubes. Reprinted from C. Rutherglen, D. Jain, and P. Burke *Appl. Phys. Lett.* **93** (2008), art. no. 083119, with permission from AIP Publishing.

Like the other measurement approaches described here, this approach has its own challenges and trade-offs. For example, if the intended application is a CNT transistor, the CNTs must ideally all be semiconductors. Though this is challenging, recent advances in CNT separation suggest that this is possible. Measurements made with this technique reflect the aggregate behavior of the ensemble of nanofibers. Thus, this technique is not amenable to isolating the properties of individual nanofibers or the contacts to individual nanofibers. However, one can envision using measurements of individual nanoscale building blocks to characterize and optimize single elements and contacts before integrating them into massively-parallel, commercially viable devices that are compatible with bulk manufacturing.

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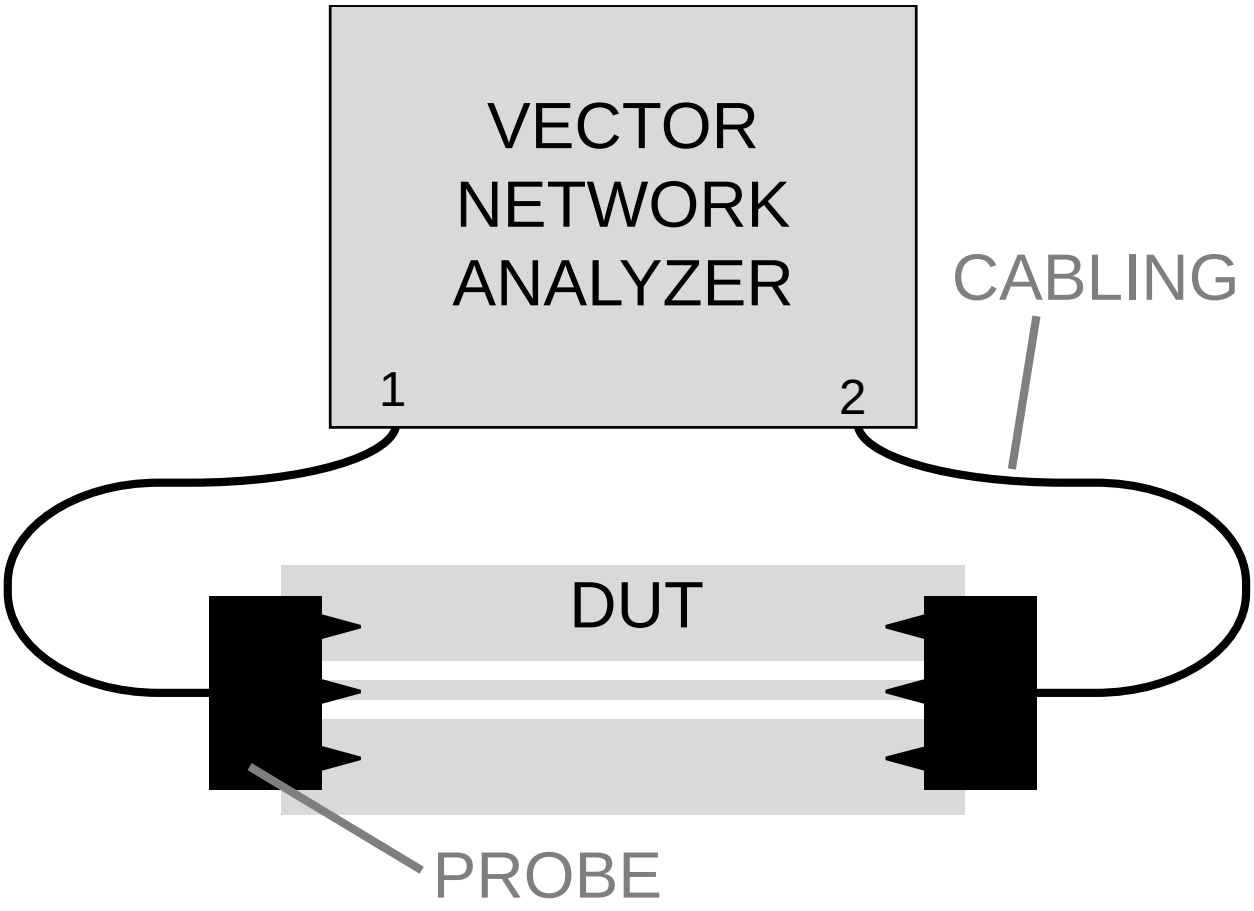



FIGURE 4-1.

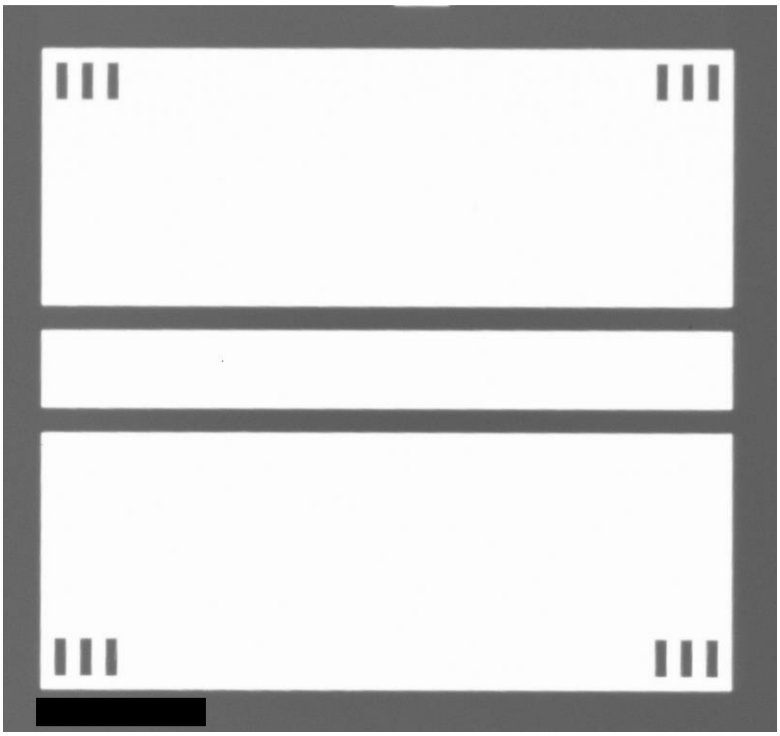
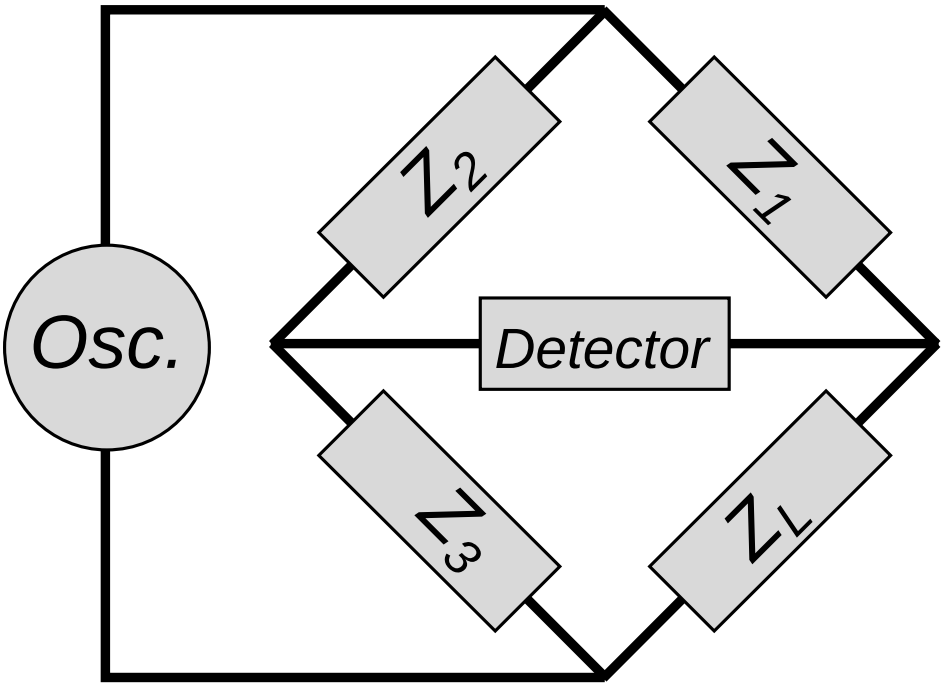


FIGURE 4.2


Osc.
Z2
Z1
Detector
Z3
ZL

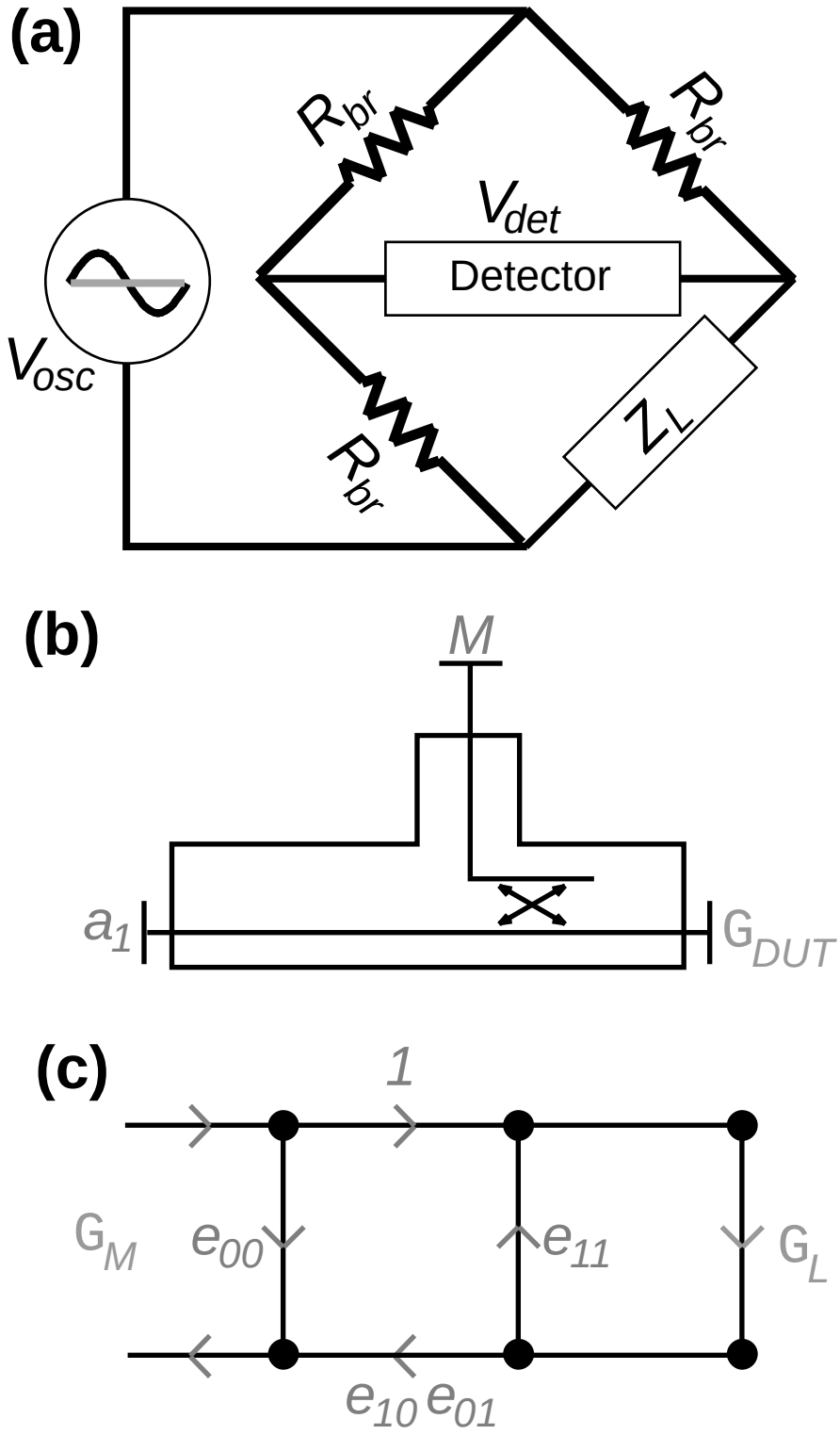
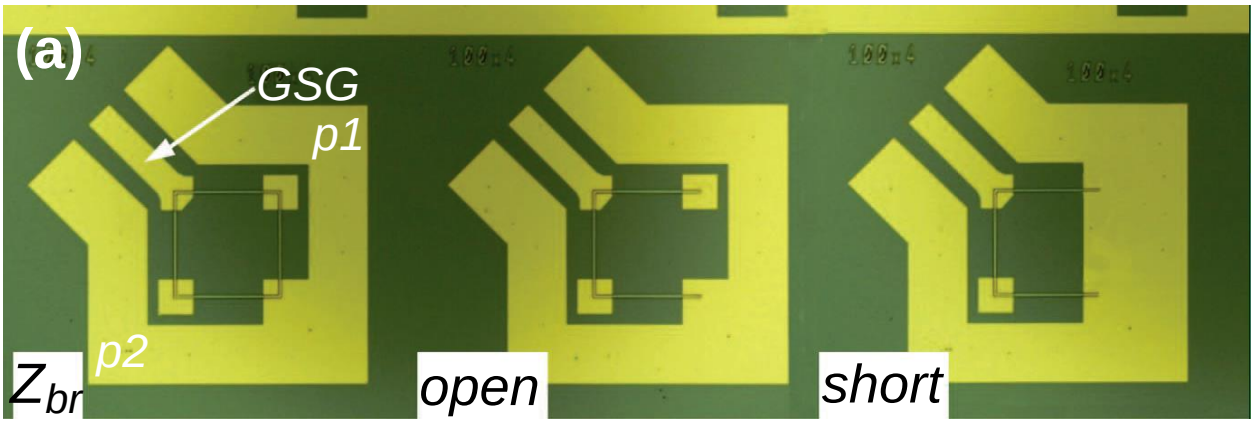
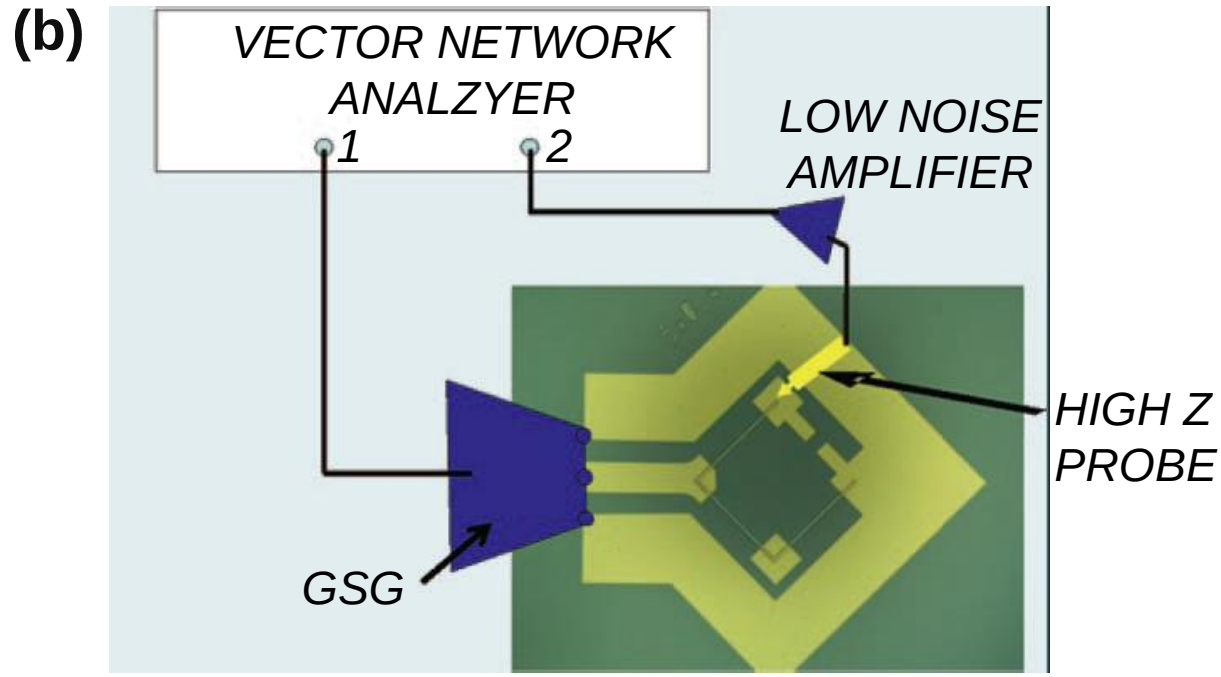

(a)
$R_{br}$
$R_{br}$
$V_{det}$
Detector
$V_{osc}$
$R_{br}$
$Z_L$
(b)
M
$a_1$
$G_{DUT}$
(c)
1
$G_M$
$e_{00}$
$e_{11}$
$G_L$
$e_{10}$
$e_{01}$

FIGURE 4.4


(a)
GSG
p1
p2
$Z_{br}$
open
short


(b)
VECTOR NETWORK ANALZYER
1
2
LOW NOISE AMPLIFIER
HIGH Z PROBE
GSG

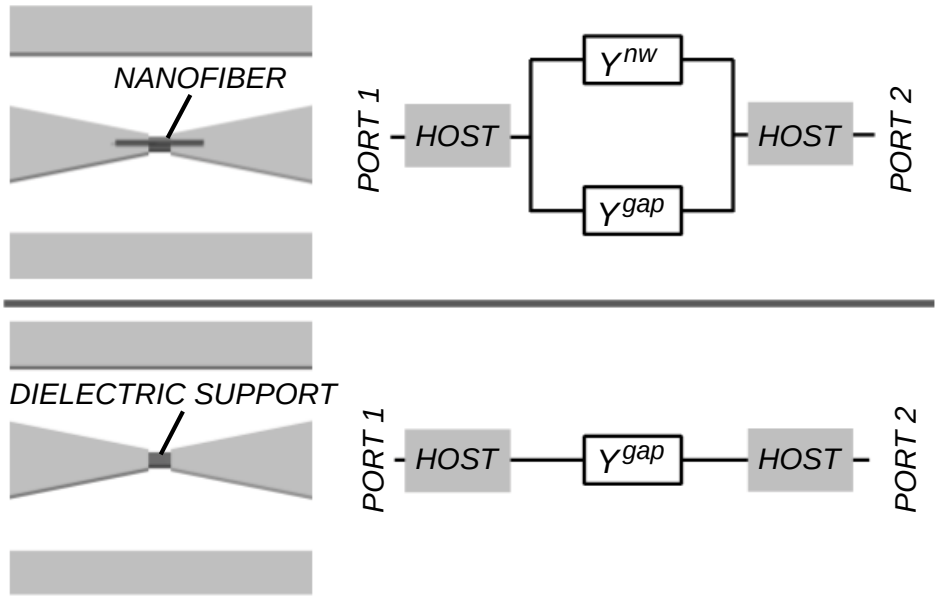

NANOFIBER
PORT 1
HOST
$Y^{nw}$
$Y^{gap}$
HOST
PORT 2
DIELECTRIC SUPPORT
PORT 1
HOST
$Y^{gap}$
HOST
PORT 2

FIGURE 4.6

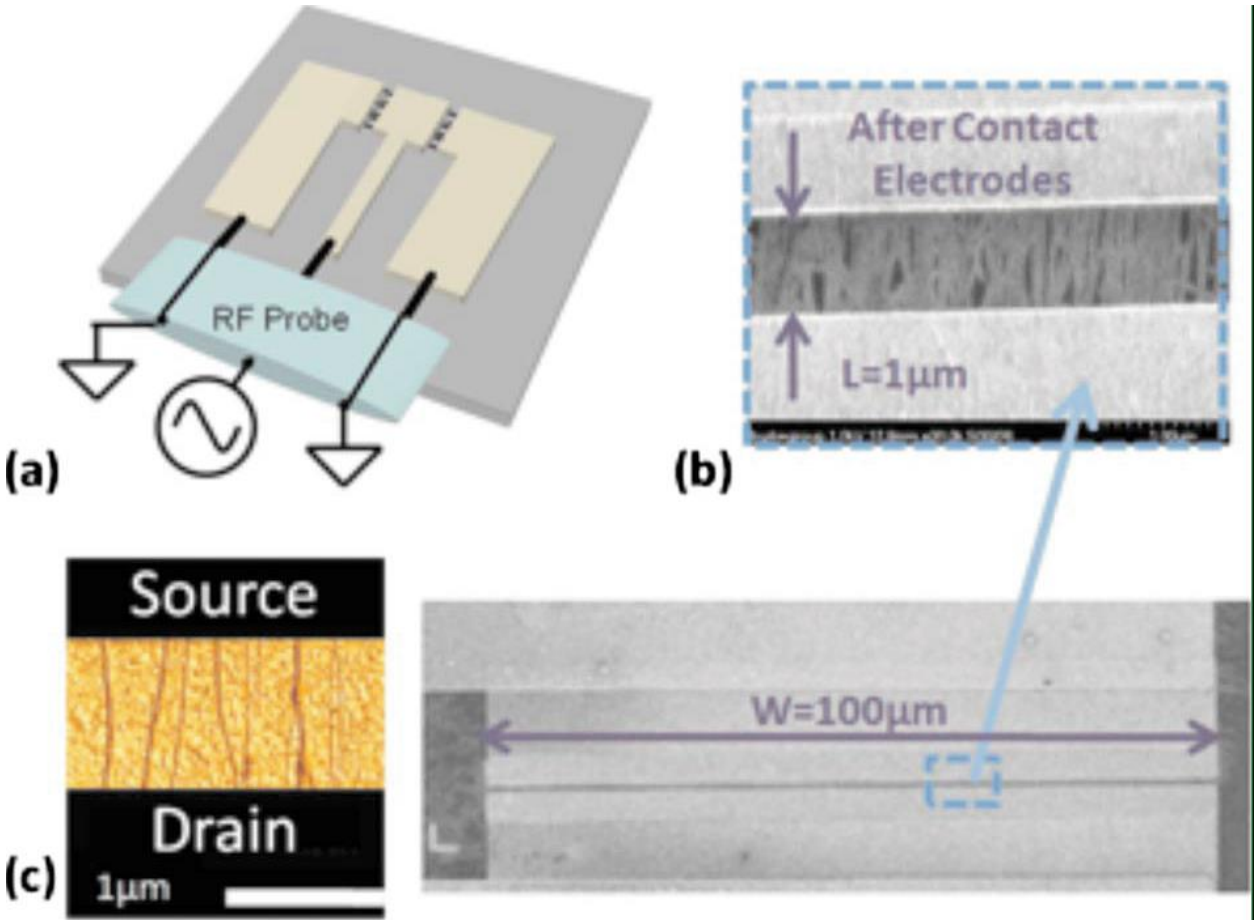

RF Probe
(a)
After Contact
Electrodes
L=1µm
(b)
Source
Drain
1µm
(c)
W=100µm

Figure 4.7