On-Chip Temperature Distribution of Josephson Voltage Standard Devices

Anna E. Fox, Evan B. Golden, Paul D. Dresselhaus, and Samuel P. Benz, *Fellow, IEEE*

***Abstract*—A substrate surface temperature characterization for the National Institute of Standards and Technology Josephson voltage standard has been performed by fabricating and measuring Josephson junction arrays with on-chip thermometry. Circuits were designed with a single voltage standard style array consisting of 12 810 junctions. 31 banks of thermometer junctions were placed around the array and microwave termination resistor to monitor temperature via a junction critical current measurement. Temperature rise in devices with on-chip termination resistors were compared to that of devices terminated off-chip. The thermal profiles on several different substrates were measured and compared to determine which substrate exhibited the best thermal transport. Finally, the thermal properties of junctions deposited directly on silicon were compared to those of the junctions deposited on an interface layer. We found that devices with off-chip terminations had half the temperature rise compared to the devices with on-chip termination, and the devices with remotely located terminations exhibited larger constant-voltage steps over a larger frequency/power range than the devices with termination resistors very close to array junctions. Comparing substrates, we found that sapphire was best for transporting heat from voltage standard circuits and that an interface layer did not affect heat transport in the substrate.**

***Index Terms*—Josephson junctions, Josephson devices, superconducting device fabrication, superconducting integrated circuits.**

I. Introduction

As SUPERCONDUCTING electronic circuits increase in size and complexity, power dissipation needs to be considered as it leads to heating of the cryogenic circuit. Josephson voltage standard devices consist of circuits of damped Josephson junctions and microwave-termination resistors all of which dissipate heat. In order to optimize the performance of a voltage standard circuit, it is necessary for the junctions to be as isothermal as possible in order to maintain the circuit's uniform electrical properties. For example, the NIST programmable Josephson voltage standard (JVS) circuit uses over a quarter of a million superconducting-normal-superconducting (SNS) $Nb/Nb_xSi_{1-x}/Nb$ Josephson junctions to generate a constant-voltage output of 10 V when microwave-biased with an 18.4 GHz signal [1]. A typical power requirement for this JVS circuit is on the order of hundreds of milliwatts of combined microwave and DC bias power. Thermal uniformity of the components in this circuit is critical for the device to produce the largest possible constant-voltage step or operating margin. Additionally, optimizing heat removal from the junctions and resistors is essential for JVS systems operating on liquid cryogen-free cryocoolers [2].

The challenge of sinking heat and maintaining a uniform temperature distribution in a JVS circuit can be examined as a multistep process. The first thermal interface of this system is heat transport from the junction into the substrate, which is understood to be limited by electron–phonon coupling [3]. Once heat is in the substrate it must spread away from the junction and across the substrate, an effect dependent on the substrate thermal conductivity. NIST and other groups making superconducting integrated circuits rely on silicon substrates with thermal oxide or a metal as an interface layer between the junctions and the substrate [4]–[9]. Finally, the heat couples from the substrate to either the liquid He bath or the cryostat cold plate. For voltage standard devices, this final interface has been studied extensively in the context of using cryostats with liquid cryogen-free coolers, and is not discussed here [10]–[12].

In this study, we characterize the thermal uniformity of a JVS circuit and investigate its effect on the operating margins of a JVS array. By use of an SNS junction's temperature dependent critical current (I_c), on-chip thermometry was performed by inferring temperature from the measured I_c of many small banks of junctions placed at various locations around the JVS circuit. Temperature is mapped and steps are measured for JVS arrays with terminations in two on-chip locations, and also off-chip. Heat dissipation is characterized from junction arrays and resistor structures fabricated on three different substrates with three different interface materials, or materials deposited between the junction layer and the substrate. The substrates examined are high purity silicon, ultra-high purity silicon, and sapphire. The interface materials compared are bare silicon, thermal oxide, and aluminum.

II. Device Design

The devices used in this study were specifically designed for on-chip thermometry at locations adjacent to the JVS array. The single JVS array per device consists of 12 810 triple stacked junctions forming the center conductor of a co-planar waveguide (CPW). Microwaves are launched into a 50 Ω transmission line which is tapered to a 20 Ω termination resistor [13]. The CPW center and ground are directly coupled through the termination resistor. Separate low pass filtered voltage and current taps are accessible on both ends of the junction array.

The thermometry structure on each device consists of 31 individually current biased junction banks, each consisting of

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The authors are with the National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: anna.fox@nist.gov; evan.golden@nist.gov; haus@boulder.nist.gov; samuel.benz@nist.gov).

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60 junctions in three-junction stacks. 60 junctions were used in order to provide sufficient voltage signal for reliable I_c measurements while being small enough to be considered a point-like sensor. The thermometry junction banks all share a common voltage measurement connection. The banks are spaced at approximately 500 μm increments around the array and approximately 175 μm from the nearest JVS junction. In addition to the JVS array and the termination resistor as heat sources, each chip has a pair of 250 Ω resistors located on the sides of the chip. Distances from resistors to thermometry junctions ranged from 193 μm to 7.665 mm

In addition to characterizing the on-chip temperature distribution using thermometry junctions, it was important to study the effect of substrate heating on the constant-voltage step. Circuit variations A and B were designed with on-chip termination resistors respectively located 100 μm and 1 mm from the nearest array junction.

In circuit design C, we incorporated a 20 Ω to 50 Ω microwave impedance transformer rather than a 20 Ω on-chip termination resistor. This design allows the remaining microwave bias signal that is not dissipated in the junctions to be terminated off chip; a 50 Ω CPW connects the transformer's 50 Ω output to a microwave launch, which is at the edge of the chip, that is in turn connected to a coaxial cable going to room temperature. The purpose of this design is to measure on-chip heating due only to the junctions, since the remaining microwave bias signal is transmitted and terminated off chip. For all three variants, the thermometry junctions are in similar locations around the JVS array, as are the 250 Ω heaters.

III. Wafer Fabrication

In order to measure heat dissipation for different conditions, test circuits were fabricated on silicon and sapphire with different interfaces, creating many combinations for characterization. Resistivity of the silicon substrates was 10 Ω · cm and greater than 18 000 Ω · cm for the high purity (HP) and the ultra-high purity (UHP) silicon respectively. The surface orientation of the sapphire substrate was c-plane. Wafer thicknesses were 350 μm for the HP and UHP silicon, and 430 μm for the sapphire.

The fabrication process starts with a 76.2 mm diameter wafer substrate. Silicon wafers have either 150 nm of thermally-grown oxide or 5 nm of sputtered aluminum as the interface layer and etch-stop. Sapphire requires no additional etch stop.

The junction barrier material is a co-sputtered Nb_xSi_{1-x} film tuned for current density and resistivity using the ratio of the sputter powers and source deposition rates. The barriers in this study were $4\,\mu m \times 14\,\mu m$ in area and ~ 30 nm thick. These barriers were designed to have a current density, J_c, of $0.2\,mA/\mu m^2$, and a resistivity of approximately 700 $\mu\Omega \cdot$ cm. This results in junctions with an I_c of about 11 mA and a normal-state resistance of approximately 4.5 mΩ. Fabrication of Nb_xSi_{1-x} barriers has been described elsewhere [14]–[16]. When a JVS circuit with an aluminum etch-stop is used, the aluminum that remains following the base electrode etch is removed from the wafer using aluminum etchant. No additional patterning is required for this step.

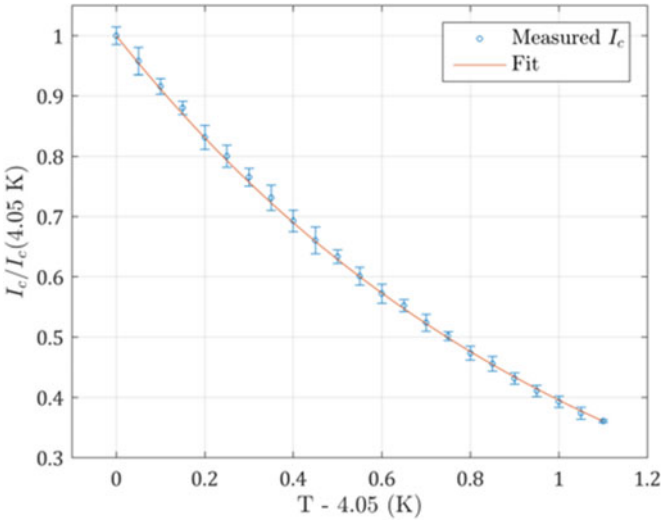

Fig 1. The temperature calibration shows the ratio of I_c at a temperature above bath to the I_c at bath. Fit to the calibration data is shown as the solid line. Measured using an array of 1200 junctions. The functional dependence of the fit is a decaying exponential.

IV. Measurements

All measurements were performed in liquid helium at a bath temperature of 4.05 K using a rapid circuit testing dip probe with two microwave coaxial lines. Methodology used to measure temperatures relied on a four-wire I_c measurement of the thermometer junction using a current source and a nanovoltmeter. The voltage threshold used to determine if the junctions were on a constant-voltage step was set to 10 μV. I_c measurements were performed in series under various heating conditions, and found using a binary search algorithm. These measurements were repeated up to 10 times to assess repeatability. I_c measurements were converted to temperature using a calibration such as the one shown in Fig. 1. The fit applied to this experimental data in Fig. 1 is a decaying exponential.

To account for substrate differences, this calibration was performed on each wafer so that temperature could be calculated from the I_c data. Each calibration sample was measured in liquid helium vapor above the bath temperature of 4.05 K. Temperature was measured using a calibrated silicon thermometer in contact with the sample. Calibration temperatures were collected from the bath temperature to approximately 6 K. A fit to these data were used for calculating temperatures in the heat distribution analysis.

In order to understand the power distribution in the system, the microwave losses of the probe were characterized using a circuit with only a 50 Ω CPW connecting the coaxial input and output. The round-trip probe loss at 18 GHz was measured to be approximately 6 dB.

In order to tabulate the on-chip power distribution, a circuit with an off-chip termination was mounted in the characterized probe and terminated using a 50 Ω resistor at room temperature. The I_c and maximized bias current of the first constant-voltage step at 18 GHz were measured to be 11.5 mA and 4.56 mA respectively, which is 40 % of I_c. Using these microwave bias parameters and a dc current bias at the center of

the first constant-voltage step ($\sim I_c$), input and output powers were measured after compensating for cable loss in the cryoprobe. It was found that approximately 20% of the normalized input power was measured at the room temperature termination, indicating that about 80% of the normalized input microwave power is dissipated in the junction array.

For this particular circuit with 12 810 junctions, maximizing the first constant-voltage step required 13.8 mW input power at the chip, 80% of which, or 11.3 mW is dissipated in the junctions. The remaining 2.5 mW is dissipated in the termination resistor. In addition to microwave dissipation, the junction array also dissipates a DC bias power equal to the bias current multiplied by output voltage. For this example, an additional 5.25 mW of DC bias power is dissipated in the junction array. Aggregating the power, 19 mW of microwave and dc bias power is required to maximize the first constant-voltage step for this circuit.

V. Temperature Mapping

To map the temperature of the circuit around the junction array, a DC current was applied to simulate the heating effects of the microwave input. A power of 19 mW was used as it was calculated in the last section to be a reasonable power required under actual operating conditions. Microwave power is not used for this measurement because there is an undesired microwave coupling between the JVS array and the thermometry junctions that reduces the zero-step current range and is unrelated to heating.

The heat profile was measured in order to compare circuits with different termination resistor locations ($\sim$100 μm, 1 mm, and off-chip). Temperature was measured with power applied as stated above and the resulting temperature rises are shown in Fig. 2. A graphic of the array is superimposed on each figure to represent the array meander location with respect to the thermometer locations, and the termination is shown on the lower right side of figures A and B. Temperature change at each thermometer is plotted on a color map ranging from 50 mK to 500 mK and the trio is plotted on the same color map showing agreement in temperature along the array far from the termination. The circuits with on-chip termination show temperature rise ranging from $\sim$200 mK to 450 mK above bath near the termination. In Fig. 2(a), the widespread effect of its heat dissipation can be observed at distances over 1 mm, well into the area of array junctions. On HP silicon, 1 mm of distance from the heat source yields a temperature rise of just greater than 400 mK. In contrast, the circuit terminated at room temperature has a measured temperature rise ranging from $\sim$200 mK to $\sim$250 mK as a result only of junction dissipation.

Though the junction array dissipates over 80% of the on-chip power, it is clear from a power density calculation why the termination resistor exhibits a hot spot. Comparing the junction and termination areas, the power density of the termination is over 30 times that of the junction array. This indicates that placing the component that produces the greatest power density as far as possible from array junctions results in a more uniform temperature distribution within the array.

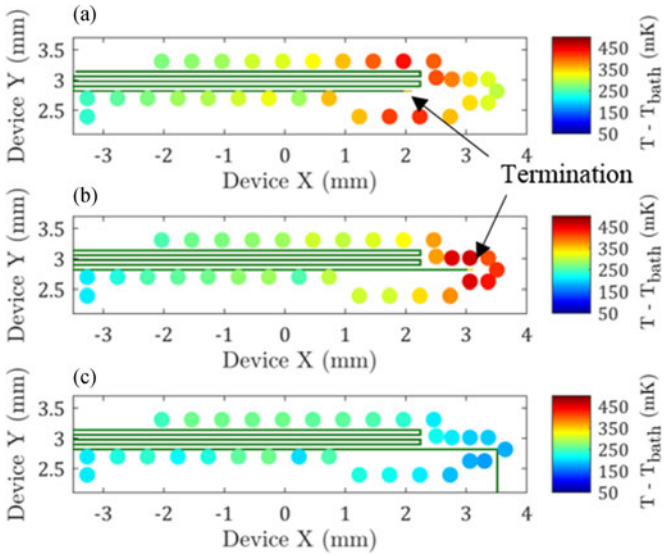

Fig 2. Comparison of devices with on and off-chip termination resistors on HP silicon with 19 mW into the array shown with relative distances to junctions and termination resistor. X and Y axes are device dimensions. Filled circles represent a temperature at an on-chip thermometer. Temperature corresponds to the color map and is shown in millikelvin above T_{bath}. (a) Device with 20 Ω on-chip termination resistor located approximately 100 μm from the nearest array junction. (b) Device with a 20 Ω termination resistor located approximately 1 mm from the nearest array junction. (c) A similar device terminated off-chip.

To measure the effect of heat-induced I_c non-uniformity on a JVS array, constant-voltage steps measured and frequency/power maps were created for these circuits. Fig. 3 shows step size in a color map as a function of input microwave power and frequency where step size is normalized as a percent of I_c. These frequency/power maps show a similarity in microwave properties, as expected from the similar microwave design. These maps also show that by moving the heat source away from the junctions, a larger constant-voltage step is achieved over a larger frequency/power range as a result of the improved temperature and therefore I_c uniformity within the array. Frequency/power maps were also measured for circuits with off-chip termination (not shown). Narrow-band regions of improvement were observed; however, the microwave properties of the system caused degradation of the constant-voltage step at most frequencies, negating any improvement due to improved temperature uniformity of the junctions. Terminating off-chip introduces the opportunity for eliminating an on-chip heat source; however, it is at the cost of microwave complexity.

VI. Substrate Comparison

Temperature profiles were performed using JVS arrays on the different substrates to evaluate temperature rise as a function of distance from the heat source. It is expected that a substrate with higher thermal conductivity will spread heat more effectively. Published values for the thermal conductivity of silicon at 4 K range from ($\sim$20 to $\sim$400) $\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$ depending on the purity [17] while the thermal conductivity of sapphire at 4 K is approximately 100 $\mathrm{W}/(\mathrm{m}\cdot\mathrm{K})$ [18].

Temperature measurements were collected for a common power of 27 mW and plotted as a function of distance from

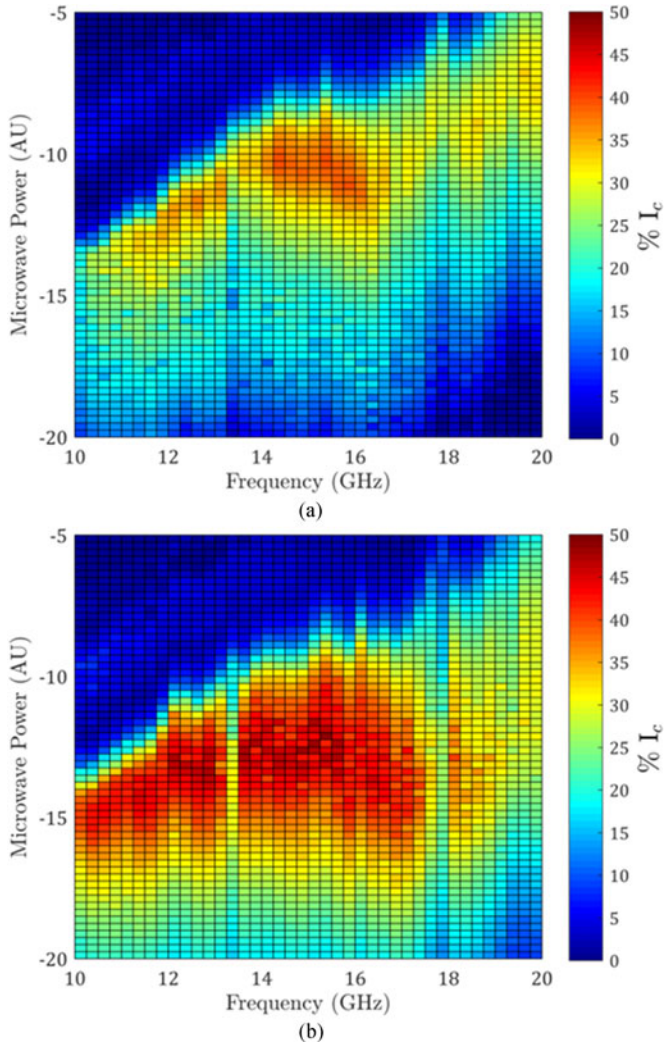

Fig 3. Power versus frequency maps showing constant-voltage step size as a percent of I_c for (a) termination located 100 μm from the nearest array junction and (b) 1 mm from the nearest array junction.

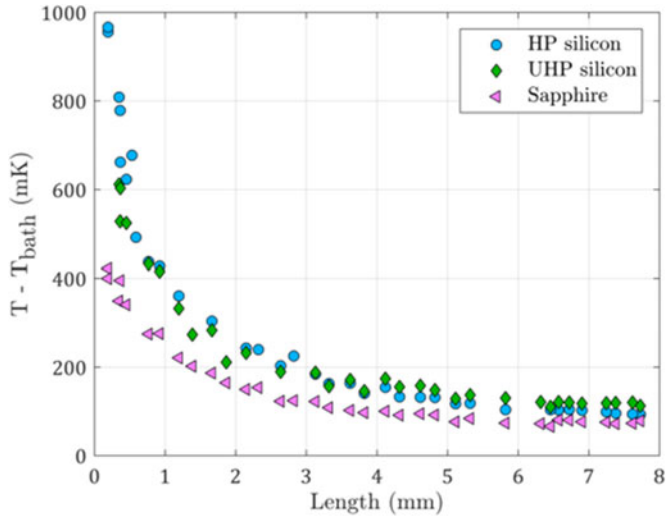

Fig 4. Temperature rise above bath plotted as a function of distance from the heat source for three substrates for a common power. Heat sources are the termination resistor from <1 mm to $\sim$6 mm and the on-chip heater from distances of (6–8) mm. Array junctions were in their zero-state for this measurement.

TABLE I
THERMAL CONDUCTIVITY

Substrate	k (W/(m · K))
HP silicon	88
UHP silicon	132
Sapphire	176

the heat source in Fig. 4. This value of power was the maximum power for which no test structure became normal. For short length scales, the termination resistor was used as a heat source, while for longer lengths the on-chip heater was used. In these measurements, the array junctions were not biased; they were in their zero-state and thus did not dissipate any heat. Multiple measurements for each circuit were collected for the purpose of showing repeatability; temperatures collected had a standard deviation of approximately 5 mK. Assuming two-dimensional heat transport, thermal conductivity was estimated from these measurements using power and an average of distance and temperature gradient. Estimates from these measurements were calculated in order to illustrate the expected upward trend in thermal conductivity with increasing crystal purity and a general agreement with published values. These estimates are summarized in Table 1.

Notable in the data collected is the heat transport difference between substrates at distances less than 1 mm from the heat source. The HP silicon reaches nearly 1 K above the bath temperature close to the heat source while the thermometers on sapphire reach less than half of that. This temperature rise near the heat source in HP silicon is due to an area of less efficient cooling as a result of lower thermal conductivity. Additionally, the HP silicon converges to a cooler temperature, almost that of sapphire, at the farthest distance from the heat source. This observation can be explained simply as less heat spreads at this distance due again to the lower thermal conductivity of the substrate, but this result is within the uncertainty of the measurement.

Between the upper and lower bounds of the HP silicon and the sapphire substrates is the temperature profile of UHP silicon. UHP silicon has fewer defects and higher thermal conductivity than the HP silicon. Thus, UHP silicon exhibits more efficient cooling than the HP silicon, yet still not as efficient as sapphire.

VII. INTERFACE COMPARISON

Studying interface materials, Fig. 5 shows only minor differences between temperature profiles of the three different materials on length scales up to 5 mm. However, other factors may contribute to slight temperature variability, such as wafer-to-wafer and fabrication variations.

Previous work has shown that typically the interface material, whether it is oxide, bare silicon, or metal affects the maximum current a junction can withstand before transitioning into the normal state and trapping flux [3]. Fig. 6 shows junction

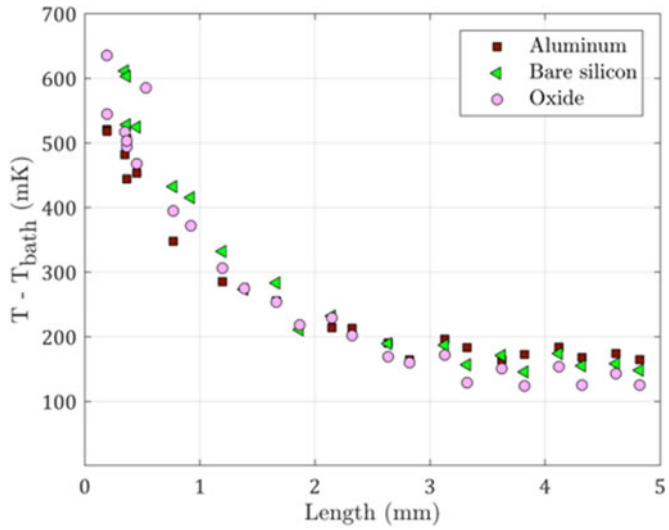

Fig 5. Temperature rise above bath as a function of distance from heat source on devices with different interface materials. All substrates were UHP silicon. Array junctions were in their zero-state for this measurement.

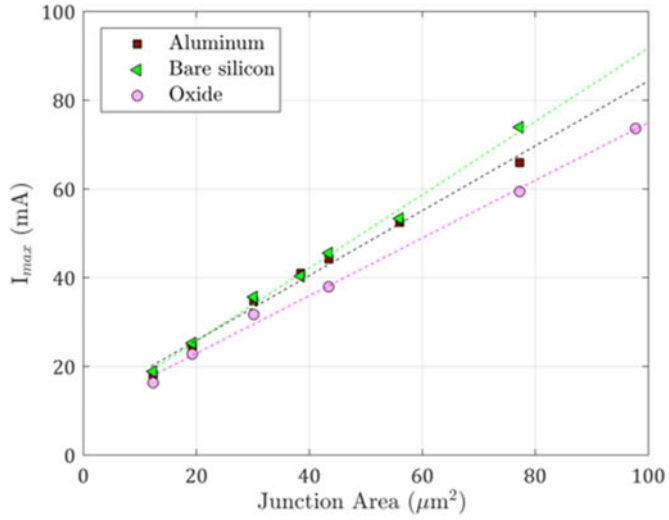

Fig 6. Maximum junction current as a function of junction area. All substrates were UHP silicon.

maximum current measured for the three interface materials and confirms the previous research that shows bare silicon as the best interface for coupling heat into the substrate.

VIII. Conclusions

By characterizing JVS arrays using on-chip thermometry, we find that circuits with off-chip termination resistors have much lower temperature rise compared to circuits with on-chip terminations. After characterizing circuits with termination resistors in two different locations, it was found that locating the hot spot of the termination resistor as far as possible from the array yielded larger constant-voltage step size over a greater frequency/power range. Measuring temperature as a function of distance for several substrates, it was found that sapphire conducts heat better than HP silicon and UHP silicon. Additionally, we confirmed that the choice of interface material does not significantly contribute to the circuit thermal distribution however it does affect maximum junction current. These measurements provide an understanding of the on-chip thermal characteristics of a JVS array and will enable development of more robust voltage standard circuits.

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