Compliance-Free Pulse Forming of Filamentary RRAM

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Despite the overwhelming effort to improve the efficacy of resistive random access memory (RRAM), the underlying physics governing RRAM operation have proven elusive. A survey of the recent literature almost universally indicates that the remaining glaring issues center around variability as well as endurance. The initial filamentary "forming" process is often linked to these problems. This work details our recent efforts to bring the forming process under control and the resulting improvements in RRAM viability in hafnia-based devices. We track the forming process via a "forming energy" metric that allows for filament optimization. By removal of all current compliance elements, and their associated parasitics, a targeted forming energy is achieved using ultrashort voltage pulses. By tailoring the forming energy, we show remarkable endurance window control.

Introduction

Recent memory research has focused on the development of transition metal oxide filamentary resistive random access memories (RRAM) (1, 2). While there are many published accounts detailing resistive switching in a variety of transition metal oxide material systems, hafnia-based systems are seemingly one of the most promising candidates (3, 4). Most explanations of filamentary RRAM involve discussions akin to traditional dielectric breakdown phenomena (5). The application of a relatively large voltage is thought to induce a breakdown event which "forms" a conductive filament through the dielectric region and induces a consequent resistance change. However, unlike dielectric breakdown, the effect in RRAM is not catastrophic. It is commonly observed that limiting the extent of the breakdown event results in a less robust conductive filament. Subsequent bipolar voltage application leads to cyclic dissolution and reforming of this conductive filament. This reversible switching between high and low conductance states defines the RESET and SET state variables of this non-volatile memory. Considering that the initial breakdown (forming event) greatly determines the switching characteristics, a substantial effort has been spent studying this initial electrical forming process (6, 7). A survey of the recent literature almost universally indicates that the remaining glaring RRAM issues center around variability as well as endurance. Perhaps the only consensus in the RRAM community is that the, inherently random, forming process is strongly linked to these variability and subsequent endurance concerns (8).

Experimentally, forming is difficult to control due to the inrush of current associated with a large resistance change. The most common way of controlling the forming process is to introduce a resistive component in series with the RRAM element (9). This series resistance component (via resistor or transistor) introduces a current compliance limit which arrests the forming process by shifting the voltage drop from the RRAM element to the resistive compliance element. Our recent efforts show that even the most careful experimental inclusion of a series resistance element still introduces an unavoidable parasitic capacitance which invokes a serious forming variability (10, 11). During the fast transient forming process, the, often unintentional, parasitic capacitance discharges in an effort to exert a compliance limit. This discharge leads to a current level which briefly exceeds the compliance limit and is often referred to as overshoot (10). The current overshoot greatly alters the ability to terminate forming (i.e., a large current continues to flow through the filament for some uncontrollable time before the compliance element can clamp). This introduces a relatively large uncertainty in the forming energy and consequent variability in the filament (11).

In this work we show that the source of the overshoot variation is strongly linked not only to the overshoot amplitude, but also to the duration of the overshoot (10, 11). Some recent simulations show that the duration of the forming process is linked to the higher overshoot amplitude (6, 12). However, we demonstrate that these two factors (amplitude and duration) are independent by monitoring the effect of the current overshoot duration (fixed overshoot amplitude) on the first RESET current (10, 11). Armed with this knowledge of the compliance-induced overshoot variability we propose a compliance-free forming process which allows for remarkable control of the forming energy via short voltage pulses (picosecond range)(11). This approach allows for an examination of the dissipated energy during the forming and SET/RESET processes and reveals how this energy plays a critical role (11). The SET/RESET cycling endurance of thus formed devices is shown to also be dependent on the SET/RESET energy (11). Multiple-pulse forming is also investigated as a method to further tighten the control of forming energy with promising endurance results (11).

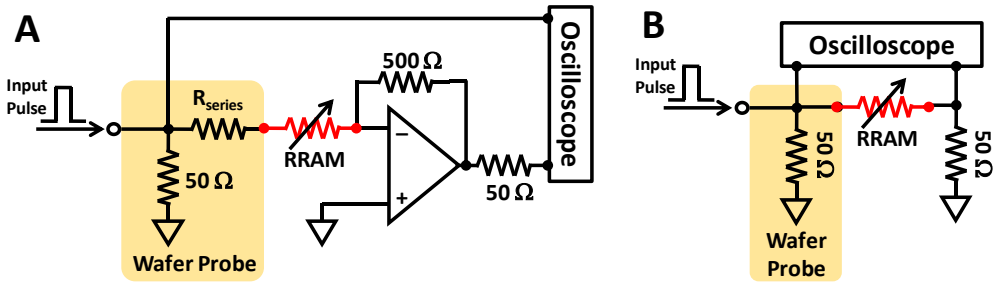

Figure 1. (a) Experimental set-up for forming of RRAM using series resistance for current compliance and a current amplifier to monitor the transient forming current. (b) Experimental setup for ultra-short voltage pulse forming. Note that there is no compliance element. All connections are consistent with proper high speed signal integrity.

Experimental Details

The RRAM devices used in this study consist of TiN/Ti/HfO_2/TiN crossbar stacks (5.8 nm HfO_2). The Ti metal film was deposited on top of the metal oxide to create a sufficient degree of oxygen deficiency in the dielectric, which allows to perform forming at a reasonably low voltage. Both (100 x 100 nm^2 and (50 x 50) nm^2 device geometries were utilized in these studies. In order to better examine the forming process, a variety of experimental approaches are employed.

In an effort to understand the impact of current overshoot we employ an experimental set-up schematically shown in Fig. 1a. In this arrangement, the forming voltage is applied to the device through a series resistance (R_s) compliance element. The current through the device is measured using a fast amplifier capable of sensing current with the resolution of 4 ns (10). The value of the series resistance is chosen to achieve a desirable compliance current during forming. This simple series resistor configuration is sufficient to understand the details of the effects of the overshoot during forming (10). The experimental parasitic capacitance is minimized as much as possible by minimizing signal path lengths. This is mostly accomplished via good signal integrity practices. For these measurements the series resistor is mounted on a PCB (printed circuit board) and placed as close to the device as possible as shown in inset of Fig. 1a. In this arrangement, the vast majority of the parasitic capacitance consists of the pad capacitance of the device (< 50 fF), and the capacitance of the trace connecting the probe to the device (< 0.4 pF). The total parasitic capacitance is thus less than 0.5 pF. Note that these parasitics are far less than that reported in most RRAM experiments. Forming is performed by applying a voltage pulse to the top electrode using a pulse generator. The bottom electrode is held at ground potential through the virtual ground of the current measuring amplifier. The input voltage and the current through the device are recorded using an oscilloscope. After forming, the device is RESET by applying a slow voltage sweep using a parameter analyzer. The maximum RESET current (I_{max}) depends on the size and the resistivity of the formed filament (6). Thus, the obtained I_{max} is taken as an indicator to check for the variations in the formed filaments (10, 11).

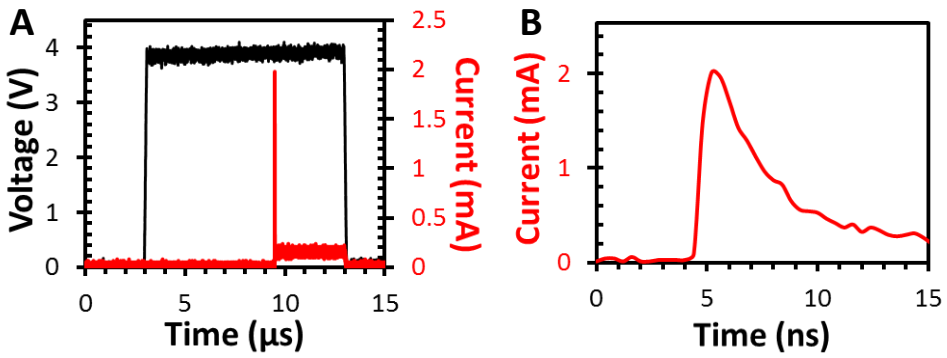

Figure 2. (a) Voltage and current output obtained during forming showing the large current overshoot before the compliance element can clamp. (b) Zoomed in image of the current overshoot in (a) showing that the overshoot lasts for a few ns.

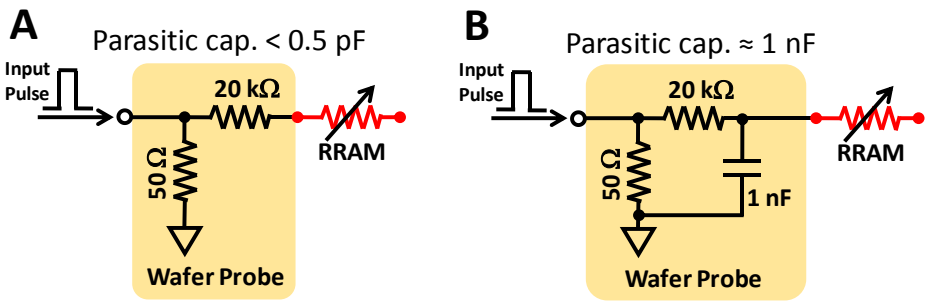

Figure 3. Schematic of our wafer probe used to deliver the forming voltage. The wafer probe consists of a circuit board which can accept the external series resistors (a) and parasitic capacitors (b). The distance between the probe top and the series resistor is < 1 cm. The unavoidable parasitic capacitance in (a) is dominated by the circuit board line capacitance.

In an effort to mitigate current overshoot and explore a means to better control the forming process, a slightly different experimental arrangement is also employed (Fig. 1b) for parts of this study. In this set-up impedance matching and return path control are of critical importance to ensure accurate forming characteristics. Note that there is no current limiting (compliance) element. The 50 Ω termination at the probe provides a fast path to dissipate the charges stored by the parasitic elements, drastically minimizing any overshoot. In this manner, the forming current duration is entirely limited by the pulse duration which is kept very short (ns to ps). In other words, this compliance-free experimental implementation allows the overshoot amplitude to increase in an uncontrolled manner. However, the extent of this overshoot is highly controlled by the pulse duration. All post-forming RESET operations were achieved with a parametric analyzer negative voltage. I_{max} is then noted as a characteristic indicator of the quality of the formed filament.

Results and Discussion

An Examination of the Current Overshoot

Utilizing the experimental set-up in Fig. 1a, a typical input voltage and output current plot obtained during forming is shown in Fig. 2. The current level is very low before the device forms around 2.5 μs. Note the large transient overshoot current at forming followed by a settling to the compliance limited value. This current overshoot during forming is linked to higher I_{max} and likely more filament variability. In an effort to establish the ill-effects of the overshoot due to parasitic capacitance, two experimental variations are employed (Figs. 3a and 3b). The parasitic capacitance in Fig. 3a is (as describe above) experimentally minimized to < 0.5 pF and is mostly comprised of the wafer probe capacitance. Contrastingly, the parasitic capacitance of the second set-up (Fig 3b) is dominated by the addition of a 1 nF external capacitor. This value (1 nF) was chosen to imitate common experimental arrangements (6). For both cases the parasitic capacitance is in parallel to the device. The amplitude of the forming voltage pulse is +4 V for both cases. The width of the forming voltage pulse is 2 μs for first case (<0.5 pF) and 2 ms for the second case (1 nF). The current transient during forming is then plotted for both set-ups as in Figs. 4a and 4b respectively. It can be clearly seen that the time taken to reach the current

compliance for each set-up is quite different. For the first case, the time to compliance is in the range of a few ns, whereas for the 1 nF capacitor it is few µs (1000x longer).

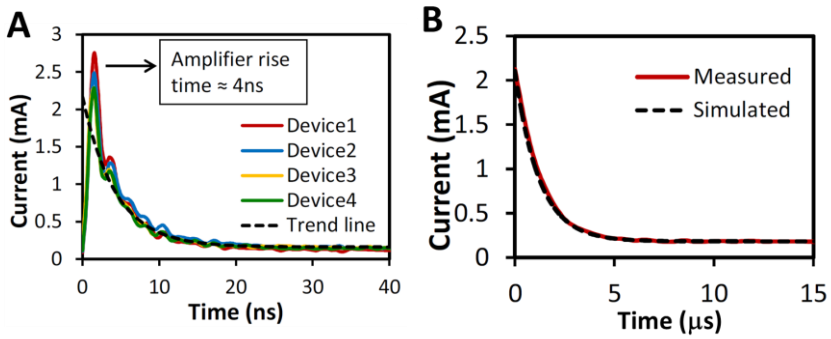

Figure 4. (a) Current transient during forming for the small parasitic capacitance of Fig. 3a and (b) the large 1 nF parasitic external capacitance. Note that the time range in (a) is in ns further demonstrating the very low parasitic capacitance compared to (b) where the time is in the µs range.

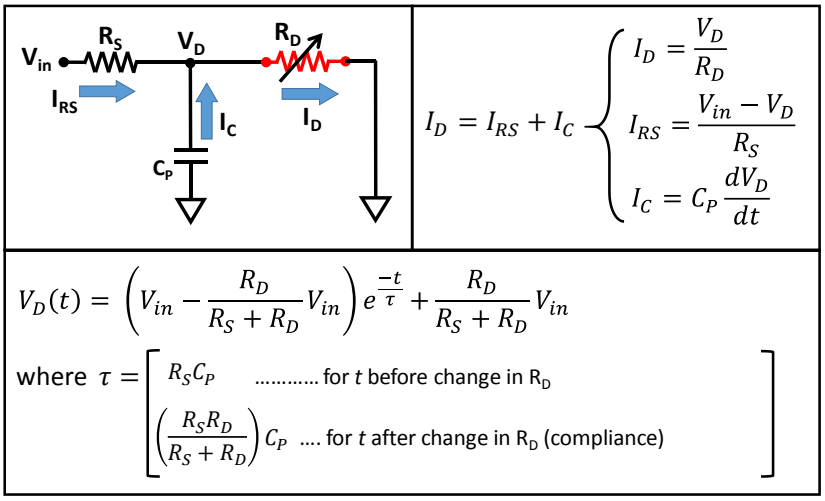

Figure 5. Circuit schematic of the RRAM device (R_D) along with the series resistance (R_S) and parasitic capacitance (C_P) showing the origin of the current overshoot through the device. Also given are the equations for current through the device, I_D, and the voltage across the device, V_D.

The overshoot transients in Fig. 4 illustrate that during forming, the current peaks before it settles to the current compliance level set by the series resistance. The current peaking is due to the charge stored in the parasitic capacitor. A simple circuit schematic of the system is shown in Fig. 5 along with a simple circuit analysis of the current through the device during forming. R_S is the series resistance used to limit current through the device during forming. R_D is the resistance of the device. C_P is the parasitic capacitance. V_{in} and V_D are the input voltage and voltage across the device respectively. When the device is in the high resistance state (R_D > GΩ) all the applied voltage (V_{in}) drops across the device. Therefore, voltage across the device $V_D \approx V_{in}$. When the filament forms, the device changes

to a low resistance state (R_D < 10 kΩ) presumably very fast (t < 130 ps) (11). In this low resistance state, *the voltage across the device, V_D may not decrease at the same rate as the resistance reduction. The rate depends strongly on the size of the parasitic capacitor*. The voltage across the device is given by the equation for $V_D(t)$ in Fig. 5. This is derived by solving the differential equation given by the total current I_D flowing through the device. From the equation for $V_D(t)$, it is clear that larger parasitic capacitance leads to slower discharges and therefore, longer overshoot current duration (bigger RC product in the exponential). This is easily verified via an examination of the current overshoot durations in Fig. 4. The derived equation for $V_D(t)$ was also used to simulate the current through the device. The simulated and measured current overshoots match well (Fig 4b).

Note that the current overshoot amplitude is quite similar for both parasitic capacitance cases. This may seem counterintuitive to recent reports (6, 12). But if the change in the resistance is abrupt such that the rate of change of resistance is faster than the discharge rate of the parasitic capacitance, then the maximum overshoot current is independent of the parasitic capacitance. This is true for both of the cases illustrated in Fig. 4. In the lower parasitic capacitance case, the amplitude of the overshoot current is about 2 mA as shown by the trend line Fig. 4a. The measured data below 4 ns is not reliable due to the amplifier ringing, therefore, we use an extrapolation to estimate the current amplitude. The amplitude given by the trend line in Fig. 4a is similar to that of the higher parasitic capacitance case (1nF shown in Fig. 4b). This result differs from earlier reports linking higher parasitic capacitance to higher overshoot amplitude (6, 12). This is the case only when the change in the resistance is slower compared to the discharge rate of the parasitic capacitance. One such slow change in resistance shown in (6) is similar to progressive breakdown in thin film dielectrics. Such reduced rate in change of resistance during forming was achieved using constant voltage forming (CVF) (6) with very low forming voltages.

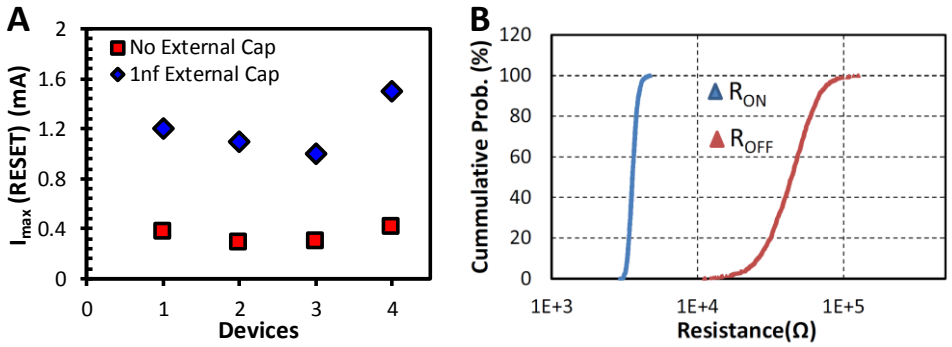

Figure 6. (a) Measured I_{max} required for 1st RESET after forming with and without the 1 nF capacitor. The RESET currents required after forming with 1 nF are higher compared to the devices formed without the 1 nF capacitance. (b) 1000 cycles switching using V_{SET}= 1.5 V with the pulse width of 500 ns and V_{RESET} = -2 V with the pulse width of 250 ns.

Utilizing the two experimental arrangements of Fig. 3, formed devices were subsequently RESET (low resistance to high resistance) by applying a negative voltage using a parameter analyzer (Fig. 6a). This I_{max} is lower for the minimum parasitic capacitance case as compared to the 1 nF capacitance set-up which may indicate the

formation of a filament of a smaller cross-section. After the first RESET, only the devices formed using the lower parasitic capacitance set-up were able to be successively switched between low and high resistance states (Fig. 6b) while the higher capacitance devices simply did not switch (forming was catastrophic).

It is important to note that the peak overshoot currents during forming are similar for both parasitic capacitance cases depicted in Fig 3. However, the duration of the current overshoot is much longer for the 1 nF capacitance forming (Fig 4). This is an indication that the variations in I_{max} in Fig. 6a and device switching capabilities are due to the difference in the duration of the current overshoot, which has been observed to be critical to control the filament properties.

The Forming Energy Paradigm

The demonstrated independence of the magnitude and duration of the current overshoot provides a useful clue towards bringing the forming process under better control. As illustrated in the preceding section, increasing the overshoot duration while maintaining quite similar overshoot amplitudes led to undesirable filaments which were not switchable (high I_{max}). This strongly suggests that the product of the amplitude and duration (or integrated area under the overshoot current curve) is a more apt indicator of the forming process. Further scaling this product with the forming voltage leads to a forming energy metric with which to track the effectiveness of the forming process. The forming energy is taken as the product of the forming voltage, forming current, and time.

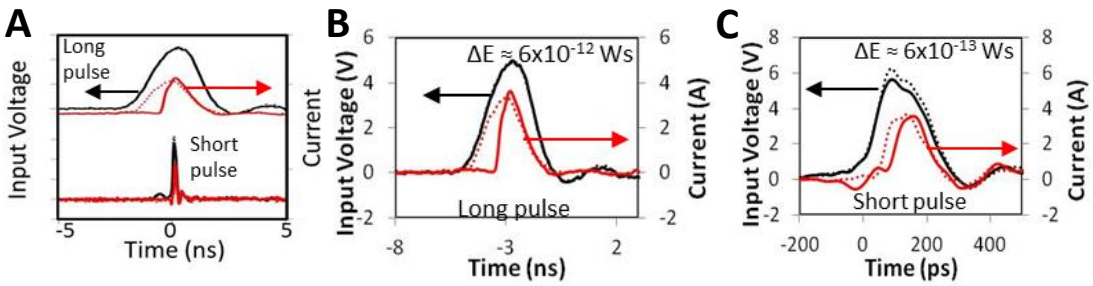

Figure 7. (a) Voltage and current vs. time for forming pulses with pulse durations of 2.5 ns and 130 ps. (b) details the 2.5 ns forming and (c) details the 130 ps forming. The calculated energy difference (ΔE) for dotted (early forming) and the solid line (late forming) are also show. Note that long pulse forming (ΔE) (b) is almost 10x larger than for (c).

Recognition that the inclusion of a compliance element in the RRAM forming process will invariably introduce an unwanted (and uncontrolled) current overshoot might tempt one to suspend all hopes of forming control. However, it is exactly this recognition, coupled with the notion of a forming energy, which allowed us to gain substantially greater control on the forming process. Since there will be an inevitable current overshoot associated with the forming resistance change, then one can limit its duration by minimizing capacitance. In the ultimate incarnation of this approach, one can nearly eliminate the capacitance by also eliminating the compliance element and employing very short voltage pulses (Fig 1b). In this scenario, there is still a current overshoot which proceeds unchecked for the duration of the forming voltage pulse. However, limiting the duration of the forming voltage pulse

limits the duration of the current overshoot and actually provides greater control in targeting a specific forming energy (and consequent I_{max}). One can think of each pulse as providing a quantized portion of the total energy necessary to form. Narrower pulses provide a smaller quanta and therefore improve forming control.

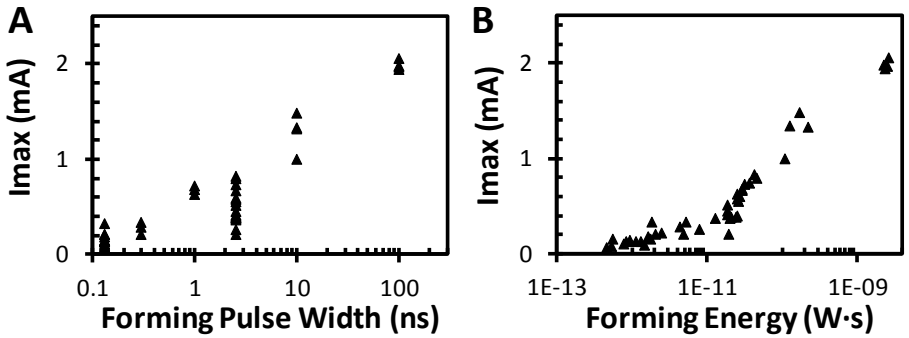

Figure 8. (a) I_{max} current observed after pulsed forming with varying pulse duration. After forming, the devices are RESET using a parametric analyzer. It can be seen that the variation in I_{max} (with same pulse duration) is larger for longer durations. (b) I_{max} versus energy during forming. We observe a much tighter distribution (than in (a)) when the forming energy is carefully monitored.

Compliance-Free Forming

Representative compliance-free forming characteristics are shown in Fig. 7a for both slow (2.5 ns) and fast (130 ps) duration forming pulses. Sometimes forming occurs early in the pulse (Fig. 7 dotted lines), while other times forming occurs later in the pulse (Fig. 7 solid lines). In the case of early forming, the filament is subject to forming current for longer durations. This results in less desirable properties in formed filaments. Note that even in the 2.5 ns pulse duration case, there exists a significant randomness as to when the forming process occurs (within the 2.5 ns pulse). As shown in Fig. 7b for the 2.5 ns pulse case, this randomness of the forming current transient can introduce substantial differences in the forming energy ($\Delta E_{forming} \approx 6.1$ pWs) which results in poorer control of the forming process. However, reducing the pulse duration down to 130 ps greatly minimizes this forming energy randomness (Fig 7c) and brings the forming process into greater control ($\Delta E_{forming} \approx 0.65$ pWs). While the within pulse randomness of the current transient is still present, its impact on the overall forming energy (and presumably filament variability) is greatly reduced. This is best illustrated by comparing the calculated difference between late and early forming for the two pulse cases (2.5 ns and 130 ps). This early/late forming uncertainty introduces almost an order of magnitude more energy uncertainty into the formed filament (Figs 7b and 7c).

One might be tempted to ignore this early/late forming pulse variation and simply look at the product of the pulse duration and forming voltage (Fig 8a). However, proper accounting for the "within-pulse variability" (which was the impetus for forming energy evaluation) is seemingly required to bring the forming process under control. If one presumes that I_{max} is related to forming energy, then proper within-pulse variability accounting, drastically reduces forming variation (Fig. 8b). Fig. 8b also suggests that any chosen I_{max} is attainable via the application of the necessary pulses to net the target forming

energy. In order to trust the forming energy values shown in Fig. 8b, there is a requirement to accurately measure the forming current. At very high speeds, the parasitic current that does not actually flow through the device becomes large (Fig. 9a) and must be removed. We employ a de-embedding procedure to remove these parasitic components from the measured forming current (Fig. 9b) (13). Using this approach, proper forming energies can be extracted.

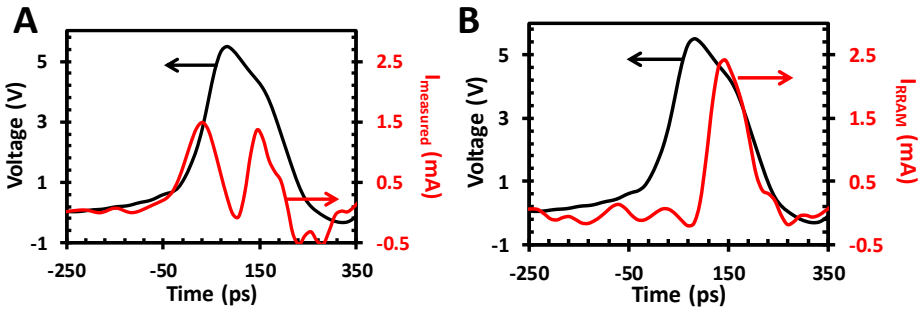

Figure 9. Measured voltage and current pulse before (a) and after (b) de-embedding the parasitic current components. This step is necessary to extract accurate forming energy.

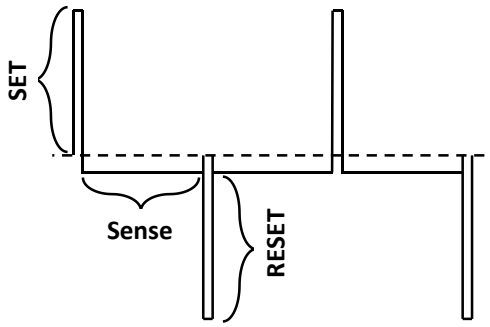

Figure 10. Input pulse train used to analyze the SET/RESET endurance. In this manner every single SET/RESET cycle can be measured.

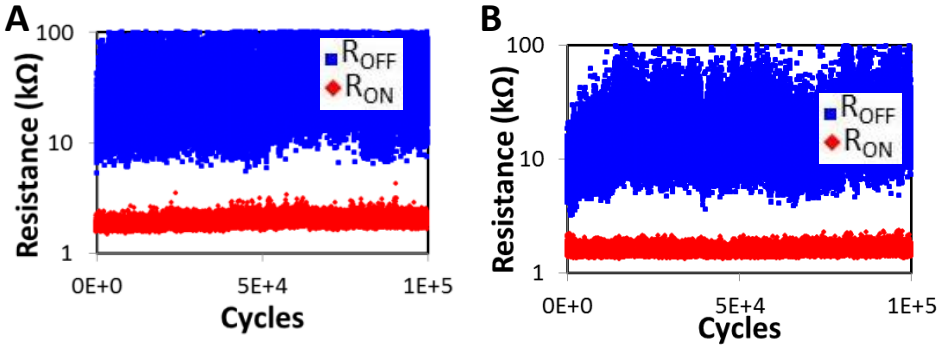

Figure 11. Reliable SET/RESET was obtained on devices formed using a "medium" energy. The switching duration = 2.5 ns and the forming energy was (a) 4.7×10^{-11} Ws (I_{max} = 790 µA, V_{ON} = 1.5 V, V_{OFF} = -2 V) and (b) 2.67×10^{-11} Ws (I_{max} = 550 µA, V_{ON} =2.5 V, V_{OFF} = -2.5 V).

Using forming energy (fig. 8b) as a guide, we investigated the endurance of the pulse formed devices using the input pulse train schematically shown in Fig. 10. Typical SET/RESET operations involve a 2.5 ns pulse of several volts. The RRAM resistance values are sensed at -200 mV. We note that devices with larger forming energies exhibited very poor switching behavior with most devices lasting only a few cycles (not shown). However, as the forming energies and the consequent I_{max} is reduced to 790 μA (Fig. 11a), and then to 550 μA (Fig. 11b), we observe a steady increase of the endurance window and a drastic reduction in SET/RESET switching errors.

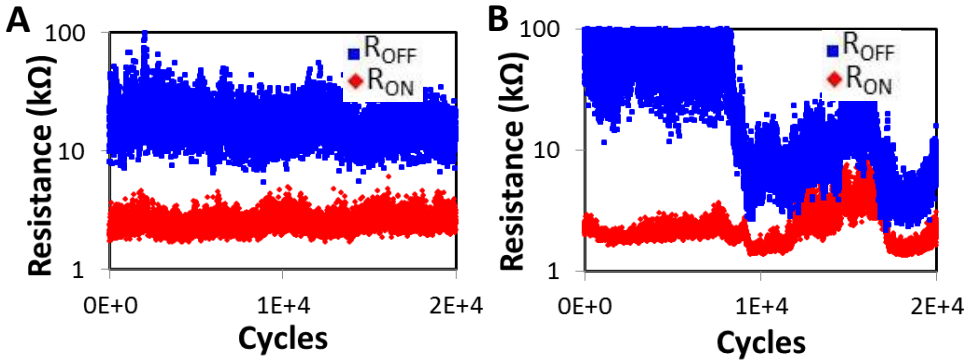

Figure 12. Dependence of cycling reliability on SET/RESET energy is shown by comparing (a) low energy (V_{ON} =1.5 V, V_{OFF} = -2 V, duration = 2.5 ns) and (b) high energy (V_{ON} =2.5 V, V_{OFF} = -2.5 V, , duration = 2.5 ns) SET/RESET.

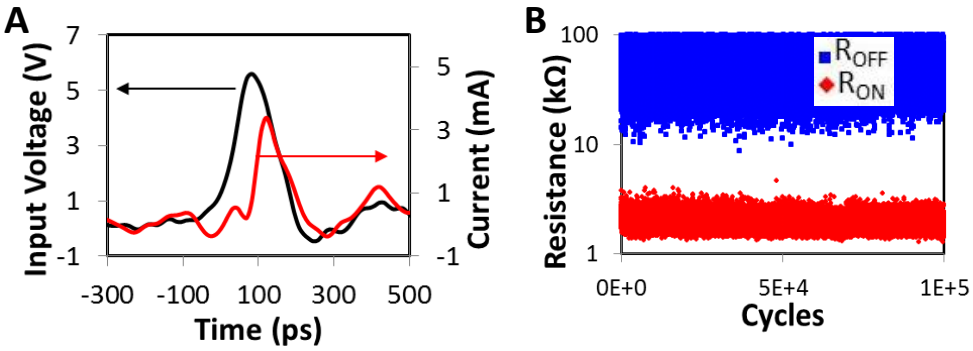

Figure 13. (a) First forming voltage and current plot for multiple pulse forming. After the first pulse shown in (a) 4 additional pulses of the same amplitude and duration were applied to the formed filament. (b) 10^5 SET/RESET cycles for the multiple-pulse forming (V_{ON} =2 V, V_{OFF} = -2 V, duration = 2.5 ns).

Since SET/RESET processes are composed of short pulses, the energy metric is useful here as well. Similar to forming energy, an endurance dependence on the SET/RESET energy (Fig. 12) is also observed. In fig. 12a (I_{max} = 900 μA) a device was switched with lower energies (V_{ON} = 1.5 V, V_{OFF} = -1.5 V, pulse duration = 2.5 ns). In Fig. 12b the same device was switched with higher energies (V_{ON} = 2.5 V, V_{OFF} = -2.5 V, pulse duration = 2.5 ns). It is clear that the higher SET/RESET energy (Fig. 12b) temporarily increases the resistance window markedly, though it comes at the price of lower endurance. This strongly suggests that there is an additional SET/RESET energy influence which is linked to

forming energy (i.e., a filament formed with a specific energy has a SET/RESET energy which complements its switching characteristics).

Even with short pulses, there is still a random forming or SET/RESET timing within the pulse duration. One solution to further tighten the timing, and therefore energy distribution, is to use multiple-pulses for forming. This approach is investigated by first forming the filament using a very short pulse (130 ps) (Fig. 13a) and then subjecting the device to an additional four pulses. The resulting endurance (Fig. 13b) shows a very promising improvement in endurance window. In general, one might be able trade much lower amplitude forming/SET/RESET voltage pulses for the requirement of using multiple pulses to accomplish each step. This could, in principle, allow one to tailor the forming/SET/RESET energies to maximize endurance. This collective line of thinking leads to the notion that the forming step should really be thought of as the last processing fabrication step which defines the identity of the final device.

Conclusions

In this work we have discussed the sources of variability associated with the forming process in RRAM devices and their impact on the endurance window. We have shown that the intentional inclusion of a compliance series resistance unintentionally introduces a parasitic component which leads to current overshoot. This current overshoot was shown to have deleterious effects on the RRAM characteristics and be a significant source of variability. Both the duration and amplitude of this current overshoot are shown to be independent and can each be experimentally treated in different fashions (10). Together, the product of the forming voltage and the duration and amplitude of the current overshoot define a forming energy (11). This forming energy was shown to be strongly correlated to the maximum RESET current, which is an indication of the viability of the formed filament (10, 11). We then introduced a method to completely remove the compliance element from the forming procedure and instead utilize very short voltage pulses to induce a forming event (11). Minimizing the duration of these forming pulses provides greater control of the forming energy and the consequent maximum RESET current. We demonstrated that selecting a target forming energy and pairing this energy with appropriate SET and RESET pulse “energies” leads to improved endurance. Furthermore, this compliance-free forming approach lends itself to multi-pulse forming which shows improved control of the forming energy and a commensurate improvement in endurance (11). Overall, our results strongly suggest that controlling the forming/SET/RESET energy is an effective method to achieve reliable RRAM endurance.

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