PREFACE

A PERSPECTIVE ON NONVOLATILE MAGNETIC MEMORY TECHNOLOGY

As context for this book, computer memory hierarchy ranges from cache (fastest and most expensive) to main memory, to mass storage (slowest and least expensive). Cache memory, immediately accessible by the central processing unit, is usually static random-access memory (SRAM). Main memory is usually dynamic random-access memory (DRAM); like SRAM, it requires power to maintain its memory state, but additionally must be electrically refreshed, typically every 64 ms (1). Mass storage is exemplified by nonvolatile flash memory (of the NAND and NOR varieties) and magnetic hard-disk drives.

Although magnetic random-access memory (MRAM), in particular spin-transfer torque MRAM (STT-MRAM), has the potential to serve as a universal computer memory—cache, main memory, and mass storage—it will likely be most cost-effective as main memory. MRAM is already a commercial product, albeit expensive and of low density relative to DRAM, and several variations of STT-MRAM are in development. Particular interest is in the superior performance of STT-MRAM with perpendicular magnetic anisotropy. Still under research are three-terminal spin–orbit torque MRAM (2,3), which has high endurance and separate paths for read and write current, and voltage-controlled magnetoelectric MRAM (4–7), which has low energy requirements.

More generally, MRAM, the subject of this book, is characterized by nonvolatility, low energy dissipation, high endurance (repeated writing), scalability to advanced (sub-20 nm) technology nodes, compatibility with complementary metal–oxide semiconductor (CMOS) processing, resistance to radiation damage, and short read and write times. The most intriguing of these, nonvolatility and low energy dissipation, are the main drivers of the technology.

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Introduction to Magnetic Random-Access Memory, First Edition. Edited by Bernard Dieny, Ronald B. Goldfarb, and Kyung-Jin Lee.
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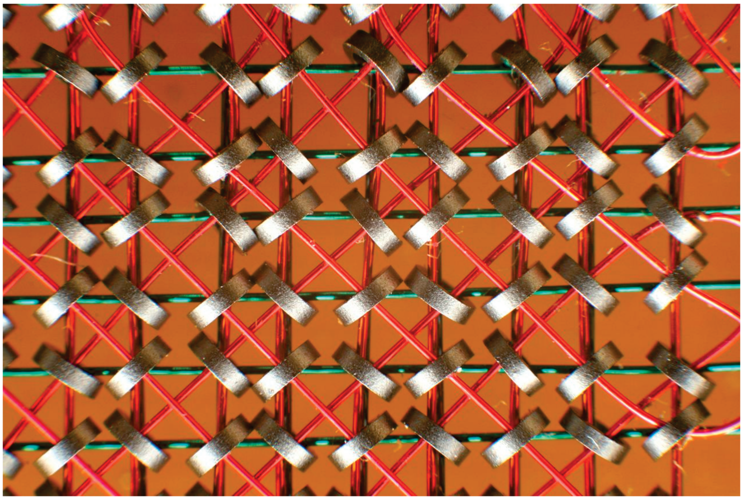


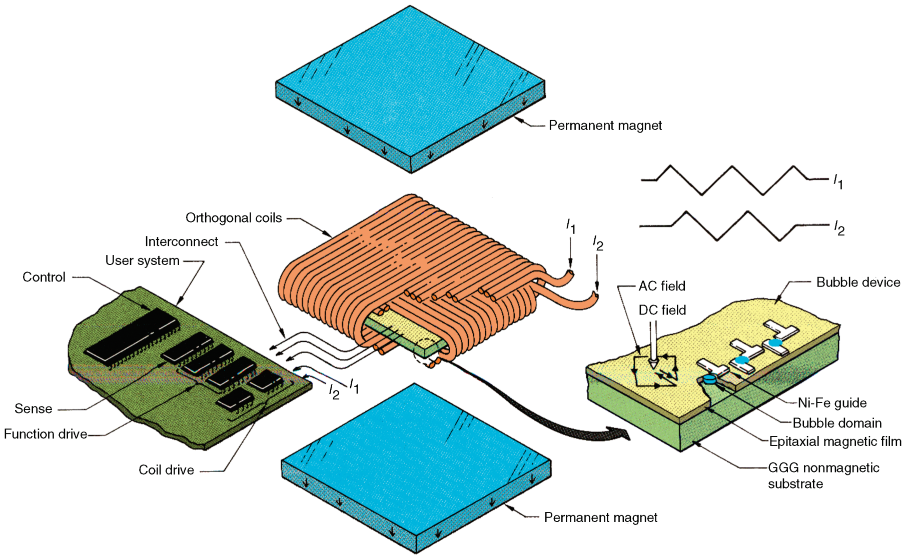
Details of a 1024 bit core plane memory module (11). When magnetic-core memory was introduced in the mid-1950s, toroid cores were about 2 mm in outer diameter.

Nonvolatile MRAM is not really new. It was first developed in the early 1950s by Jay W. Forrester at Massachusetts Institute of Technology (8,9). As envisioned by Forrester, a three-dimensional magnetic-core memory module consisted of circumferentially magnetized toroids strung with *x*-, *y*-, and *z*-plane select wires and a fourth inductively driven output-signal wire. Switching times of the original material studied by Forrester, grain-oriented $Ni_{50}Fe_{50}$ "Deltamax," were on the order of 10 ms. He noted that nonmetallic magnetic ferrites would switch in less than 1 μs based on materials research by William N. Papian (10), and that is how the technology developed. The estimated cost per bit was $1 ($9 today, adjusted for monetary inflation).

Another form of nonvolatile magnetic memory was developed by Andrew H. Bobeck and colleagues at Bell Laboratories in the late 1960s and early 1970s for mass storage: magnetic bubble memory (12,13). It was based on sequential, not random, access. Magnetic bubble domains in synthetic garnets with perpendicular magnetic anisotropy were stabilized by bias fields from permanent magnets. The presence or absence of a bubble—a logic "1" or "0"—was detected with magnetoresistive sensors. Bubbles could be generated, propagated, transferred, replicated, stored, and annihilated. Two orthogonal drive coils provided an in-plane rotating magnetic field to control the magnetization of Ni-Fe bubble-propagation elements (14).

The advent of DRAM in the 1970s, which sacrificed nonvolatility for reduced size, higher speed, and reduced cost, made core memory obsolete for main memory. By the early 1980s, storage density advances and cost reductions in hard-disk drives made bubble memory obsolete for mass storage (although bubble memory continued to be used in military and aerospace applications that required ruggedness).

Besides MRAM, other forms of nonvolatile memory are subjects of intense research. They are based on binary state variables that include "spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states" (15). Mechanisms

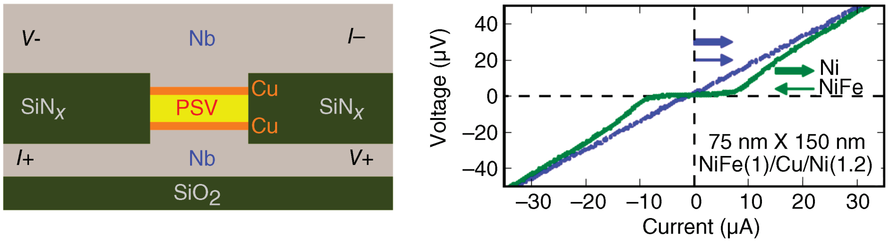


Schematic diagram of the first commercial magnetic bubble memory module, TIB0103, manufactured in 1977 (14). Shown are the bias magnets, drive coils, control and interface circuits, bubble chip, and Ni-Fe "T-bar" bubble-propagation pattern. (An asymmetric chevron pattern was used instead in the TIB0203 in 1978.) The magnetic bubble diameter was 5 µm. The chip had 92,000 bits, a storage density of 155,000 bits/cm^2, an access time of 2–4 ms, and a data transfer rate of 50,000 bits/s.

with great potential include resistive RAM ("memristors") (16) and phase-change RAM (17). One of these may eventually become the dominant technology for cache memory, main memory, or mass storage, but for now, MRAM seems the most promising for main memory. Nevertheless, alternatives to MRAM should not be discounted (18,19).

Coincident with the memory revolution is a rethinking of computer logic and architecture, particularly to address problems of energy consumption in supercomputers and massive data centers. For example, in the United States, the Intelligence Advanced Research Projects Activity (IARPA) has sponsored the development of a prototype cryogenic computer under its "Cryogenic Computing Complexity" program (20). Dramatic reductions are projected in both energy consumption and size (21). Such a computer would combine superconducting, single flux quantum (SFQ) logic with hybrid superconducting/magnetic RAM. Hybrid superconducting/magnetic Josephson junctions switched by spin-transfer torque, resulting in measureable changes in critical current, have been demonstrated (22).

Recent accelerated growth in data centers and their demand for energy are bringing the need for new computer logic and memory to a head. World Wide Web search engines have resorted to storing most of their data in energy-inefficient DRAM (23) because retrieval from mass storage is too slow. There is a need to prototype, test, and benchmark (24) the energy dissipation, high-speed performance, reliability, dimensional scalability, temperature margins, and fabrication reproducibility of MRAM materials, devices, and circuits. Inevitably, new physical phenomena arise as nanostructures shrink in size, and failures will be determined by unknown variables



Nanopillar Josephson junction with a $Ni_{0.8}Fe_{0.2}$/Cu/Ni pseudo-spin valve (PSV) barrier (left) and voltage versus current at 4 K and zero applied field for parallel and antiparallel magnetic states (right) (22).

and the increased relative importance of uncontrolled edge properties with respect to the bulk (25).

This book is designed for microelectronics engineers who need a working knowledge of magnetic memory devices. As conceived by one of the editors, Bernard Dieny, it aims to promote synergy between researchers and developers working in the field of electron devices and those in magnetics and information storage.

The chapters in this volume cover basic concepts in spin electronics (spintronics); magnetic properties of materials; micromagnetic modeling; dynamics of magnetic precession and damping; different implementations of MRAM; the integration of MRAM with CMOS; and future hybrid logic-in-memory architectures.

The authors are leaders in their respective fields. Nicolas Locatelli and Vincent Cros are known for their major contributions in the field of spin torque nano-oscillators and nanodevices assembled in novel computer architectures (26,27). Shinji Yuasa is noted for his pioneering experimental work (28,29) on giant magnetoresistance in magnetic tunnel junctions with MgO barriers (30,31). Liliana Buda-Prejbeanu is expert in micromagnetic modeling and computational magnetics (32). Bill Bailey is an authority on magnetization dynamics and spin–orbit coupling (33). Bernard Dieny is famous for his key role in the discovery of giant magnetoresistance in spin valve structures (34,35). Lucian Prejbeanu is known for his work on thermally assisted MRAM (36). Michael Gaidis is a microwave engineer who has specialized in "back-end-of-line" integration of MRAM with CMOS (37). The chapter on nonvolatile logic-in-memory (38,39) by Takahiro Hanyu, Hideo Ohno, and the team at Tohoku University represents one of the most complete compilations on this topical subject.

This book was sponsored by the IEEE Magnetics Society and published under the Wiley-IEEE Press imprint. The editor at Wiley-IEEE Press was Mary Hatcher.

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