

Device-Level Jitter as a Probe of Ultrafast Traps in High-k MOSFETs

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Abstract—A methodology for the evaluation of ultra-fast interfacial traps, using jitter measurements as a probe, is developed. This methodology is applied to study the effect of PBTI stress on the density of ultra-fast electron traps (with 500 ps to 5 ns characteristic capture/emission times) in a high-k/Si nMOSFET. It is shown, that in spite of an observed increase of timing jitter after PBTI stress, this increase may not be correlated with an increasing density of interface traps. Rather, it is solely caused by a V_T shift which simply decreases the output signal amplitude. The results indicate that ultra-fast (presumably interface) traps may not be affected by PBTI stress.

Index Terms—D_{it}, jitter, high-K MOS, Interface characterization.

I. INTRODUCTION

Timing jitter, manifested as a deviation of signal timing edges from their “correct” positions, is always an undesirable factor in electronics and telecommunications as it leads to corruption of signaling intervals. These jitter-induced errors impose limitations on the operating speed of modern integrated circuits. For the case of discrete MOSFETs, charge trapping and detrapping by fast traps is one of the possible origins of jitter. Fig. 1 illustrates the mechanistic description of jitter caused by electron trapping at the defects in the gate dielectric stack.

Previously, we developed a methodology to measure the jitter of a single device at realistic circuit speeds in response to BTI stress [1,2]. In this study, we apply similar techniques to probe fast electron traps (defects in the gate stack) in Si/high-k nMOSFETs. Using this approach, we attribute PBTI-induced

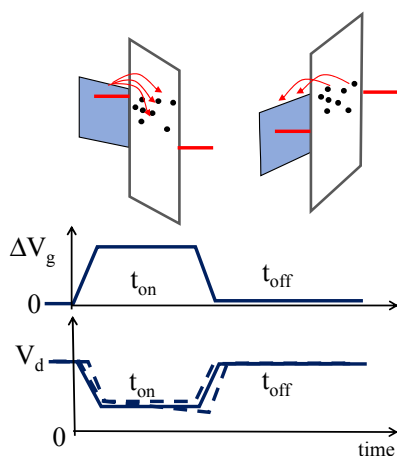


Figure 1. Schematic of trap kinetics during **on** (MOSFET channel is open) and **off** (MOSFET channel is closed) periods of the gate pulse sequence. Different numbers of traps are filled after each t_{on} and t_{off} interval causing V_T variation, and as a result, jitter of the output signal (dashed lines in the bottom panel).

jitter increase to a V_T shift, with seemingly no noticeable generation of fast electron traps in the devices under investigation.

II. EXPERIMENT

The experimental set-up is shown in Fig. 2. High-k/Si nMOSFETs with 2 nm HfO₂/0.8 nm SiO₂ gate stacks were used (30 μm \times 100 nm). A user-defined sequence of ultra-fast pulses with variable widths and intervals between them was applied to the gate terminal of the device under study, while the drain terminal followed by a 50 ohm load resistor was held at constant voltage $V_d \approx 1$ V. The high-speed pattern generator used in the experiment had fixed rise and fall times ≈ 25 ps. Fast rise and fall times are essential for high resolution jitter measurements. The pattern generator clock rate was set to 2 GBit/s, the maximum clock rate at which the device response was not strongly affected by an RC delay (originating from device parasitics). The amplitude of the pulses were chosen to be high enough to open the device during the pulse (**on**-time interval), and to keep the device channel closed in between the pulses (**off**-time interval). The output drain current response was measured using a fast sampling oscilloscope and visualized using an eye diagram representation. Random fluctuations of the number of filled fast traps in the device under study after each **on/off** sequence should cause a variation in the device threshold voltage, and thus, should result in a distribution of transistor turn-**on/off** timing edges – jitter.

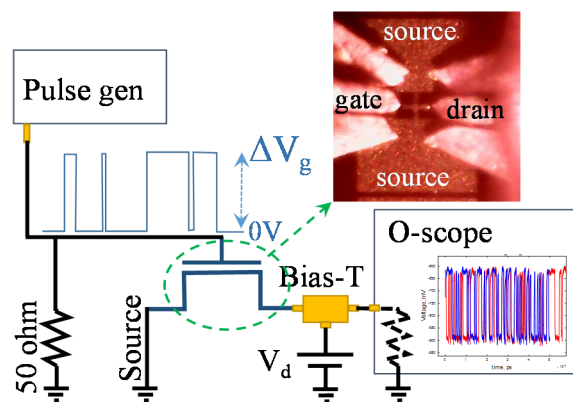


Figure 2. Experimental set-up. Device layout is designed to minimize parasitics. For these devices, the maximum data rate is 2 GBit/s. The experimental system is capable of 20 GBit/s characterizations.

III. RESULTS AND DISCUSSION

It was shown earlier [1,2] that a sequence of pulses of fixed width fired with fixed duty cycle, i.e. a signal pattern generated by a ring oscillator (RO), commonly used for jitter evaluation, does not allow one to conveniently measure stress-related increase of jitter in a MOSFET. Involving numerical Monte Carlo simulations of trap charging/discharging kinetics, we discovered that driving the MOS transistor's gate with a RO pattern would not be an efficient way to produce jitter associated with filling/emptying traps at the oxide/channel interface. To maximize variation of the number of filled traps in the device at the time of each timing edge, it is beneficial to use a pseudo-random input signal pattern. (The details about simulations and results of the evaluation of the method sensitivity will be published elsewhere.) Pseudo-random binary bit sequence (PRBS) is well known in telecommunications [3].

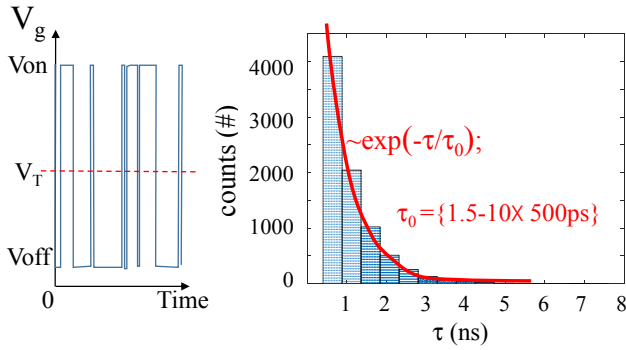


Figure 3. Generated pseudo-random (PRBS) input gate patterns with t_{on} (and t_{off}) following a Poisson distribution. With characteristic time τ_0 ranging from 750 ps to 5 ns to probe different traps through the oxide thickness.

For example, PRBS-15 consists of $2^{15} - 1$ bits, with **on** and **off** bits repeated in a random order, forming t_{on} and t_{off} intervals of random lengths. The distributions of numbers of repeating bits of the same value in the PRBS follow a Poisson distribution. Employing input signal patterns with different characteristic parameter, τ_0 , (see Fig. 3) of the Poisson distribution of τ_{ON} and τ_{OFF} in our experiment, we measured jitter of rising and falling edges of the output signal at different signal levels (Fig. 4). In our experiment, τ_0 was changed in range from 750 ps up to 5 ns and was kept the same for distributions of both t_{on} and t_{off} interval lengths. The length of the pattern (16384 bits) and the number of pattern repetitions (4 times) taken for the jitter analysis is a tradeoff between the desired time resolution, the depth of the available oscilloscope memory, and the number of desired timing edges in the pattern. The latter should be sufficient to obtain statistically significant jitter distributions. It is worth noting that measuring jitter at different signal levels results in higher confidence in analyzing jitter distributions; this approach makes the analysis at least partially immune to any stress induced changes of the shape of the output signal. Note that purposeful variations of the PRBS characteristic times, τ_0 , effectively varies the defect profiling range and can be a useful experimental tool to identify defects contributions to jitter, their characteristic capture and emission times, and location within the oxide stack.

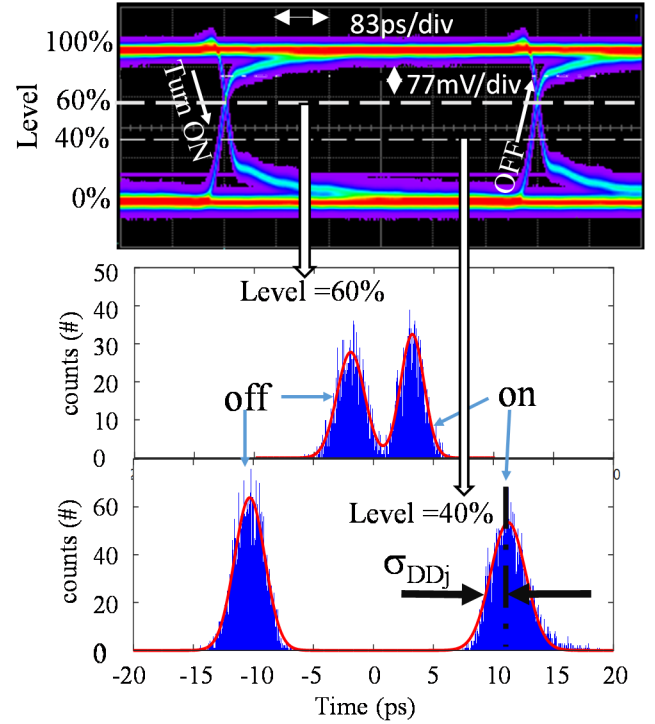


Figure 4. Representative experimental results show an eye diagram representation of the transistor output signal obtained using 2 GBit/s PRBS input signal ($\tau_0 = 750$ ps, $T = 300$ K, $V_{dd} \cong 1.0$ V, and $V_T = 0.3$ V). The bottom panel illustrates the distribution of timing edge positions in the output signal measured at different signal levels for both the rising and falling edges. The dispersion, σ_{DDj} , in each distribution is used as a figure of merit to quantify the jitter.

The described methodology was applied to evaluate the generation of fast electron traps during PBTi stress in a MOSFET with a high-k gate stack. Devices under investigation were stressed at room temperature by applying +1.9 V to the gate while drain, source, and substrate were grounded. The stress was interrupted to perform jitter measurements. In an effort to remove recoverable degradation from consideration, all terminals were held at 0 V for a time period equal to the stress duration prior to each jitter measurement.

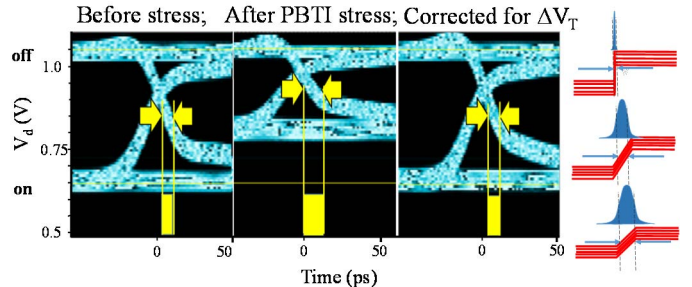


Figure 5. The left panel illustrates the pre- and post-PBTi eye diagrams as measured using a PRBS ($\tau_0 = 750$ ps) input gate waveform. PBTi stress: 4000 s @ $V_{G, stress} = +1.9$ V, $V_d = V_s = V_{sub} = 0$ V, $T = 300$ K). The PBTi induced V_T shift necessarily reduces the output signal amplitude and subsequently increases σ_{DDj} . However, a simple correction of the eye diagram for the V_T shift ($\Delta V_g = \Delta V_{g0} + \Delta V_T$) completely compensates the increase of the timing jitter. The right panel schematically illustrates how a reduction in signal amplitude necessarily causes an increase in measured jitter.

Fig. 5 (right panel) shows representative eye diagrams of the output drain signal before and after stress, obtained using a PRBS gate pattern with $\tau_0 = 750$ ps. The stress introduces the expected increase in jitter of both the **on** and **off** timing edges.

However, more detailed analysis did not relate the observed increase of the timing jitter with an increase of the interface trap density. After PBTI stress, reduction of the amplitude of the output signal from the MOSFETs under investigation was observed. The increase in measured jitter after stress was attributed to the stress related reduction of the output signal amplitude. The left panel of Fig. 5 schematically illustrates how a reduction in signal amplitude causes an increase in measured jitter. While the experimental rise and fall times of the input gate signal are kept the same, the V_T shift-induced reduction of output amplitude, ΔV_d , causes a reduction of the measured $d\Delta V_d/dt$ slope, and thus, increases jitter. After the amplitude of the input signal was increased to compensate for the stress-induced V_T shift ($\Delta V_g = \Delta V_{g0} + \Delta V_T$), the stress-induced increase of timing jitter, $\Delta\sigma_{DDj} = \sigma_{DDj}(t_{\text{stress}}) - \sigma_{DDj}(0)$, was completely compensated (Fig. 6). I.e. the observed stress induced jitter increase was strongly linked to a more permanent V_T shift and had very little to do with the generation of new fast traps in the device under study.

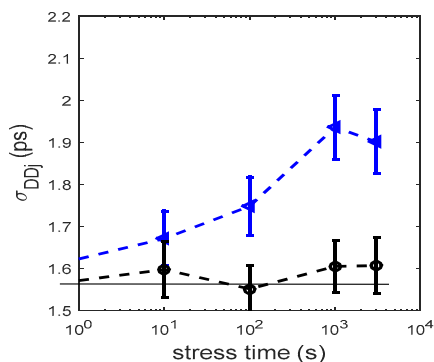


Figure 6. Jitter (σ_{DDj}) of the transistor output signal rising edge vs. PBTI stress time ($V_{\text{stress}} = 1.9$ V, $T = 300$ K). Jitter is measured using a PRBS pattern with $\tau_0 = 4.5$ ns, at the signal level = 50% of the output signal amplitude. The blue dotted line reports the as measured jitter distributions ($\Delta V_G = 1.2$ V). The black line is obtained by correcting for V_T shift after each stress.

We note that this increased jitter derived from the output signal amplitude reduction will impact the device timing and presumably the circuit timing, if introduced into a circuit, regardless of the origin of the increase. However, it is beneficial to know the physical mechanism responsible for the discussed increase of timing jitter during stress, as well as the reversibility of the jitter increase, and its connection with the specific types of defects in the device gate stack.

Pseudo-random bit patterns with different characteristic times, τ_0 , were used in the experiment. If an input signal pattern with a longer τ_0 was used, one would expect to observe a contribution to jitter from larger numbers of traps, including traps located further away from the Si/SiO₂ interface. Fig. 7 shows the measured dependence of σ_{DDj} versus τ_0 before and after stress, and after increasing the input signal amplitude to compensate for the stress-induced increase of the device threshold voltage, V_T . The curves in Fig. 7 show very little

dependence on τ_0 . The seeming independence of jitter versus τ_0 implies that increasing average time intervals (t_{on} and t_{off}) do not necessarily cause an interaction of channel electrons with the larger numbers of traps. This may be an indication that fast traps contributing to jitter at the 2 Gbit/s rate have characteristic response times shorter than 750 ps – the shortest value of τ_0 used in the experiment.

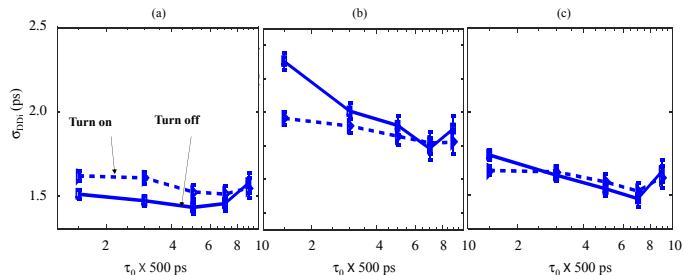


Figure 7. Jitter (σ_{DDj}) of the turn-on (dashed) and turn-off (solid) edges of the transistor output signal vs. the characteristic pattern distribution times (τ_0). These measurements are shown for both 50 % signal level. (a) Before stress. (b) After 4 ks PBTI stress (c) After stress, but corrected for V_T shift. The V_T corrected post PBTI jitter returns to the pre-stress levels.

IV. CONCLUSION

We develop a methodology to quantify ultra-fast (presumably interface) traps using jitter measurements as a probe. This methodology was applied to study the timing impact of PBTI stress in high-k/Si nMOSFETs (500 ps to 5 ns scale). It is shown that PBTI stress does increase the observed jitter, but that this increase is solely caused by a more permanent V_T shift, which decreases the output signal amplitude. More interestingly, our results indicate that PBTI does not cause detectable increase of the density of fast interface traps. This observation is in line with the literature reports stating that, contrarily to NBTI, PBTI stress does not create new fast defects at the Si/SiO₂ interface [4,5].

On the other hand, the evolution of MOSFET technology from SiO₂/poly-Si, to high-k/metal gate, and to III-V/high-k, has seen the level of acceptable interface defect density increase. This functions to enhance the significance of timing jitter moving forward. Thus, augmenting typical reliability data with circuit speed jitter measurements results in more complete understanding to optimize fabrication processes.

The developed methodology can be used for the evaluation of the interface quality and quantification of fast interface traps in MOSFET and HEMT devices, built using different technologies and material systems. It can be used to study the interface degradation induced by different type of stresses, including radiation effects.

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