



Towards Understanding Early Failures Behavior during Device Burn-In: Broadband RF Monitoring of Atomistic Changes in Materials

Yaw S. Obeng,^{a,*} Chukwudi A. Okoro,^{a,b} Papa K. Amoah,^c Johnny Dai,^d and Victor H. Vartanian^e

^aEngineering Physics Division, Physical Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, Maryland 20899, USA

^bTheiss Research, La Jolla, California 92037, USA

^cDepartment of Electrical Engineering, Frostburg State University, Frostburg, Maryland 21532-2303, USA

^dRudolph Technologies Inc., Bud Lake, New Jersey 07828, USA

^eSEMATECH, Albany, New York 12203, USA

In this paper, we attempt to understand the physico-chemical changes that occur in devices during device “burn-in”. We discuss the use of low frequency dielectric spectroscopy to detect, characterize and monitor changes in electrical defects present in the dielectrics of through silicon vias (TSV) for three dimensional (3D) interconnected integrated circuit devices, as the devices are subjected to fluctuating thermal loads. The observed changes in the electrical characteristics of the interconnects were traceable to changes in the chemistry of the isolation dielectric used in the TSV construction. The observed changes provide phenomenological insights into the practice of burn-in. The data also suggest that these “chemical defects” inherent in the ‘as-manufactured’ products may be responsible for some of the unexplained early reliability failures observed in TSV enabled 3D devices.

© The Author(s) 2016. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution 4.0 License (CC BY, <http://creativecommons.org/licenses/by/4.0/>), which permits unrestricted reuse of the work in any medium, provided the original work is properly cited. [DOI: 10.1149/2.0411609jss] All rights reserved.

Manuscript submitted May 26, 2016; revised manuscript received July 8, 2016. Published August 17, 2016. This was Paper 996 from the San Diego, California, Meeting of the Society, May 29–June 2, 2016.

The performance demands of emerging nanoelectronic devices appear to conflict with the need for reliability; they are expected to operate at higher current densities, with lower voltage tolerances and higher electric fields.¹ These performance demands render new devices vulnerable to early failure. Thus, proper tradeoffs in the early design stage are now prerequisites for managing yields. This situation is further complicated by the introduction of new materials and integration schemes, and requires careful failure analyses to find new models for individual failure mechanisms and to identify possible interactions between them. This problem is further exacerbated by the fact that the mechanical and electrical properties of integrated circuits (IC) change during the fabrication process and over time, even in storage, due to the changes in chemistry of the materials of construction.^{2,3} Thus, there is a need for improved performance and material monitoring during and after device fabrication.

Classical models relate reliability to yield by assuming that devices are constructed out of perfectly stable materials, with well-defined and uniform physicochemical properties, and that the same extrinsic defects are responsible for limiting both die and packaged die yields. This implies that early reliability failures are attributable to defects present in the ‘as-fabricated’ devices.¹ In reality, the reliability of electronic devices depends on the materials of construction, integration schemes, thermal history, use conditions, the structures of the devices, and test conditions.² For example, several new failure mechanisms appear when devices are stressed at low voltages (1–3 V range), that are otherwise overshadowed by competing failures mechanisms when the systems are stressed at higher voltages and temperatures usually used for accelerated aging in reliability studies.⁴ Thus, there is a gap between the yield models and the physics of failure of IC devices. Hence, there is the need for effective reliability analyses to determine the dominant fundamental failure modes and their respective mechanisms (i.e., physics of failure), and to predict appropriate device lifetimes. We also need physical insights that would help us to understand, and validate, the assumptions entailed in reliability modeling, as well as test their sensitivities to the evolving materials and the integration schemes used in emerging nanoelectronics.

The reliability of electronic components is frequently described by the instantaneous failure rate or hazard rate, the time evolution of which resembles a ‘bathtub curve’. The ubiquitous bathtub curve represents the idea that the operation of a population of devices is comprised of three distinct periods: (1) an “early failure” (burn-in) period, where the failure rate decreases over time, (2) a “random failure” (useful life) period, where the failure rate is constant over time, and (3) a “wear-out” period, where the failure rate increases over time.⁵ The root cause of wear-out is the thermo-mechanical stresses that develop in the materials of construction and at material interfaces under fluctuating operating temperature profiles. The concept is frequently used in justifying burn-in strategies for improving system reliability.^{3,6,7} However, the value of the bathtub curve in characterizing infant mortalities has been questioned.⁸ The initial decreasing failure rates in the infant mortality region of the bathtub curve assumes some design or manufacturing defects cannot be completely eliminated, resulting in a subpopulation of “weak devices”; the “weak devices” could either die off completely or get stronger under stress. While this explanation of infant mortality is not analytically self-consistent, the bathtub model has historically been used successfully in the semiconductor industry.^{8–10} We need to develop physical evidence-based insights to help bridge the gap between theory and practice of burn-in, and to understand, at least phenomenologically, what happens during post device fabrication burn-in.

The chemistry and physics of materials play crucial roles in determining the reliability of nanoelectronic devices, especially in low voltage devices.¹¹ Low-voltage devices are invariably put together using low temperature processes, such as plasma deposited (PECVD) and sub-atmospheric pressure (SACVD) deposited dielectric films derived from metallorganic precursors.¹² Unfortunately, the low temperature processed materials are metastable from reliability perspectives due to the presence of reactive intermediates and incomplete reactions within the films. These inherent dangling / non-bridging bonds behave as electrical ‘defects’ and limit the utility of such materials in many possible applications.¹³ We recently reported on the changes in the electrical properties of the isolation dielectrics in through silicon vias (TSVs).¹⁴ The changes we observed were reminiscent of the changes in device performance during burn-in, where grossly defective devices are ‘weeded out’, while the recoverable defective “weak sisters” devices are ‘healed’.¹⁵ This apparent correlation motivated us to

*Electrochemical Society Member.

^zE-mail: yaw.obeng@nist.gov

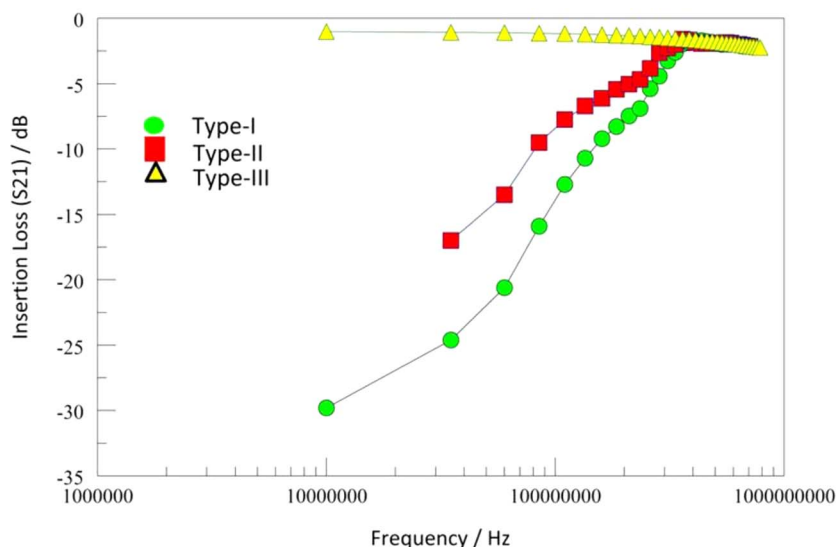


Figure 1. Comparison of the three defect types in the “as received” (zero thermal cycles) material. (Adapted from reference 14).

reexamine our TSV reliability historical data, and to relate the observed physicochemical changes in materials to the early failures and discuss them from the perspectives of the practice of ‘burn-in’ of integrated circuits. In this paper, we use our experimental data to propose an insight into the practice of device ‘burn in’ and to suggest that atomistic chemical transformation of inherent defects in the ‘as-manufactured’ products may be responsible for the success of the ‘bathtub’ modeling of infant mortality in semiconductor devices.¹⁴

Experimental

For this study, SEMATECH (Albany, NY) fabricated TSV-enabled two-level stacked dies, bonded together with benzocyclobutene (BCB)² were used. The TSVs were nominally 5.5 μm in diameter and 50 μm deep and were located at the top chip. The thicknesses of the isolation silicon-oxide liner (HARP, Applied Materials, Santa Clara, CA), and the barrier layer (TaN) were 500 nm and 25 nm, respectively. The details of fabrication are reported elsewhere.¹⁶

The samples were stored at room temperature in a nitrogen-purged enclosure for more than nine months before being used for this study. It is possible that the materials of sample construction (both metal and dielectric) may have undergone some room temperature annealing during storage. So, the observations reported in this work may not reflect all the potential changes possible in freshly fabricated devices. During thermal cycling, the samples were heated from 30°C to 150°C and then cooled to 30°C repeatedly in a nitrogen ambient. The thermal cycling was used to incrementally anneal and induce material changes in the devices.

For FTIR and other spectroscopic measurements, 500 $\pm$ 10 nm thick blanket silicon oxide films were deposited on 300 mm Si wafers, by sub-atmospheric pressure chemical vapor deposition from ozone and tetraethylorthosilicate gas mixtures (SACVD O₃-TEOS, HARP, Applied Materials, Santa Clara, CA).¹⁷ The reported film thickness uniformity is one standard deviation (1- σ) from a 49-points thickness map, with 2 mm edge exclusion. To approximate the thermal history of the ‘as-received’ devices, the blanket wafers were first static annealed at 350°C for 10 minutes under nitrogen before being subjected the thermal cycling. For experimental convenience, we have chosen to focus on samples thermal cycled to 500 cycles in this paper.

Film properties such as thickness, density, modulus, roughness, and phase were measured with picosecond ultrasonic technology (PULSE) (Rudolph Technologies, Bud Lake, NJ).¹⁸ A pump-probe setup in which a 0.1 ps laser pulse (pump) is focused to about 5000 $\times$ 7000 nm² spot onto a wafer surface to create an acoustic wave. The acoustic wave then travels away from the surface through the film. At the interface with another material, a portion of the acoustic

wave is reflected to the surface while the rest is transmitted. When the reflected acoustic wave reaches the wafer surface, it is detected by another focused laser pulse (probe) which was diverted from the pump pulse by the beam splitter. Intrinsic physical properties of the film are calculated from first principles and do not require calibration standards or reference wafers.

For the dielectric spectroscopic studies, changes in the microwave scattering (S-parameters) were measured from 0.5 to 40 GHz using a PNA N5230A vector network analyzer (Keysight, Santa Clara, CA). Measurements were done at intervals of 500 thermal cycles. All measurements were made on devices without electrical bias. The transient insertion losses at the low frequency end of the broadband RF spectrum (below 300 MHz) were used to detect and characterize the response of device under test (DUT).

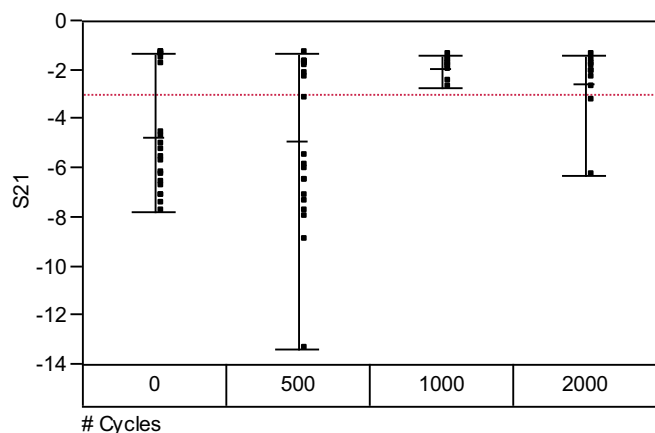
Results

SACVD silicon-oxide films, such as O₃-TEOS, are frequently used as the isolation liner dielectric in high aspect ratio features, such as in TSVs.¹⁷ However, the material reliability of such films are sub-optimal. For example, the time dependent dielectric breakdown (TDDB) lifetime of O₃-TEOS based TSV isolation liner is far below ten years due to the transformation and degradation of the oxide material.¹⁹ The degradation byproducts of water and hydrogen suggest temperature and time driven chemical reactions involving possible condensation reactions of defects, such as silanol.²⁰ The transformation of the dielectric material changes the electrical, and mechanical properties, of the TSV interconnects. We have previously reported on the detection and characterization of such defects in TSV enabled devices. Figure 1 suggests that there are at least three distinct classes of defects in the “as-manufactured” devices we studied. Interestingly, the defect Type-I converts to Type-II with modest thermal treatment. Ultimately, all the defects convert into the Type-III with time, although this step can be accelerated with temperature.¹⁴

Table I compares the characteristic relaxation time of the defects Types-I and -II respectively, with some benchmark values, for bulk pure water²¹ and adsorbed water on nonporous silica.²² The time constants observed in this work are about two orders of magnitude slower than those for the benchmarks, which is reasonable since the three systems are physically different from each other.²³ In the present work we are looking at the non-bridging bonds grafted to the silicon oxide film, whereas Huang et al.²² looked at external water adsorbed on nano-porous silica matrices, and Kaatz²¹ looked at frozen pure water. In the condensed phase, water molecules are associated with each other through weak hydrogen bonds; the molecular rotation relaxation resonance frequencies (e.g., 20 GHz at 25C and 100 Hz at -80 C for

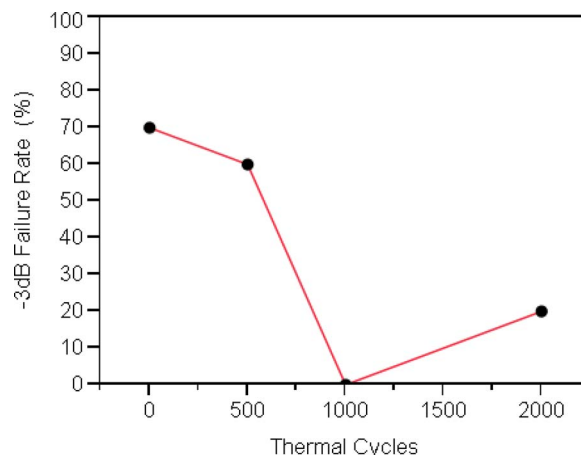
Table I. Comparison of the characteristic relaxation time of the observed defect types in this work with some literature values obtained by terahertz spectroscopy on adsorbed water.

Species	Relaxation Time / s	Reference
Type-I	3.5×10^{-10}	14
Type-II	4.3×10^{-10}	14
Surface adsorbed water on nano-porous silica	4.8×10^{-12}	22
Bulk pure water	8.3×10^{-12}	21

**Figure 2.** Distribution of Insertion losses (S21) at 210 MHz as a function of number of thermal cycles. The horizontal dashed line denotes the -3dB (50% signal loss criterion).

crystalline ice) are indicative of the energy of coordination between the water molecules. In our study, the dangling bonds are not free to rotate, so the major relaxation frequencies are probably due to polarization induced “flip-flop” motions of the dangling bonds in the silicon oxide matrix in response to the rapidly changing electric fields of the microwaves. Thus, it is reasonable to observe slower relaxation of the dangling bond defects in the silicon oxide. Furthermore, a close inspection of Figure 1 reveals multiple slopes, suggesting that the signal loss traces may be actually composites of losses from a variety of defect types, which would be consistent with the wide range of polarizations associated with the multiple chemical environments and interfaces in such a complex matrix.²⁴ In effect, the relaxation time constants for the defects in Table I represent the fastest of the species in each of the defect type categories.

Figure 2 compares the microwave insertion loss (S21) magnitude, at 210 MHz, of a population of 30 ‘as received’ samples and subsequently thermally cycled (i.e., heat treated up to 2000 thermal cycles). In this report, we have arbitrary defined device failure as an insertion loss increase of 3dB, i.e., 50% loss of incident radiation at 210 MHz. Figure 3 shows the fraction of failing dies (expressed as a failing rate) as a function of the number thermal cycles. As we have previously reported, the profiles of the S21 magnitude of the thermally cycled die population were much different from the ‘as-received’ population.¹⁴ The failure rate decreased monotonically with increasing number of thermal cycles, to a minimum at 1000 cycles, and then increased when cycled beyond that. The decreasing number of failing dies with thermal cycling is most likely related to atomistic transformations in the liner dielectric material with heat-treatment. We speculate that these reactions involve the conversion of silanol and silicon-ester defects into siloxane centers.^{20,25} Not all dies in the population studied were transformed into less lossy devices with the thermal cycling; the defects that could not be annealed out (i.e., hard-failed parts) continue to show very large RF signal losses even after extensive thermal treatment. Figure 4 compares the distribution of failed dies in ‘as-received’ and after 500 thermal cycles. Curiously, the “hard-failed” devices were

**Figure 3.** Fraction of Device Population Failing -3dB (50% Insertion losses (S21), at 210 MHz) criterion.

concentrated in the right edge of the wafer. The concentration of “hard-failed” dies suggests that the chemical composition of the local dielectric differs substantially and did not undergo the same atomistic transformation that resulted in improved device performance elsewhere on the wafer.

Indeed, as shown in Figure 5, acoustic impedance measurements on an ‘as-received’ 500 nm thick O_3 -TEOS film show three distinct zones of constant sound velocity. The edge band of acoustic impedance is much wider than the edge exclusion and one standard deviation of the thickness non-uniformity. As we have shown previously, the acoustic impedance, and other physical properties, of TEOS based thin oxide films depend on the local silanol concentration.²⁶ Furthermore, as shown in Figure 6, the FTIR spectra after 500 thermal cycles suggest that quality and chemistry of materials from the right edge and the transition, are different from those from the center zone of Figure 5. While the former exhibit predominantly longitudinal optical (LO-mode) Si-O vibrations, the later exhibits predominantly transverse optical (TO-mode).²⁷ This difference is attributable to the atomistic level structure of the silicon oxide, which depends on the local film deposition details, such as the local substrate temperature and or the composition of the reactant gases over the local area.^{26,28} Furthermore, all three zones show significant amounts of hydrogen-bonded silanol ($\sim 3650\text{--}3200\text{ cm}^{-1}$), as well as surface silanol ($\sim 3759\text{ cm}^{-1}$).²⁸

The microwave energy dissipation from scattering is accompanied by signal attenuation. Figure 7 is a comparison of the microwave attenuation constants^{29,30} in representative ‘as-manufactured’ devices selected from the three zones depicted in Figure 5. The data show distinct differences between the electrical performances of the devices from the center and the edge zones of the wafer. However, the performance of the devices from the transition zone was fluxional, spread around those from the two end zones.

Discussion

The observations that the number of failing dies decreased monotonically with increasing number of thermal cycles, reaching a minimum at 1000 thermal cycles, suggests transformation in the materials of construction. For the simple devices studied in this work, this transformation could be in either the isolation dielectric or in the conducting metal fill of the vias. We believe the changes we describe here, at least at 500 thermal cycles, are more related to changes in the dielectric than to the metal fill, as TSV RF characteristics at low frequency ($< 1\text{ GHz}$), have been shown to be dictated by the capacitance of the isolation liner.³¹ However, we cannot totally discount contributions from the metal fill toward the improved device performance with thermal cycling.³² The changes in the device failure rate with thermal cycling is reminiscent of the changing characteristic product failure distribution with post-processing anneals and after product burn-in. It

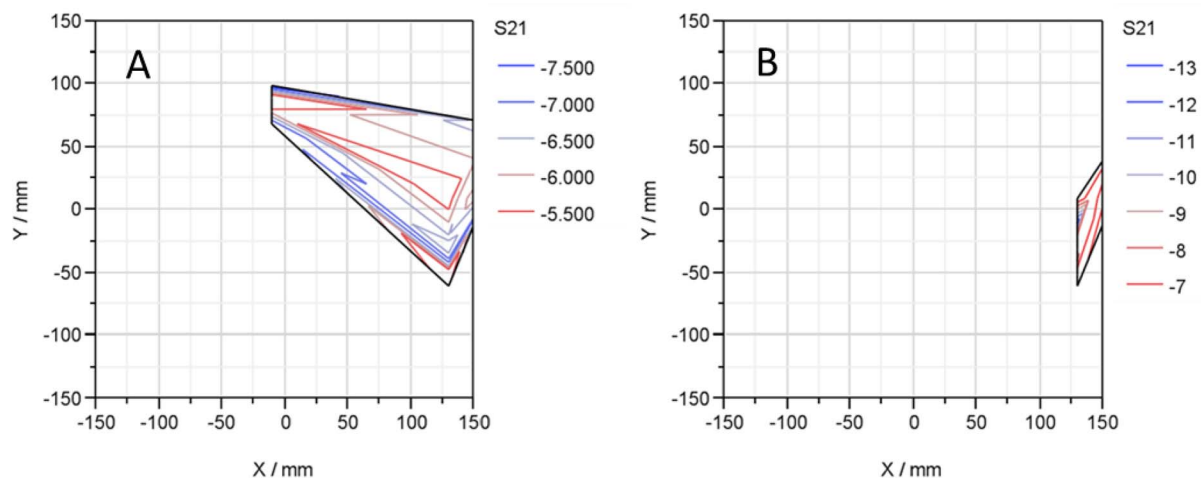


Figure 4. Comparison of the geographic distribution of failed dies in 'as-received' (A) and after 500 thermal cycles dies (B). The failing dies after 500 thermal cycles are concentrated in right edge of the wafer.

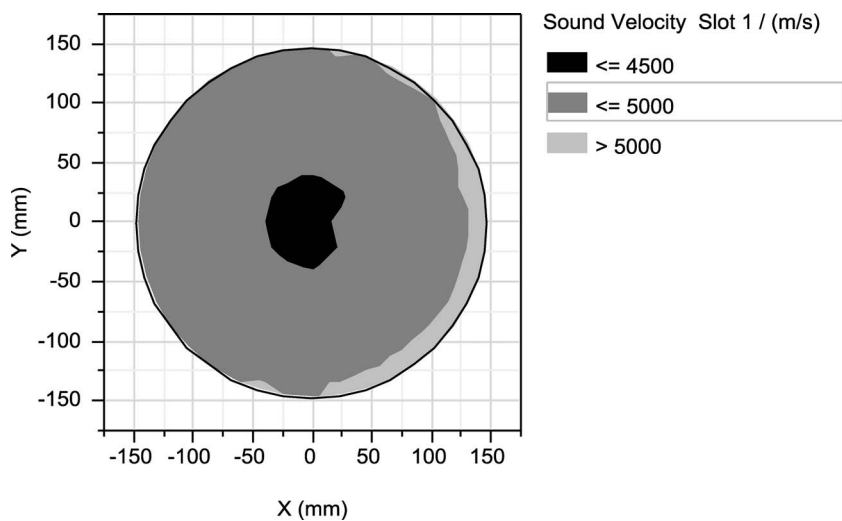


Figure 5. Segmentation of zones of constant sound velocity across a 500 ± 10 nm thick SACVD O₃-TEOS film on a 300 mm silicon wafer.

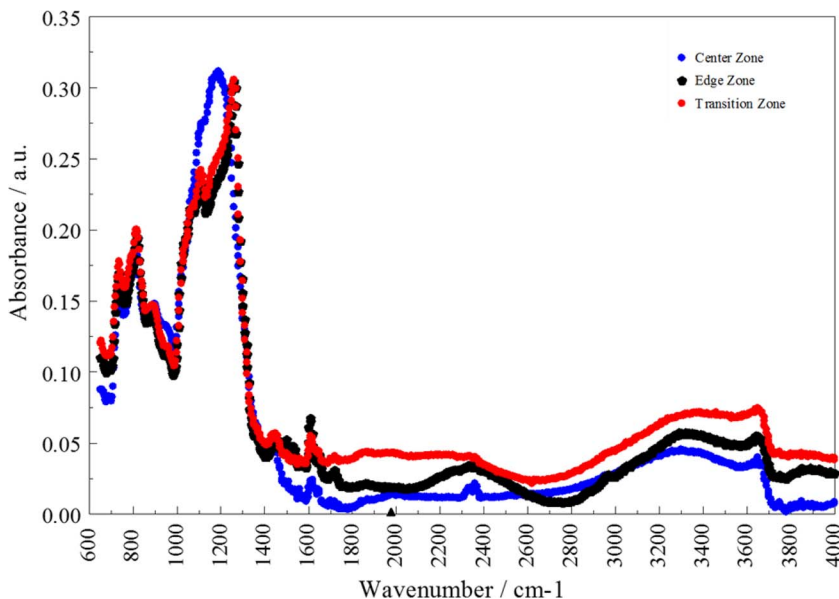


Figure 6. FTIR of blanket 500 nm SACVD O₃-TEOS film after 500 thermal cycles between 30°C and 150°C, following a 10-minute static anneal at 350°C.

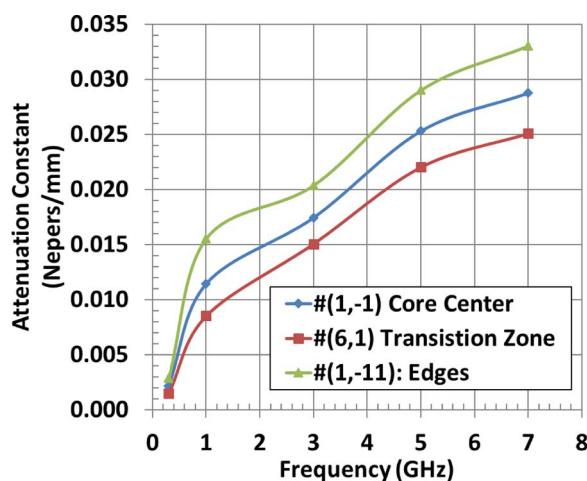


Figure 7. Comparison of the microwave attenuation constants in ‘as-manufactured’ devices selected from the three zones of constant sound velocity shown in Figure 5.

is assumed that during post-processing anneal and burn-in, the chemical bonds within a material strengthen over time, making their failure increasingly unlikely over time. In fact, the shape of Figure 3 fits a mathematical definition of the bathtub curve.³³ The data presented in this work supports atomistic dielectric material transformation with thermal cycling as a contributor to the decreasing initial failure rate.

The RF insertion losses stem from polarization changes due to the reorientation of dangling bonds in the dielectric film. The partially ionic dangling bonds create interfacial polarizations which attempt to align their moment against the rapidly changing applied field, creating orientational polarization.³⁴ This results in ‘flip-flop’ motions in the non-bridging bonds. The dipoles store energy when their moments are antiparallel to the applied electric field (ϵ') and dissipate energy when they are out of phase with the applied electric field (ϵ''). The complex permittivity becomes frequency-dependent when dipoles can no longer stay in-phase with the applied field. At high frequency, dipoles do not get the opportunity to move much before the applied electric field changes orientation, and thus dipoles make insignificant contribution to ϵ' , whereas at low frequency, the dipoles are fully displaced, and their net moment stays antiparallel with the field, resulting in the maximum ϵ' . Between the high and low frequencies exists a relaxation frequency, where the dipoles are maximally out of phase with the applied field, resulting in peak ϵ'' .³⁵

In this work, dipolar relaxation govern the evolution of dielectric properties. Based on FTIR data, we ascribe the Type-I defects to the polarization silanols in the dielectric; and the changes observed after 500 thermal cycles to condensation reactions involving the silanols. When the devices are heated during the thermal cycling, the silanol non-bridging bonds presumably convert to siloxane bridging bonds, thus changing the electrical properties of the liner dielectric. These atomistic reactions remove of the dangling bonds, and thus eliminate the root causes of the energy loss, leading to reduced failure rates. We note that not all the dies in the population studied were transformed into less lossy devices with the thermal cycling, which suggests the dielectric material in the hard-failed area of the wafer did not undergo the same atomistic transformation that resulted in improved device performance.

The samples used in this work were stored at room temperature in a nitrogen-purged enclosure for more than nine months before use. It is possible that the materials of construction (both metal and dielectric) may have undergone some room temperature relaxation or annealing in storage. So, the observations reported in this work may not reflect all the potential changes possible in freshly fabricated devices. Room temperature anneal is improbable at least in the case of the copper fill and interconnect metallization. The Cu metallization in the ‘as-received’ test structures studied here had been stabilized

during fabrication processing flow. The front- and back-side dielectric and etch stop depositions processes exposed the copper fill to heat-treatment of about 2 min at 350°C and 400°C, respectively.³² Furthermore, the completed devices were further annealed at 150°C for at least 1 h.³⁶

The reliability changes we report in this paper could conceivably originate from other materials of construction beside the dielectric. For example, we,^{32,37,38} as well as others,³⁹ have shown that the hydrostatic stress in typical Cu-filled SEMATECH fabricated TSV test structures change overtime, mostly due to changes in Cu grain size with additional post fabrication heating. We have also shown elsewhere that thermal cycling can lead to mechanical damage the SEMATECH fabricated test structures studied in this work.⁴⁰ All these metal stress related changes are expected to be uniform across the wafer and do not show localization, and are different from the regional reliability issues reported in this paper. Besides the Cu, the only other materials in the test devices were dielectrics. As we discuss above the TSV isolation dielectric (SACD O₃-TEOS) change with modest heating as non-bridging bonds condense into bridging bonds.¹⁴ Thus, it is reasonable to argue that the proposed atomistic transformation with thermal cycling that result in the decreasing initial failure rate, involves only to the TSV isolation dielectric material.

Conclusions

We have applied a new way of detecting and characterizing different bond types and defects in dielectrics, based on changes in the low frequency (<300 MHz) dispersion of RF scattering, to gain insights into the changes that occur in O₃-TEOS dielectrics during post processing heat-treatment. The utility of this method was demonstrated in characterizing the atomistic changes in SACVD O₃-TEOS used as an isolation liner in Cu TSVs fabrication during thermal stressing. In summary, the non-bridging / dangling bonds in the “as-processed” film react upon modest heat-treatment to form bridging bonds as a first step in the atomistic processes that result in improved reliability during device burn-in.

Acknowledgment

Helpful discussions with Dr. Martin Green, Dr. Christina Hacker, and Dr. Lin You are acknowledged with sincere thanks.

A contribution from U. S. National Institute of Standards and Technology, not subject to copyright. All views expressed in this paper are those of the authors and of others whom attribution is given and are not necessarily those of NIST nor of any of the institutions cited therein.

Certain commercial equipment, instruments, or materials are identified in this report in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

References

1. R. Muralidhar, T. Shaw, F. Chen, P. Oldiges, D. Edelstein, S. Cohen, R. Achanta, G. Bonilla, and M. Bazant, *Presented at the Reliability Physics Symposium*, 2014 IEEE International, 2014 (unpublished).
2. C. Okoro, P. Kabos, J. Obrzut, K. Hummler, and Y. S. Obeng, *Electron Devices, IEEE Transactions on*, **60**(6), 2015 (2013).
3. Y. S. Obeng, C. A. Okoro, J.-J. Ahn, L. You, and J. J. Kopanski, *ECS Transactions*, **69**(6), 69 (2015).
4. W. Kuo, W.-T. K. Chien, and T. Kim, *Reliability, Yield, and Stress Burn-in: A Unified Approach for Microelectronics Systems Manufacturing & Software Development*. (Springer Science & Business Media, 2013).
5. F. Jensen and N. E. Petersen, *Burn-in: an engineering approach to the design and analysis of burn-in procedures*. (Wiley, 1982).
6. L. You, C. A. Okoro, J.-J. Ahn, J. Kopanski, R. R. Franklin, and Y. S. Obeng, *ECS Journal of Solid State Science and Technology*, **4**(1), N3113 (2015).
7. L. You, C. A. Okoro, J.-J. Ahn, J. J. Kopanski, and Y. S. Obeng, *ECS Transactions*, **61**(6), 113 (2014).
8. G.-A. Klutke, P. C. Kiessler, and M. Wortman, *IEEE Transactions on Reliability*, **52**(1), 125 (2003).
9. H. W. Block and T. H. Savits, *Statistical Science*, **12**(1), 1 (1997).

10. D. Klinger, Y. Nakada, and M. Menendez, (New York, Van Nostrand Reinhold, 1990).
11. J. H. Stathis and D. J. DiMaria, *presented at the Electron Devices Meeting*, 1998. IEDM '98, Technical Digest., International, 1998 (unpublished).
12. A. Boogaard, *Plasma-enhanced chemical vapor deposition of silicon dioxide: optimizing dielectric films through plasma characterization*. (University of Twente, 2011).
13. G. Lucovsky, Y. Wu, H. Niimi, V. Misra, and J. Phillips, *Journal of Vacuum Science and Technology B Microelectronics and Nanometer Structure*, **17**, 1806 (1999).
14. Y. S. Obeng, C. A. Okoro, P. K. Amoah, R. R. Franklin, and P. Kabos, *ECS Journal of Solid State Science and Technology*, **5**(4), P3025 (2016).
15. M. F. Zakaria, Z. A. Kassim, M. P.-L. Ooi, and S. Demidenko, *Design & Test of Computers, IEEE*, **23**(2), 88 (2006).
16. S. Olson and K. Hummler, *presented at the 3D Systems Integration Conference (3DIC)*, 2011 IEEE International, 2012 (unpublished).
17. A. T. Tilke, R. Hampp, C. Stapelmann, M. Culmsee, R. Conti, W. Wille, R. Jaiswal, M. Galiano, and A. Jain, *Presented at the Advanced Semiconductor Manufacturing Conference, 2006. ASMC 2006*. The 17th Annual SEMI/IEEE, 2006 (unpublished).
18. D. Hsieh, T. Tsai, S. Huang, Y. Yang, C. Yang, J. Wu, J. Dai, J. Chen, J. Tan, and P. Mukundhan, *Microelectronic Engineering*, **88**(5), 583 (2011).
19. Y. Li, Y. Oba, C. Wu, S. Van Huylenbroeck, E. Van Besien, G. Vereecke, M. Stucchi, I. De Wolf, G. Beyer, and E. Beyne, *Applied Physics Letters*, **104**(14), 142906 (2014).
20. K. Ramkumar and A. N. Saxena, *Journal of The Electrochemical Society*, **139**(5), 1437 (1992).
21. U. Kaatz, *Journal of Chemical and Engineering Data*, **34**(4), 371 (1989).
22. Y.-R. Huang, K.-H. Liu, C.-Y. Mou, and C.-K. Sun, *Applied Physics Letters*, **107**(8), 081607 (2015).
23. F. Kremer, A. Huwe, A. Schönhals, and S. Rózański, in *Broadband Dielectric Spectroscopy* (Springer, 2003), pp. 171.
24. A. I. Kingon, J.-P. Maria, and S. K. Streiffer, *Nature*, **406**(6799), 1032 (2000).
25. S. L. Warring, D. A. Beattie, and A. J. McQuillan, *Langmuir*, **32**(6), 1568 (2016).
26. C. A. Okoro and Y. S. Obeng, *Thin Solid Films*, **520**(15), 5060 (2012).
27. K. Ishikawa, H. Ogawa, and S. Fujimura, *Journal of Applied Physics*, **85**(8), 4076 (1999).
28. A. Lehmann, L. Schumann, and K. Hübner, *Physica status solidi(b)*, **117**(2), 689 (1983).
29. J. Obrzut and O. Kirillov, *Presented at the Instrumentation and Measurement Technology Conference (I2MTC)*, 2013 IEEE International, 2013 (unpublished).
30. HP Product Note 8510-3 - Measuring Dielectric Constant with the HP 8510 Network Analyzer.
31. K. Joohee, P. Jun So, C. Jonghyun, S. Eakhwan, C. Jeonghyeon, K. Heegon, S. Taigon, L. Junho, L. Hyungdong, P. Kunwoo, Y. Seungtaek, S. Min-Suk, B. Kwang-Yoo, and K. Joungho, "Components, Packaging and Manufacturing Technology," *IEEE Transactions on*, **1**(2), 181 (2011).
32. C. Okoro, L. E. Levine, R. Xu, K. Hummler, and Y. Obeng, *Journal of Applied Physics*, **115**(24), (2014).
33. N. J. Lynn and N. D. Singpurwalla, *Statistical Science*, **12**(1), 13 (1997).
34. K. HÜBner, *Physica status solidi (a)*, **40**(2), 487 (1977).
35. Y. Feldman, A. Puzenko, and Y. Ryabov, in *Fractals, Diffusion, and Relaxation in Disordered Complex Systems* (John Wiley & Sons, Inc., 2005), pp. 1.
36. S. Kang, Y. Obeng, M. Decker, M. Oh, S. Merchant, S. Karthikeyan, C. Seet, and A. Oates, *Journal of electronic materials*, **30**(12), 1506 (2001).
37. C. Okoro, L. E. Levine, R. Xu, and Y. Obeng, *Journal of Materials Science*, **50**(18), 6236 (2015).
38. C. Okoro, L. E. Levine, R. Xu, K. Hummler, and Y. S. Obeng, *IEEE Transactions on Electron Devices*, **61**(7), 2473 (2014).
39. R. M. Tian Tian, H. Shin, H.-Y. Son, K.-Y. Byun, Y.-C. Joo, R. Caramto, L. Smith, Y.-L. Shen, M. Kunz, N. Tamura, and A. S. Budiman, *Procedia Engineering*, **139**, 101 (2016).
40. C. Okoro, J. W. Lau, F. Golshany, K. Hummler, and Y. S. Obeng, *Electron Devices, IEEE Transactions on*, **61**(1), 15 (2014).