Macromolecules

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Synthesis, Fabrication, and Heterostructure of Charged, Substituted Polystyrene Multilayer Dielectrics and Their Effects in Pentacene Transistors

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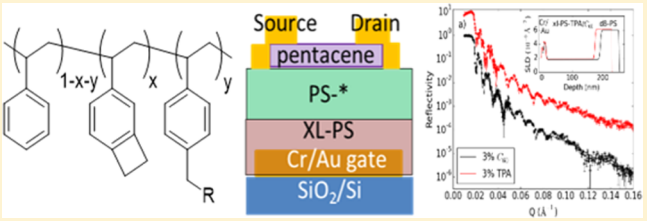
Supporting Information

ABSTRACT: Charge trapping and storage in polymer dielectrics can be harnessed to control semiconductor devices. Organic transistor (OFET) gate insulators affect bias stress and threshold voltage (V_{th}), and charging them can preset the operating voltages and control bias stress. We describe a chemical design and film fabrication procedure for construction of stacks of polystyrene (PS) layers, each with arbitrary concentrations of potentially chargeable functional groups. Thermal cross-linking of benzocyclobutene subunits ensures layer integrity while keeping the layers free of polar functionality and small molecule byproducts. Neutron reflectivity (NR), scanning electron microscopy, and atomic force microscopy (AFM) showed that individual layer thicknesses varied systematically with polymer concentration in deposition solutions, and interfacial thicknesses ranged from 1.5 to 4 nm, independent of layer thickness, demonstrating formation of distinct layers with minimal roughness or intermixing. The PS-based materials were used as the sole gate dielectrics for pentacene OFETs. We compared V_{th} before and after charging. Increased bias stress stability as evidenced by reduced V_{th} shift was seen in devices with trilayer dielectrics with substituted PS as the middle layer compared to a dielectric made from unsubstituted PS. On the other hand, increased V_{th} shift was seen in many devices with bilayer dielectrics made with substituted PS as the top layer. We attribute the decreased V_{th} shift seen in trilayer devices to an increased dielectric polarization of the substituted PS in the middle layer that countered the charge trapping effect in the top layer. This demonstration establishes a method for utilizing vertical charge patterns for various electronics applications.



1. INTRODUCTION

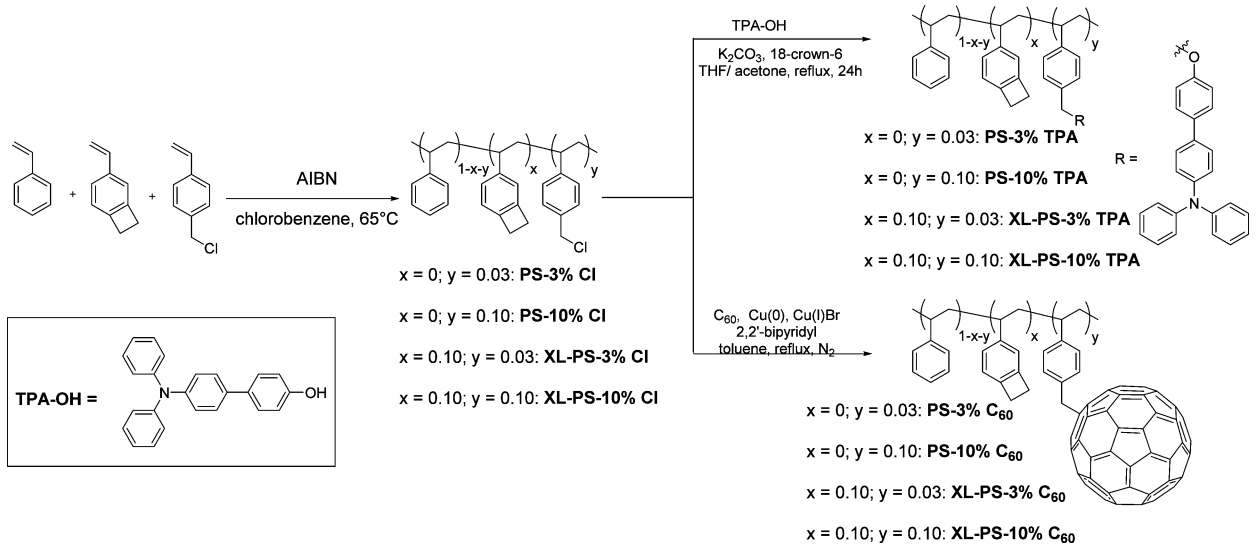
Dielectric polymer films show surprisingly rich electronic properties that can control electronic device action in ways beyond passive insulation, such as in memories and piezoelectrics.[1−4] In organic field-effect transistors (OFETs), the bulk and interface properties of the gate dielectric determine operating voltage ranges. The dielectric interfaces greatly influence the number densities and mobilities of charge carriers in adjacent semiconductors as well as threshold voltages (V_{th}) governing the turning-on of the OFETs.[5] Electric fields applied to OFET gate dielectrics can cause charge trapping or polarization that results in V_{th} shifts of tens of volts, either intentionally in the case of nonvolatile transistors[1,6−8] or incidentally as a result of bias stress.

Both nonpolar and ferroelectric polymers have been used as bulk electrostatically polarizable film materials. Much of the published work relies on silicon oxide protective "blocking" layers to prevent leakage current, rather than designing this protective capability in polymer dielectric materials themselves. An upper protective "tunneling" layer is often employed as well. Examples of polymers used in these studies include poly(methylstyrenes),[9,10] poly(vinylidene fluoride),[11,12] polystyrene−poly(vinylidene fluoride-*co*-trifluoroethylene) bilayers,[13] and poly(vinyl alcohol) paired with polystyrene (PS) as a tunneling layer.[14] Multiple inorganic dielectrics have also been stacked to make trap-based memory devices, such as one case where an inorganic gate dielectric stack sandwiches HfO_2 between layers of Al_2O_3 to result in extremely high hole and electron trapping capacity.[15] An organic/inorganic hybrid trap-based memory device with an Al_2O_3 dielectric modified by self-assembled monolayer showed clear memory characteristics.[16] A substituted triphenylene trap layer was sandwiched between poly(methyl methacrylate) (PMMA) and oxide to form a memory element.[17] A variety of polymer compositions have been employed as chargeable dielectrics. Nakajima and Fukjii used fullerene−polystyrene blends in hysteretic gate dielectrics

Received: February 2, 2016
Revised: April 5, 2016
Published: April 19, 2016

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

Scheme 1. Synthesis of Polymers Containing Cross-Linkable Functionality and Chargeable Units



characterized as capacitors.[18,19] Fullerenes were embedded in polymer or self-assembled monolayer dielectrics for charge storage.[18,20,21] Fluorene polymer and polyaniline particles with PMMA, and fluorene–methacrylate diblock copolymers with poly(vinyl alcohol), respectively, were blended to function as the gate dielectrics in pentacene memory transistors.[22−24] Fluorene, triarylamine, diphenyl ether, thiophene/selenophene oligomers, or polycyclic arenes were considered as the "donor" when embedded in polyimides where the imide was the "acceptor" in "donor–acceptor" electrets,[25−28] and a fullerene was used as the acceptor in fluorene star polymers.[29,30] A fluorene oligomer was placed as a side group in a polystyrene (PS), and ferrocene was mixed with polystyrene-*co*-poly(4-vinylpyridine) for the same purpose.[31] *However, there are no general procedures for introducing vertically localized functionality into an electret film composed of a single type of hydrophobic polymer.*

OFETs continue their development as substitutes and supplements for silicon-based electronics in large area and flexible electronics. Their well-known advantages include scalable, low-temperature fabrication techniques; control over electronic properties via organic chemistry; and device qualities like transparency, self-healing, flexibility, and stretchability for use in new applications. However, the issue of bias stress and the increase of V_{th} over time continue to detract from the applicability of OFET-based circuits. There are two major mechanisms of charging nonvolatile, or hysteretic, gate dielectric systems.[32,33] The first is the conventional "bias stress" mechanism where trap occupancy energies become equilibrated to an applied gate voltage, shifting V_{th} toward the voltage being applied from the gate. In this mechanism, net static charge is stored at the semiconductor–dielectric interface, or immobile carrier states emerge at energies equivalent to the charging voltage, and the OFETs turn off over time as they are left in the on state.[34] The second is the "dielectric polarization" mechanism, which has the opposite effect; the stored charge arises from the polarization response of the bulk of the dielectric, possibly in combination with the semiconductor or gate electrode, to the applied charging voltage.

Bias stress can arise from some very subtle effects in dielectric polymers. For example, the simple existence of chain ends or branching was found to increase the bias stress from a polystyrene dielectric, likely by a charge trapping mechanism.[35,36] Very recently, the increasing free volume in the series isotactic, syndiotactic, and atactic PMMA correlated with increased bias stress in pentacene transistors.[37] In that work, once again, a SiO_2 layer was in series with the polymer films comprising the gate dielectrics. Some solutions for bias stress instability have been proposed in the literature for polymer dielectrics. One approach is to use a fluorinated gate dielectric,[38] which decreases the trap density at the organic semiconductor (OSC)/dielectric interface. On the other hand, fluorinated gate dielectrics are also hydrophobic, which can affect the morphology and adhesion of subsequent layers.

In this paper, we explore the topics of bias stress and V_{th} through materials synthesis and multilayer dielectric fabrication. Specifically, we describe a polymer film system based on PS that allows the placement of arbitrary concentrations of electron donor or acceptor groups in different vertical positions of the stacks. Vinylbenzocyclobutene was used as a cross-linking subunit to keep the system free of polar functionality and small molecule byproducts. The layers were characterized using neutron reflectivity (NR), scanning electron microscopy (SEM), and atomic force microscopy (AFM). The PS-based materials were used as the sole gate dielectrics for pentacene OFETs, without any intervening oxide. Contrasting effects of chargeable groups on OFET charging were observed. This demonstration establishes a method for utilizing vertical charge patterns for various electronics applications.

2. EXPERIMENTAL SECTION

2.1. Polymer Synthesis. *Synthesis of PS-Cl Precursor.* A solution of styrene, 4-vinylbenzyl chloride (2% or 8% in molar ratio), and 2,2′-azobis(isobutyronitrile) (AIBN, 1% in molar ratio) in chlorobenzene (1 mL for 2 mmol total monomers) in a high-pressure vessel was bubbled with nitrogen for 10 min and then sealed rapidly under a nitrogen atmosphere. The mixture was stirred vigorously at 65 °C for 18 h in the dark. After cooling to room temperature, the resulting viscous solution was precipitated into methanol (150 mL) and stirred for 1 h. The precipitated polymer was dissolved in tetrahydrofuran (THF) and then reprecipitated into methanol. The purification procedure was repeated twice, and the precipitate was dried under vacuum (at 60 °C in the vacuum oven) to yield polystyrene-*co*-4-vinylbenzyl chloride (PS-Cl) in 68% yield (chemical structures in Scheme 1; NMR spectra and gel permeation chromatograms in

DOI: 10.1021/acs.macromol.6b00253
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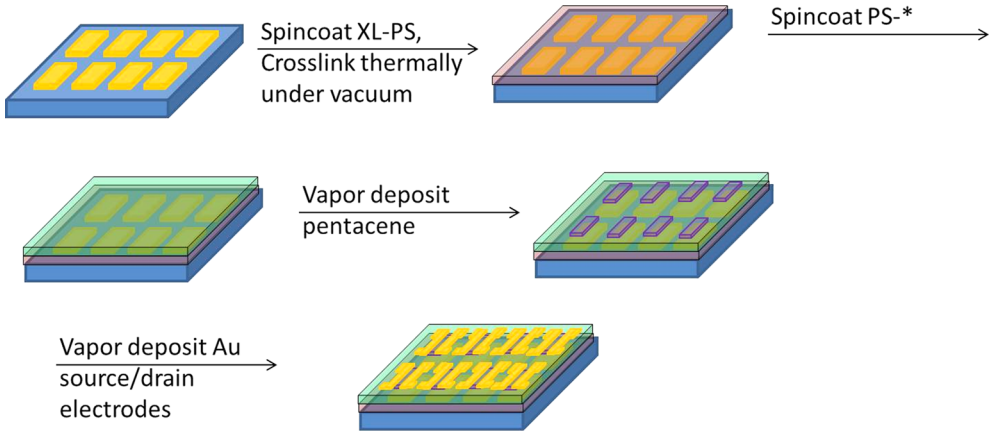

Figure 1. Fabrication steps for individual-gate bilayer OFETs. PS* refers to a PS layer that may have functionality different from the PS layer on which it is deposited. (a) Entire 1 in. square wafer with eight OFETs, during fabrication. (b) Top (left) and cross section (right) views of a completed bilayer OFET.

Supporting Information) (M_n: 13 622; polydispersity index (PDI): 1.35).

Synthesis of Cross-Linkable Polystyrene-co-4-vinylbenzocyclobutane (XL-PS)-co-(3% or 10%) Cl Precursor. The same procedure as described above for PS-Cl was followed, except that a solution of styrene, 4-vinylbenzyl chloride (2% or 8% in molar ratio), 4-vinylbenzocyclobutane (8% molar ratio), and AIBN (1% in molar ratio) in chlorobenzene was used. Depending on the initial molar ratios of the starting monomers, XL-PS-3% Cl and XL-PS-10% Cl were obtained in 77% yield (M_n: 10 476; PDI: 1.60).

Synthesis of PS-(3% or 10%) Triphenylamine (TPA) and XL-PS-(3% or 10%) TPA. The precursor polymer (0.3 g, PS-(3% or 10%) Cl or XL-PS-(3% or 10%) Cl was dissolved in a solvent mixture of THF and acetone (8 + 8 mL), in which 4-hydroxyphenyl-TPA (TPA-OH) (84.3 mg, 0.25 mmol, a large excess), K_2CO_3 (69 mg, 0.5 mmol), and 18-crown-6 (6.6 mg, 0.025 mmol) were added. The mixture was refluxed and stirred under N_2 overnight. After being cooled to room temperature, the reaction mixture was poured into water (150 mL) and then filtered. The filtrate was washed with water three times and subsequently with methanol. The residue was taken up in THF and precipitated in methanol. The precipitation was repeated twice more, and the polymer was dried under vacuum at 60 °C to yield 0.20 g of PS-(3% or 10%) TPA or XL-PS-(3% or 10%) TPA.

Synthesis of PS-(3% or 10%) C_{60} and XL-PS-(3% or 10%) C_{60}. The precursor polymer (0.5 g, PS-(3% or 10%)Cl or XL-PS-(3% or 10%) Cl was dissolved in toluene (140 mL), to which C_{60} (0.216 g, 0.3 mmol, a large excess), Cu(0) (48 mg, 0.75 mmol), CuBr (8.6 mg, 0.06 mmol), and 2,2′-bipyridine (70.3 mg, 0.45 mmol) were added. The mixture was degassed by evacuation and subsequent flushing with N_2 and then refluxed for 6 h. After being cooled to room temperature, the reaction mixture was filtered, and the solvent was removed by a rotary evaporator. The residue was taken up in THF and filtered again. In order to thoroughly remove the excess C_{60}, a silica column was run with dichloromethane (DCM) as eluent. The combined organic phases were concentrated under reduced pressure and precipitated into methanol. The polymer thus obtained was taken up in a small amount of $CHCl_3$, precipitated again in methanol, filtered, and dried at 60 °C under vacuum to obtain 0.35 g of PS- (3% or 10%) C_{60} or XL-PS-(3% or 10%) C_{60}.

Synthesis of Cross-Linkable Polystyrene-d_8-co-4-vinylbenzocyclobutane (XL-PS-d8). The same procedure as described above for PS-Cl was followed, except that deuterated styrene and (8 mol %) 4-vinylbenzocyclobutane were used as monomers. The yield was 0.51 g (66%) of polymer as white powder (M_n: 14 930; PDI: 1.53).

2.2. Film and Device Fabrication. *OFET Fabrication.* Pentacene OFETs were fabricated using the synthesized polymers as in Figure 1. The steps included spin-coating dielectric polymers for each layer on a substrate containing multiple thermally vapor-deposited gold gate pads, cross-linking any layer on which an additional layer would be deposited, and vapor deposition of the pentacene semiconductor and gold source−drain electrodes, as detailed below.

Substrate Preparation. Highly doped Si wafers on which a 300 nm thick SiO_2 layer was grown were diced into 1 in. squares and cleaned in 3:1 H_2SO_4:30% H_2O_2, followed by sonication in deionized (DI) water, acetone, and isopropanol. They were dried with a stream of nitrogen. Gate electrodes were patterned by thermal evaporation of 5 nm Cr/30 nm Au through a shadow mask to give 8 gate pads per 1 in. square wafer.

Gate Dielectric. Multiple layers of polystyrene and substituted polystyrenes were deposited by spin coating over the entire 1 in. square wafer. Spin coating was done under a dry nitrogen atmosphere in a glovebox to eliminate effects of moisture. All solutions were spin coated at 1500 rpm (90 000 Hz) for 60 s, and the film thickness was controlled by varying the polymer concentration in the range 5−20 mg/mL. To deposit layers of XL-PS, solutions of the polymer in $CHCl_3$ were sonicated at 30 °C for 60 min. Prior to spin coating, the solution was filtered into a second vial through a 0.2 μm pore size PTFE syringe filter. Cross-linking was done by heating the wafers in a vacuum oven at 180−200 °C under 70−80 mm Hg pressure for 1 h. Subsequent PS layers were then spin coated and cross-linked if required.

Pentacene Deposition and Source−Drain Electrodes. Following the deposition of the gate dielectric, 50 nm pentacene was evaporated through shadow masks so each gate electrode had a pentacene region over it. Source and drain electrodes, defining 6 mm wide and 0.25 mm long channels, were deposited through shadow masks over the pentacene films to make eight devices, each with a source/drain pair, per 1 in. square wafer.

Neutron Reflectivity Sample Preparation. Oxide was cleaned from highly doped Si wafers by an HF etch followed by rinsing in DI water and drying. Wafers were diced into 1.5 in. squares and cleaned with 3:1 H_2SO_4:30% H_2O_2, followed by sonication in DI water, acetone, and isopropanol. They then were dried by a stream of dry nitrogen. For samples built on a Cr/Au substrate, 5 nm Cr followed by 10 nm Au was deposited via physical vapor deposition. The gate dielectric stack was built as for OFET fabrication. For bilayers, XL-d8-PS was on the bottom with a hydrogenated polymer on top, or a cross-linked hydrogenated polymer was on the bottom and PS-d8 was on the top. For trilayers, XL-PS-d8 was on the bottom and PS-d8 was on the top; a hydrogenated layer was in the middle. PS with chargeable side chains was always hydrogenated, and nonfunctionalized PS flanking layers were deuterated for NR experiments. For samples with a gold or pentacene top surface to facilitate charging, the edges of the sample were masked off with aluminum foil, followed by vapor deposition of 50 nm gold or pentacene.

Neutron Reflectivity Techniques. NR measurements were performed on the polarized beam reflectometer (PBR) at the NIST Center for Neutron Research. The samples studied were typically

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

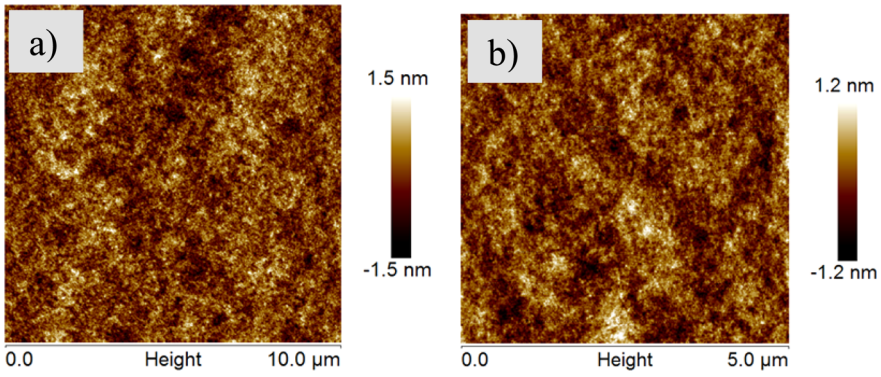

Figure 2. AFM of XL-PS films. (a) XL-PS from a 20 mg/mL solution, spin coated on a gold surface. Root mean square (RMS) roughness: 0.34 nm. (b) XL-d8-PS from a 10 mg/mL solution, spin coated on native SiO_2. RMS roughness: 0.28 nm.

fabricated on 38 × 38 mm^2 silicon wafers with a layer of native oxide. A vertically focusing pyrolytic graphite monochromator was used to select neutrons of wavelength λ = 4.75 Å with a divergence of 0.05 Å. A neutron-opaque mask was used before the sample to control the vertical size of the beam to avoid illuminating the edges of the samples. Measurements were restricted to the specular condition and typically were carried out over the range $0 < 2\theta < 7.8°$, where 2θ is the scattering angle, which corresponded to wave vector transfer Q perpendicular to the films in the range $0 < Q < 0.18$ $Å^{-1}$. Measurements of the background were taken over the same range with a 0.3° offset from the specular condition in the sample angle Ω.

In order to span the desired Q-range, two different configurations of the four slits that control the PBR's beam divergence were used. At low Q ($Q < 0.06$ $Å^{-1}$) the slit widths were set at 0.1, 0.1, 0.3, and 0.4 mm (for the bilayer samples) or 0.1, 0.1, 0.6, and 0.8 mm (for the trilayer samples) to provide constant incident neutron flux on the sample. At higher Q ($Q > 0.035$ $Å^{-1}$), a variable slit-width configuration was employed that yielded a constant 30 mm long illuminated sample area. For samples that required use of both slit geometries, both data sets were fit simultaneously to the same theoretical model (see below).

SEM and AFM Instrument Details. SEM images were obtained using a FEI Quanta 200 Environmental SEM using a cross-sectional sample holder (Electron Microscopy Sciences). AFM images were obtained using a Veeco MultiMode AFM in tapping mode.

Removable PDMS Electrode Fabrication. To create removable electrodes for charging PS multilayers for NR measurements, a 10:1 polydimethylsiloxane (PDMS, Sylgard 184) solution was prepared by stirring 10 parts by weight of base with 1 part by weight of curing agent in air for 20 min, followed by 20 min degassing under vacuum. The uncured PDMS was poured into a Petri dish and cured at 70 °C for 1 h. The cured PDMS was cut into 1 or 1.5 in. squares while face-down in the Petri dish; then the squares were removed and taped by the corners face-up on the thermal evaporator sample holder. 10 nm Cr followed by 80 nm Au was deposited over the PDMS squares. The conductivity of the metal was verified with a multimeter. Carbon paint was applied to an edge and a small patch on the opposing surface of the PDMS, and electrical continuity between the gold face and the carbon paint on the reverse side was verified. The efficacy of the removable PDMS electrode for charging was ascertained by charging pentacene/SiO_2 OFETs with a PDMS electrode and comparing the V_{th} shift observed to that seen following charging with probes on the vapor deposited source/drain electrodes. The results were similar using the two charging mechanisms, indicating that the PDMS electrode is a reliable way to charge materials without probing directly on the surface.

3. RESULTS

3.1. Polymer Design, Synthesis, and Film Formation.

We designed and synthesized novel styrene polymers (Scheme 1) so that they meet all of the requirements to function in charged heterostructures: formation of sufficiently continuous films, ability to attach varied chargeable groups to a common backbone structure, minimization of hydrophilic functional groups in the backbones and chargeable side groups, and sufficient thermal cross-linking to prevent dissolution of existing films when overlying films are deposited, while preserving the chargeable functionality. This led to the cyclobutenostyrene−chloromethylstyrene polymer system shown. For situations where cross-linking would be needed, the relative values of $1 - x - y$, x, and y were optimized to 0.87:0.10:0.03; i.e., 10% cross-linking functionality and 3% chargeable functionality, or 0.80:0.10:0.10, with 10% chargeable functionality. For top layers of heterostructures, cross-linking was not needed, and the values of $1 - x - y$, x, and y were 0.97, 0, and 0.03 or 0.90, 0, and 0.10. For samples used in neutron reflectivity studies, the unsubstituted styrene groups were perdeuterated as needed to provide scattering contrast. Cross-linking via divinylbenzene subunits, either using benzoyl peroxide or ultraviolet initiation, was not as effective as the cyclobutenostyrene. Polymers with 5% cross-linking functionality were also synthesized but gave rougher films (as observed by AFM) than with 10% cross-linker. Synthetic methods used for the polymers can be extended arbitrarily to different concentrations and structures of chargeable groups and larger numbers of layers.

All cross-linkable, TPA, and C_{60}-substituted polymers discussed here were synthesized using AIBN-initiated free radical polymerization in chlorobenzene. When a cross-linkable unit was required, 4-vinylbenzocyclobutane was used as a comonomer for reasons discussed above. 4-Vinyl benzyl chloride was used for installation of a postpolymerization functionalizable handle onto the polymer backbone. After isolation of the polymer, either TPA-OH or C_{60} was further reacted with side chain chlorobenzyl groups to obtain the required polymers PS-(3% or 10%) TPA, XL-PS(3% or 10%) TPA, PS-(3% or 10%) C_{60}, and XL-PS(3% or 10%) C_{60}, respectively, as shown in Scheme 1. TPA-OH was synthesized using a procedure previously reported in the literature.[39]

The key procedural hurdle for fabricating the multilayers was ensuring the smoothness of the cross-linkable polystyrene film after thermal curing. Chloroform was found to be a more advantageous spin-coating solvent than aromatic solvents, dichloromethane, dichloroethane, or methyl ethyl ketone. A minimum 1−2 wt % solution was also required in order to prevent dewetting and the formation of pinholes that would compromise the integrity of both morphological and electrical characterization. The cross-linked films were resistant to

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

dissolution and delamination during subsequent exposures to chlorinated and aromatic solvents.

3.2. Polymer Film Characterization. *AFM Morphology Determination.* We measured the roughness of the surface of cross-linked PS samples, both to ensure film quality of the XL-PS and to compare with the roughness observed by NR. In general, the roughness seen by AFM was lower than that found by NR for buried interfaces involving these materials, indicating either that the spin coating of subsequent layers causes a modest alteration of the film interface or that there is a variation in the topography results because of the smaller lateral scales probed by AFM compared to NR. In Figure 2a, AFM data for an XL-PS film spin coated from a 20 mg/mL solution on Cr/Au are displayed, while Figure 2b shows AFM data for a 10 mg/mL film on native SiO_2. The similarity between the surface roughnesses of these two films showed that interface quality was not sensitive to the substrate for films in the thickness range we are using (50−200 nm).

SEM Thickness Determination. The film thicknesses of the single XL-PS layer and a XL-PS/PS bilayer were determined using SEM. The Cr/Au on SiO_2/Si substrate was prepared as described in the OFET Fabrication section. Both layers were spin coated from 20 mg/mL solutions. The sample was fractured using a diamond scribe and a pair of tweezers prior to imaging. The cross section of the film was sputtered with platinum before imaging. As seen in Figure 3a, film thickness of a single layer of polystyrene (XL-PS) spin coated from a 20 mg/mL solution was found to be 240.4 ± 5.5 nm (note that the uncertainties (error bars) for the SEM thickness data are the standard deviations of 10−15 measurements on various points on the same film, when the substrate was broken at different places). Sharp focusing was difficult due to charging of the film from the electron beam. The Cr/Au layer was clearly visible as a bright feature on the bulk silicon and was found to be 36.6 ± 3.3 nm (10 measurements). When a second PS layer was deposited from a 20 mg/mL solution after cross-linking the first layer, the overall film thickness was found to be 551.1 ± 8.1 nm (11 measurements, Figure 3b). While a sharp contrast between the two polymer films was not obtained, a distinct region was visible at the bottom of the film which may be the cross-linked polymer layer. This further corroborates the idea that the integrity of the initially deposited polymer layer is maintained through the second deposition step.

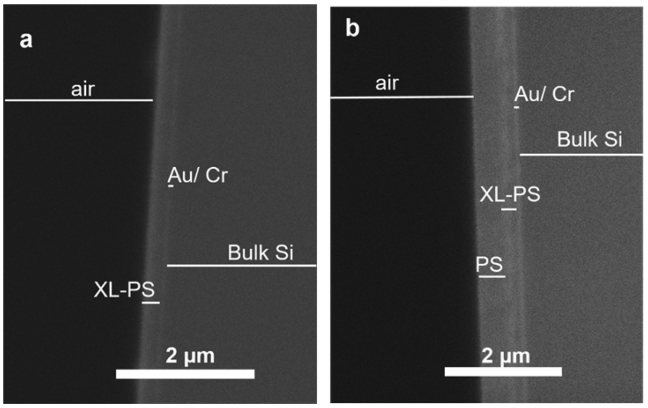

Figure 3. SEM of cross sections of XL-PS (a) and XL-PS/PS (b) films deposited on gold surfaces.

We note that the thickness of the bilayer is not exactly twice that observed for the single layer. Though the concentrations of the two solutions and the spin-coating conditions were the same, the substrate on which the two layers were deposited was different from the single layer case, so it is logical that the wetting properties and final thickness would also be somewhat different.

Neutron Reflectivity Study. Figure 4a shows the measured reflectivity for two samples each with two polymer layers on Cr/Au: an XL-PS with an added functional group (3% C_{60} or 3% TPA) followed by a perdeuterated polystyrene (d8-PS) layer. The data from the fixed and variable slit configurations are overlaid to show continuous reflectivity profiles. Figure 4b shows two examples of reflectivity data for polymer trilayers. Both have a bottom layer of deuterated XL-PS (XL-d8-PS), followed by a layer of XL-PS with either 3% or 10% TPA, followed by a final layer of d8-PS.

We used the specular reflectivity to develop a full one-dimensional depth profile of such thin film structures by determining the scattering length density (SLD) $\rho(z)$, where z is the coordinate perpendicular to the film surface. Data reduction and model fitting were carried out using the Reflpak and Refl1d software packages, respectively.[40,41] Each layer of the film was modeled with a thickness and SLD. In order to determine the amount of mixing between layers, or roughness, the interface of adjacent layers was modeled with an interpolating error function of the form $\mathrm{erf}((z - z_i)/\sigma_i\sqrt{2})$, where z_i is the location of the boundary determined by layer

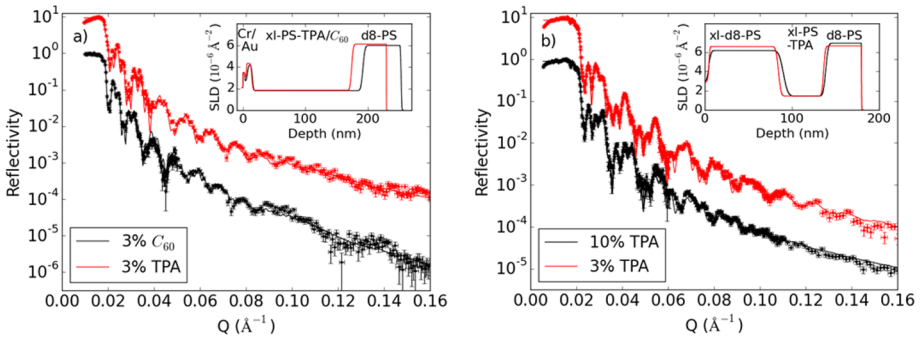

Figure 4. (a) Measured reflectivity for two bilayer samples spin-coated on Cr/Au: XL-PS-3%C_{60}/d8-PS and XL-PS-3%TPA/d8-PS. (b) Reflectivity data for two trilayers with layer structure XL-d8-PS/XL-PS-R/d8-PS, where R = 3% TPA or 10% TPA. The upper trace in each panel has been offset by a factor of 10 for clarity. The solid lines through the data are best-fit model curves determined as described in the text. This modeling yields the scattering length density (SLD) profiles shown in the insets, where the zero of the depth axis is the top of the underlying Si wafer.

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

thickness and σ_i is the reported roughness. After a model of the whole structure was determined, a theoretical reflectivity profile was calculated and compared to the measured data. χ^2 minimization schemes were employed to refine the model. The resulting fits to the reflectivity curves are shown as solid lines overlaying the data in Figure 4, and the corresponding SLD depth profiles are shown in the insets. *These fitted models reproduce the characteristic features of the data and gave parameter values that are corroborated by measurements made via SEM and AFM.*

By compiling the fitted values of layers between different samples, a systematic picture of the quality of layers can be developed. Figure 5a shows the thickness of different layers

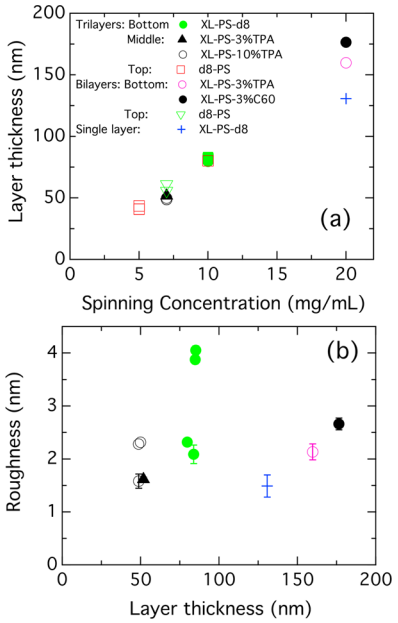

Figure 5. Comparison of layer parameters determined from NR fits. (a) Layer thickness versus the concentration the layer was fabricated from during spin-coating. (b) The roughness at the top of a layer vs the thickness of that layer. The symbols in (b) correspond to the legend in (a). Error bars show 95% confidence intervals as determined from model fitting software. Where not shown, error bars are smaller than the marker size.

plotted against the concentration of the solution from which they were deposited. We can clearly see that for layers of this size we have strong and repeatable control of the thickness of our multilayered structures. Also, the NR- and SEM-derived thickness of a 20 mg/mL solution-spin-coated layer of PS is qualitatively similar to the thicknesses of various PS polymers obtained from this solution concentration in the process of forming multilayers, both on the order of 200 nm.

By comparing the roughness between cross-linked and adjacent layers, we can assess the integrity and distinguishability of the layers. Figure 5b shows the fitted values of these parameters. From this we can see that the roughness between layers appears to be independent of layer thickness for the range of thicknesses measured and is in the range of 1.5−4 nm.

There were several other observations that came from the NR measurements. One was that layers with 10% C_{60} consistently gave reflectivity profiles which exhibited attributes consistent with poor layer integrity and uniformity. This is not surprising considering the great difference in molecular shape, free volume, and side chain interaction associated with the C_{60} subunit compared to phenyl-based side chains.

We also found that samples that included gate layers of vapor deposited Cr/Au to more fully simulate electronic device structures, such as the bilayers shown in Figure 4a, proved difficult to model solely from the NR data due to the increased complexity of their SLD profiles. To constrain these fits, X-ray reflectivity (XRR) measurements were carried out separately on Cr/Au films made under comparable conditions to those used for bilayer dielectric deposition (data not shown). The resulting Cr/Au layer parameters provided needed input to produce the fits to the NR data shown in Figure 4a. However, we later verified by AFM that the structure of the polymer layers was not measurably affected by the absence of the gate for polymer thicknesses that we considered (Figure 2), and thus, in light of the numerical complication the metal gate layers posed for the modeling, these layers were omitted in subsequent samples, such as the trilayers shown in Figure 4b.

To test for the possibility that structural changes arising from the charging process could influence the electronic properties of our OFET devices discussed below, we made NR measurements on a set of PS-trilayer samples with either Au or pentacene top layers. NR measurements were made both before and after charging via a removable silicone electrode. No samples measured exhibited statistically distinguishable changes in their reflectivity postcharging, for charging voltages of up to ±70 V, which exerts approximately twice the electric field used for OFET charging. An example of such data is shown in Figure 6. As such, we concluded that charging the devices did not have

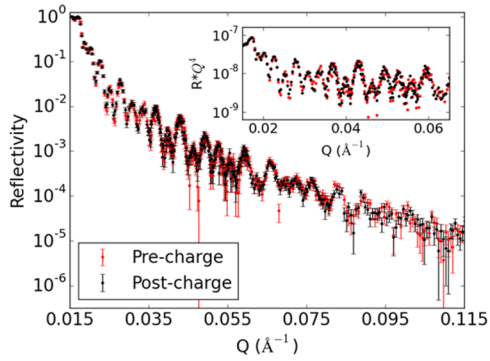

Figure 6. Comparison of the reflectivity profile before and after charging at +70 V for 10 min for a sample with the structure XL-d8-PS/XL-PS-10% TPA/d8-PS/Au. Inset shows the data multiplied by Q^4 to enable more detailed comparison of the two data sets.

a significant impact on their structure, and any observed effects of charging in devices could not be attributed to any field-induced change in the dimensions or integrity of the layers.

3.3. Modulation and Stability of Threshold Voltage in OFETs. Substituted PS films were used as the gate dielectric in pentacene OFETs. We measured the charge trapped in the gate dielectric by comparing the threshold voltage (V_{th}) of the OFET before and after a charging step. V_{th} is a measure of the free carrier and trap densities in and near the semiconductor channel, which is modulated by local electric fields. Fields produced by charges trapped in the gate dielectric layer increase or decrease the free carrier density in the OSC. Therefore, at a given gate voltage (V_g), the number of free carriers, and therefore the output current, changes depending on local static fields. In a p-channel pentacene OFET, an electrostatic field

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

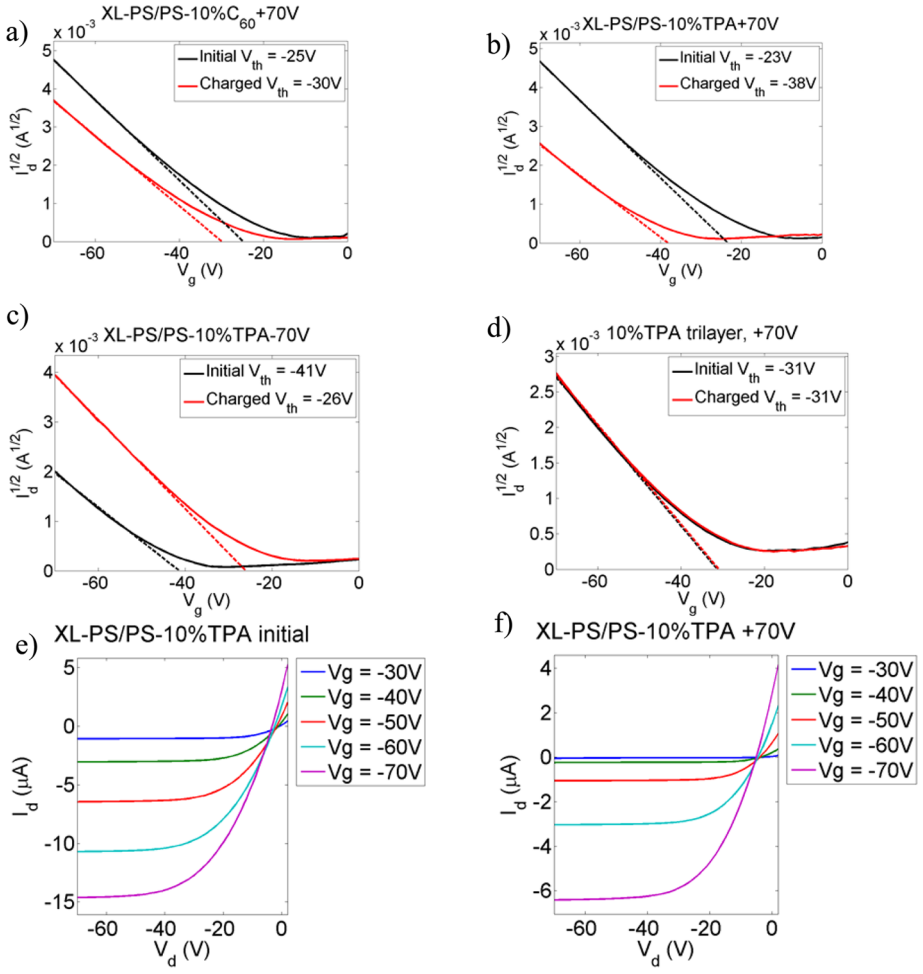

Figure 7. (a) Determination of threshold voltage V_{th} from drain current I_d vs gate voltage V_g data with V_d held at −70 V for a pentacene OFET with a bilayer XL-PS/PS-C_{60} gate dielectric. "10%" indicates 10% substitution with C_{60}. The positive V_{th} shift follows charging with +70 V for 10 min is 30 V − 25 V = +5 V. (b) The positive V_{th} shift following charging a XL-PS/PS-TPA (10%) device with +70 V for 10 min is 38 V − 23 V = +15 V. (c) A negative V_{th} shift of −15 V charging another XL-PS/PS-TPA (10%) device. (d) An example of an XL-PS/PS-TPA/PS trilayer device that was very stable to charging, with the curve before and after charging nearly superimposed. Bottom: the output characteristics, I_d vs drain voltage V_d, of the device in (b) before (e) and after (f) charging.

oriented with a layer of negative charges near the pentacene acts to induce free holes into the channel and decrease the V_{th}, according to the "bias stress" charging mechanism. In this paper, we define a decrease in the magnitude of V_{th}—indicating the device is easier to turn on—as a negative V_{th} shift. We define an increase in the magnitude of V_{th} as a positive V_{th} shift.

V_{th} for each device, before and after charging, was calculated from the square root transfer curve. A straight line was fit from data taken between gate voltages V_g of −70 and −50 V, shown in Figure 7a for an XL-PS/PS-C_{60} OFET. V_{th} was defined as the x intercept of this line. Extrapolation to the x-axis is one of the main methods of calculating threshold voltage seen in the literature.[8] The V_{th} shift following charging was determined by subtracting V_{th} of the original OFET from V_{th} after charging. We used ±70 V for charging, as this was the highest voltage at which breakdown rarely occurred, keeping in mind that the device architecture does not include any protective oxide barrier layer in series with the polymer dielectrics. Other representative I−V data are shown in Figures 7b−d for XL-PS/PS-TPA bilayers and an XL-PS/PS-TPA/PS trilayer. Output curves in Figures 7e and 7f, corresponding to the device in 7d, illustrate the extremely flat saturation regions and the excellent agreement between maximum currents obtained using the transfer and output voltage sweep modes.

We investigated V_{th} shifts in two types of systems. The first had a bilayer gate dielectric composed of a cross-linked layer nearer the gate covered by a non-cross-linked layer. We first obtained the baseline shifts from unsubstituted PS control devices, using a bilayer of unsubstituted PS deposited on cross-linked PS (referred to here as XL-PS/PS). Both layers were spin coated from 20 mg/mL $CHCl_3$ solutions. The cross-linked PS layer was measured at 240 nm thick by SEM, and at 125−175 nm thick by NR, indicating the true thickness is approximately 200 nm. The second PS layer was determined by SEM to be approximately 310 nm, but the 20 mg/mL PS on 20 mg/mL XL-PS bilayer was too thick to be measured by NR. As measured by SEM, the non-crosslinked PS has a similar thickness to the cross-linked PS (200 nm), and since spin-coating solution compositions were analogous for the NR and OFET experiments, we expect that the NR-derived thicknesses apply to both.

We observed a range of V_{th} shifts upon charging over several repetitions of device fabrication. A histogram illustrating the results is shown in Figure 8a. This data set indicates that charging PS-only films gives small and inconsistent V_{th} shifts

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

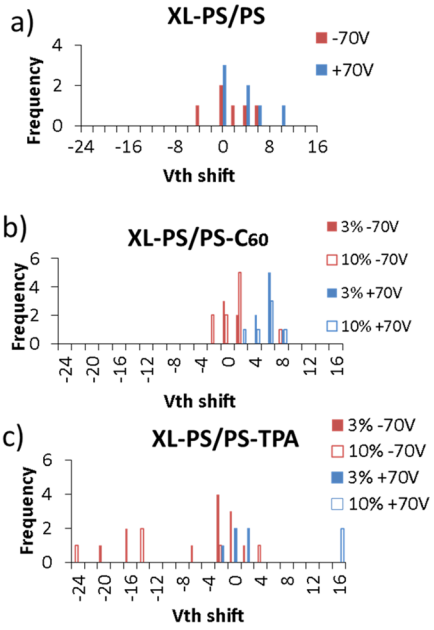

Figure 8. Histogram of V_{th} shifts before and after charging. On average, positive charging results in an increase in V_{th} and negative charging results in a decrease in V_{th}. In this paper, we define a negative V_{th} shift as a reduction in the magnitude of the gate voltage required to turn the p-channel device on. The total thickness of the bilayer dielectric is approximately 400 nm using thicknesses determined from neutron reflectivity. (a) The control: XL-PS/PS devices charged with −70 V (red) or +70 V (blue). (b) XL-PS/PS-C_{60} devices, made from either 3% (solid) or 10% (no fill) PS-C_{60} and charged with −70 V (red) or +70 V (blue). No significant difference is seen between those made with 3% and 10% C_{60}. (c) XL-PS/PS-TPA devices, made from either 3% (solid) or 10% (no fill) PS-TPA and charged with −70 V (red) or +70 V (blue). Those with 10% substitution show large shifts more frequently than those with 3% substitution.

where the polarity of charging does not have a strong correlation with the sign of the V_{th} shift. The somewhat more systematic charging (most shifts are zero or positive) seen when charging with positive voltages could be from one of two causes. Because the voltage is applied to the top surface of the dielectric through a pentacene film, it could be that positive voltages are more easily transferred through the pentacene than negative voltages. The other possible explanation is that traps in the bottom cross-linked PS layer accept negative charges more easily or the top PS layer accepts positive charges more easily.

We then studied devices with dielectric layers with substituted PS top layers over XL-PS. The substituents we used were TPA and C_{60}, which were present in the polymers at either 3% or 10% concentration. The V_{th} shifts upon charging these devices were larger and variable for both PS-TPA and PS-C_{60}, with differences seen between positive and negative charging, as well as between the two materials. In general, with the C_{60} functionality, there was no difference in charge capturing performance between those with 10% and with 3% functionalization, as seen in Figure 8b, but with the TPA functional group, 10% TPA resulted in more frequent large V_{th} shifts, as seen in Figure 8c. When comparing positively and negatively charged samples in Figure 8c, negative charging gave large shifts more frequently than positive charging. This could indicate that PS-TPA accepts negative charges more readily than it accepts positive charges, unlike what was observed for pure PS films in the control samples. The directions of these top-chargeable layer V_{th} shifts are overwhelmingly consistent with bias stress effects, except for C_{60} with negative charging, which showed little effect.

In addition to studying bilayers with substituted PS on top of unsubstituted, cross-linked PS, we studied bilayers made with unsubstituted PS on top of substituted, cross-linked PS, to compare cases where the substituents C_{60} or TPA were next to the pentacene layer or next to the gate electrode. In Figures 8b and 8c are illustrated the V_{th} shifts obtained when the substituents were next to the pentacene. When the substituted PS was on the bottom layer, next to the gate electrode, however, all V_{th} shifts following charging were under 3 V (out of 14 devices). When comparing this to the bilayers seen in Figures 8b and 8c, where the substituted PS was on top, it is clear that placing the substituted PS adjacent to the pentacene resulted in a larger V_{th} shift, particularly in the XL-PS/PS-TPA devices. When comparing with Figure 8a, which did not have any substituents, it is possible that somewhat smaller V_{th} shifts are seen. It is possible that putting substituted PS near the gate has decreased the bias stress susceptibility of the device, but more work is required to fully examine this possibility.

Finally, we made trilayer dielectrics, with the middle PS layer substituted with C_{60} or TPA and the outer layers without these substituents. The first layer was XL-PS spin coated from a 20 mg/mL $CHCl_3$ solution and crosslinked as in bilayers. The middle layer was spin coated from a 15 mg/mL $CHCl_3$ solution of cross-linkable, substituted PS (e.g., XL-PS-C_{60}). From Figure 5a, which shows spin-coating solution concentration versus NR-determined thickness, the thickness of this film may be interpolated to be approximately 125 nm. Likewise, the top layers of PS spin coated from 5 mg/mL $CHCl_3$ solutions may be seen from Figure 5a to be approximately 50 nm thick.

The threshold voltage shifts upon charging these devices were much smaller, *smaller even than those seen in the XL-PS/PS bilayer devices.* For XL-PS/XL-PS-TPA/PS, a moderate difference between the devices made with XL-PS-TPA with 10% TPA substitution and those made with 3% substitution was noted: all V_{th} shifts of magnitude 1 V or greater occurred in devices made with 3% XL-PS-TPA as the middle layer, as shown in Figure 9a. *Devices with 10% TPA as the middle layer show essentially zero V_{th} shift when charging with +70 or −70 V.* Preventing the development of bias stress upon sustained application of a gate bias is an important goal of OFET bias stress investigations, as stated in the Introduction. A likely mechanism, involving compensation of interface charge effects by charging of the middle layer, is discussed in more detail below.

For XL-PS/XL-PS-C_{60}/PS, small shifts were typically seen (Figure 9b). This trilayer was not as resistant to bias stress as the trilayer containing TPA in the middle layer. The XL-PS-C_{60} used to make these trilayers was substituted with 3% C_{60} only, as XL-PS-10% C_{60} was too insoluble to make devices.

The capacitance of several bilayer and trilayer dielectrics was measured at 1 kHz after charging and OFET testing using a voltage of 500 mV, and the dielectric constants were calculated, as shown in Table 1.

For several of the samples, dielectric constants were in good agreement with reported values for PS. Capacitances 30−50% higher than that of PS (5.3−6.6 nF/cm^2 or ε_R = 2.4−3.0) were seen in both the XL-PS/PS-10%TPA and in the trilayer dielectrics. In the former case this could be due to an increase in percent of polarizable species (i.e., from 3% TPA to 10%), which may increase the polarization response of the film to

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

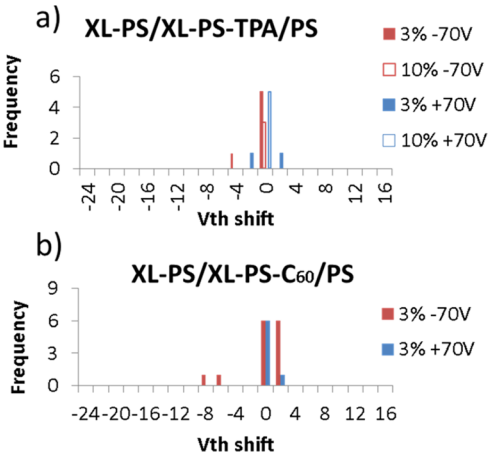

Figure 9. Charging trilayer dielectrics composed of a XL-PS bottom layer, a substituted and cross-linked PS middle layer, and a thin PS top layer. The total dielectric film thickness was approximately 375 nm thick. We saw a smaller range of V_{th} shifts after charging than in the control consisting of only PS. (a) A histogram of V_{th} shifts before and after charging XL-PS/PS-TPA/PS devices made from either 3% (solid) or 10% (no fill) XL-PS-TPA and charged with −70 V (red) or +70 V (blue). (b) A histogram of V_{th} shifts before and after charging XL-PS/PS-C_{60}/PS devices made from 3% XL-PS-C_{60} and charged with −70 V (red) or +70 V (blue). XL-PS-C_{60} made with 10% C_{60} was not soluble enough for use.

Table 1. Representative Relative Dielectric Constants (ε_R) of Bilayer and Trilayer Films

multilayer (400 nm total thickness)	C_i (nF/cm^2)	ε_R
PS (C_i calculated from typical ε_R)	5.3−6.6	2.4−3.0 typical
XL-PS/PS	5.4	2.4
XL-PS/PS-3% C60	5.7	2.6
XL-PS/PS-3% TPA	5.7	2.6
XL-PS/PS-10% TPA	9.8	4.4
XL-PS/XL-PS-10% TPA/PS	8.9	4.0
XL-PS/XL-PS-3% C60/PS	8.8	3.9

applied voltage. In the case of the capacitance of a trilayer dielectric, the additional interfaces may be locations of additional polarizability. Work in our group is ongoing to isolate the interfacial from bulk effects in these types of heterstructures.

While the variation in ε_R should not be expected to be sufficient to cause large changes in field-effect mobility (μ_{FE}) on its own, we nevertheless looked at the variation in specific capacitance among the dielectric materials to determine whether there was any correlation to μ_{FE} in our devices. We found that the devices show a range of mobility depending on the quality of the evaporated pentacene OSC, but the highest mobilities occur in the 3% TPA bilayer (over many sets of sample fabrication) and the 3% C_{60} trilayer, neither of which have exceptionally high or low values of ε_R.

Gate leakage current was measured simultaneously with the drain current for the square root transfer plots presented in Figure 7. The square root of the gate current vs the applied gate voltage of two representative devices is presented in Figure 10 for ease of comparison with the square root transfer plots of drain current vs gate voltage of Figure 7. A complete set of plots is included in the Supporting Information. The square root gate current is typically about an order of magnitude lower

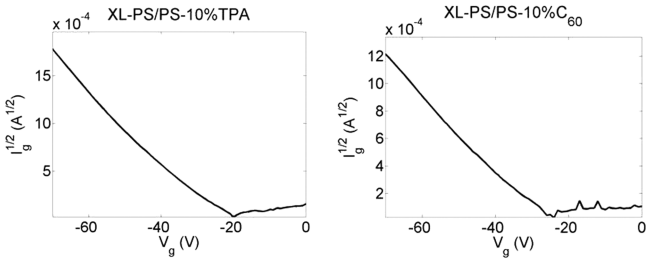

Figure 10. Square root of gate leakage current vs gate voltage for two bilayers reported in Figure 7.

than the square root drain current (meaning the absolute gate current is 2 orders of magnitude lower).

4. DISCUSSION

The NR data tell us that for the purposes of device fabrication the cross-linking technique allows us to create repeatable, controllable, and distinct layers in multilayered dielectrics prepared using spin coating as the deposition method. *This is the key conclusion from the NR study*, validating this work as the first demonstration of such a degree of layer integrity from multiple spin-coated films of chemically similar, hydrophobic, insulating polymers. The ability to append functionality to side chains in arbitrary positions in the multilayers without significantly changing the hydrophobicity is another advantage of our polymer and procedural design. The closest prior analogy is an optically reflective stack of tens of layers of polystyrene alternating with poly(vinylpyrrolidone), the latter being a highly hydrophilic polymer.[42] While AFM was used in that study to show that exposed interfaces were smooth, no NR or analogous data were presented to characterize internal interfaces. Other polymer dielectric multilayer examples included much more polar or polarizable layers appropriate for their intended applications, such as poly(vinylidene fluoride−trifluoroethylene), poly(vinylphenol), and elemental tellurium.[43−47]

The roughness of the buried interfaces in our work is somewhat larger than that observed for XL-PS/air interfaces observed by AFM, suggesting that some minimal intermixing may occur near the cross-linked layer boundaries. This is perhaps not surprising, as the low cross-linker density (10%) may still allow for some local flexibility or deformability in the XL layers when exposed to solvents in subsequent spin-coating steps.

We propose that different V_{th} shift mechanisms are active in bilayer devices compared to trilayer devices. In bilayers, the dominant charging mechanism appears to be charge trapping near the OSC/dielectric interface. The most probable direction of V_{th} shift, an increase in V_{th} with positive charging and a decrease in V_{th} with negative charging, confirms this. In the trilayer devices, however, we not only see a decreased magnitude of V_{th} shift from dielectric insulation between the charged layer and the OSC but also see a very tight range of V_{th} shifts, surrounding zero, as opposed to the much larger range of probable V_{th} shifts in devices with substituted PS as the top of the bilayer dielectrics. We believe the large range seen in bilayers is caused by the statistically driven probability of grouping multiple substituents together at the surface near the pentacene. When substituents are buried or overdiluted, they cannot lead to the consistent charge trapping required to shift the energy levels at the pentacene interface. A cluster of

DOI: 10.1021/acs.macromol.6b00253
Macromolecules 2016, 49, 3478−3489

substituents may be needed for the extra trapping beyond that done in the PS-only control. The more frequent large shifts observed in 10% TPA compared to 3% TPA top layer OFETs is consistent with this. This effect was not observed in 3% vs 10% C_{60} substituted PS, which is logical since the C_{60} molecule is much larger and may not be able to form clusters at the dielectric/OSC interface.

The greater effect of negative charging relative to positive charging at PS-TPA is somewhat counterintuitive considering that TPA is nominally an electron donor. However, there is the possibility that some fraction of the TPA becomes ionized in the course of sample preparation, and its neutralization during the charging process results in a net negative charge. Another possibility is that TPA aggregates form traps that stabilize negative charges through local polarization. The use of more strongly electron donating side chains at even higher concentrations in future work should clarify this issue. The frequent negative shifts seen with TPA also point to an eventual route to nonvolatile tuning of V_{th} for easier OFET turn-on with the use of stronger electron donor side groups.

On the other hand, if the mechanism for charging the middle of a trilayer is polarization rather than charge injection, it is not necessarily susceptible to this clustering effect. Alignment or formation of dipoles in the polymer matrix will likely not depend on substituent clustering in the way that the charge trapping mechanism does. Note that if trilayer charging effects were the result of a simply diluted effect analogous to what was seen with bilayers because of more difficult charge injection into the middle layer, the V_{th} shifts would still have been in a consistent direction. However, instead we observe V_{th} shifts in the trilayers that are nondirectional in addition to being very small.

We propose that during charging the trilayer structure, both bias stress and dielectric polarization charging mechanisms occur. Charges are injected into the semiconductor/dielectric interface, and a dipole involving the middle layer is also formed. These effects counter each other, resulting in little or no net change of the threshold voltage. The insulator/semiconductor interface is still charged by the addition of net static charge via filling of traps or creation of new traps—this happens, for example, for charging with negative voltage on the semiconductor, by injecting negative carriers into the semiconductor/dielectric interface. Since the semiconductor/dielectric interface of the trilayers does not have substituents, the baseline level of charge trapping occurs, as was observed with the unsubstituted PS dielectrics.

One remaining question is why bulk dipole formation does not seem to occur in bilayers, as we are hypothesizing for the trilayers. In a bilayer, there are three relevant interfaces. Two are directly in contact with electrically conductive materials, and one is between dielectric layers. In a trilayer, there are four relevant interfaces. Interfaces are likely locations for charge traps and defects, and so trapped charge may be stored there. The additional interface in the trilayer structure may create another layer of charges that can act on the middle substituted PS layer.

5. CONCLUSION

We have synthesized a set of PS-based polymers with which the chargeable substituents, TPA and C_{60}, can be localized in different layers of pentacene OFET gate dielectrics. The localization of functionality in each layer was quantified using NR. OFETs were made using gold gate electrodes with the polymers as the sole gate dielectrics with no intervening oxides. A reduced V_{th} shift was seen in devices with trilayer dielectrics with substituted PS as the middle layer compared to a dielectric made from unsubstituted PS. Substituted PS as the layer nearest the pentacene had a significant probability of causing much larger and more directional V_{th} shifts than unsubstituted PS. We attribute the differences to varying contributions of charge injection and dielectric polarization mechanisms operating in the different dielectric multilayer structures. The multilayer dielectric architecture can serve as a general platform for tuning OFET hysteresis to either minimize bias stress, by tuning charging activity in middle layers of trilayers, or maximizing memory effects by introducing more strongly electron donating or accepting side groups in top layers. The charging phenomena can also be applied to insulators in configurations other than OFETs. Work along all of these lines is in progress.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.macromol.6b00253.

NMR spectra, GPC traces of synthesized polymers, and gate leakage current plots (PDF)

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by the U.S. Department of Energy, Office of Science, Basic Energy Sciences, under Award DE-FG02-07ER46465. Certain commercial equipment, instruments, materials, and software are identified in this paper to foster understanding. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

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