Transistor Model Verification Including Measurement Uncertainty

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***Abstract*— We verified a model for state-of-the-art 250-nm heterojunction bipolar transistors with large-signal measurements. We demonstrated the propagation of correlated measurement uncertainties through the model extraction and verification processes and used them to quantify the differences observed in the measurements and models and the accuracy of the model parameters we extracted.**

***Index Terms*— Measurement uncertainty, microwave measurement, model verification, transistor model.**

I. Introduction

WE PROPAGATE the uncertainty in large-signal measurements through a heterojunction bipolar transistor (HBT) model verification procedure and use those uncertainties to better quantify the differences in our measurements and simulations. After eliminating differences due to process variations, we are able to obtain greater insight into the model and how well it performs under large-signal operating conditions.

Compact models are designed to capture the essential physics governing a transistor's behavior and to be used well outside the space of measurements used in the model parameter extraction process. Nevertheless, practical limitations always restrict the data sets used in even the most comprehensive transistor model extraction procedures, and models are often used well outside of the operating conditions under which they were developed. Thus, it remains important to verify the model in regions of operation not used in the extraction process.

Measurement uncertainties are not usually considered in the verification procedure. This leaves open the possibility that observed differences between the actual and predicted behaviors of the transistor in the verification process are due to measurement error, and not to the inability of the model to accurately predict transistor behavior.

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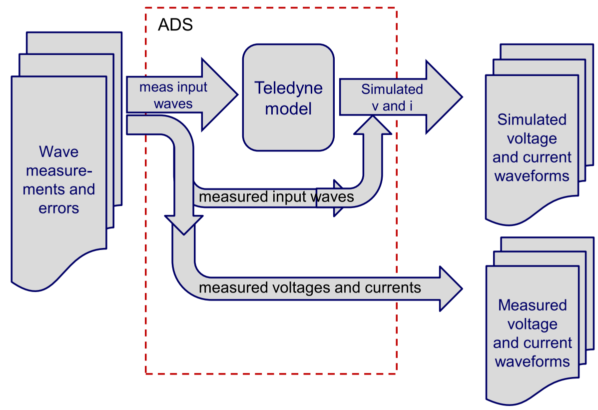


Fig. 1. Approach we used to verify an HBT foundry model in [15]. We programmed ADS to read in the measured wave parameters, simulate the response of the HBT model to the input waves, and convert the input and output waves to voltage and current waveforms. (Image courtesy of [15].)

A number of authors have studied two-tier approaches [1]–[5] and parasitic extraction techniques [5]–[8] to improve transistor characterization. Lin and Zhang [9] studied error propagation in large-signal network analysis. Lenk and Rudolph [10] performed a very interesting sensitivity analysis of an HBT extraction process. They used it as a tool for evaluating the sensitivity of the extraction process to measurement error and identifying poorly conditioned models. Miranda *et al.* [11] studied the impact of on-wafer calibration kits on the extraction of HEMT models at microwave frequencies. Williams *et al.* [12], [13] argue that on-wafer thru–reflect–line (TRL) calibrations improve the accuracy of HBT and CMOS transistor measurements.

Avolio *et al.* [14] examined the impact of measurement uncertainty on transistor capacitances and the temporal current and voltage waveforms and impedances at the transistor current generator plane and used the measurements to develop a measurement-based transistor model. Williams *et al.* [15] considered the impact of measurement uncertainties during the verification of the performance of a foundry model for a state-of-the-art HBT with large-signal measurements. As illustrated in Fig. 1, we compared the measured behavior of the transistor under large-signal operating conditions with its simulated performance. In general, we found very good agreement between the measurements and simulations.

However, by propagating our measurement uncertainties through the verification procedure, we were able to eliminate measurement error as a source of the discrepancies we observed. Nevertheless, we were not able to eliminate process variation as a source of discrepancies in our measurements and simulations. This left open the possibility that process variations might account for some of discrepancies we observed, not the inability of the foundry model to predict large-signal performance accurately.

Here, we refine the model verification procedure and eliminate both measurement uncertainties and process variations as contributors to the discrepancies between our large-signal verification measurements and simulations. We do this using the same transistor for both the model parameter extraction and model verification steps.

II. Foundry-Model Verification

Fig. 1 shows the model verification procedure we used in our prior work [15]. The transistors we studied were fabricated at Teledyne Scientific with a state-of-the-art 250-nm HBT process. Teledyne Scientific also provided the foundry model studied in [15]. This model was based on version 2.0 of the Keysight[1] HBT model implemented in their Advanced Design System (ADS) software (see [16]). The parameters used in the model were extracted at Teledyne Scientific from dc and small-signal measurements with a proprietary approach.

Williams *et al.* [15] were able to verify the ability of the Teledyne model to predict the behavior of an HBT with a 6 μm $\times$ 250 nm emitter under large-signal excitation and evaluate the impact of measurement errors on the verification procedure. However, we were not able to accurately identify possible deficiencies in the model because we were not able to estimate the impact of process variation in the verification procedure. This was because the transistors used at Teledyne to develop their foundry model and the transistors we used to verify the foundry model were processed in different fabrication lots many months apart.

III. Refined Model Verification Approach

In this paper, we eliminate process variations from our verification procedure using the Keysight ICCAP software to extract our own model parameters for the Keysight version 2.0 HBT model. This allowed us to use the same transistors for both model extraction and verification and to eliminate process variations from the verification procedure.

We did this by propagating our scattering parameter, power, and electrical phase measurement uncertainties through the refined verification procedure and using this information to determine when the differences in transistor behavior predicted by the ICCAP model and the measured transistor behavior were significant.[2] We are then able to attribute those differences to the ability of the model to predict transistor behavior under large-signal operating conditions without clouding the picture with unaccounted-for process variations in the experiment.

[1] We identify commercial products only to accurately describe the experiments and analysis we performed. The NIST does not endorse commercial products. Other products may work as well or better.

[2] We are unaware of a dc uncertainty analysis that includes correlations at this time. Thus, we did not include uncertainties in our dc measurements in our analysis.

A. Calibration

Williams *et al.* [12], [13] found that accurate calibrations improve the model extraction processes. We used the custom TRL on-wafer calibration kit described in [12] to calibrate the scattering parameters and wave parameters measured in this study. We had two reasons for this choice.

First, we have shown in prior work that on-wafer TRL calibration kits allow the measurement reference plane to be moved right next to the transistor under test. In this way, parasitics associated with the contact pads and access line can be removed from the scattering parameter calibrations and the voltages and currents at the transistor terminals can be measured with greater fidelity than is possible with other methods.

Second, the TRL calibration is based on transmission line propagation. It rigorously solves for forward- and backward-wave amplitudes and then constructs voltages and current waveforms from those amplitudes in a clearly defined way. As a result, the systematic errors of the TRL calibration are few and easily characterized with simple well-understood models. This made it much easier for us to identify and track correlations throughout the analysis.

We used a conventional first-tier 2.4-mm short–open–load–thru (SOLT) calibration to perform the power and phase calibrations needed to fix the wave amplitudes and phases of the large-signal measurements we made. We first performed the 2.4-mm SOLT calibration and then connected a power meter to the analyzer, and simultaneously recorded the power reported by the meter and the amplitude and phases of the waves measured by the network analyzer. Then we connected a traceable harmonic phase reference to the network analyzer and measured the phases measured by the network analyzer's receivers. Finally, we transferred these calibrations to the on-wafer reference plane by performing a second-tier TRL calibration with the built-in calibration modules in the National Institute of Standards and Technology (NIST) Microwave Uncertainty Framework. This procedure transfers the magnitude and phase calibrations from the 2.4-mm SOLT calibration to the on-wafer reference plane of the TRL calibration located right next to the transistor.

B. Refined Verification Approach

Fig. 2 illustrates our refined approach to develop models with ICCAP from dc and small-signal scattering parameter measurements and verify the large-signal performance of those models. To develop the models, we used a Hewlett-Packard[3] HP4142B modular dc source and monitor and a Keysight PNA vector network analyzer to measure the dc I–V curves and small-signal scattering parameters used in the ICCAP parameter extraction procedure.

We verified the models with a Keysight PNA-X, which we used to excite the transistor in a common–emitter configuration with a 1-GHz sine wave and drive it into a large-signal operating state. We then used the PNA-X to measure the incoming and outgoing waves from 1 to 25 GHz at an on-wafer reference plane next to the transistor as a function of

[3] Now Keysight Technologies.

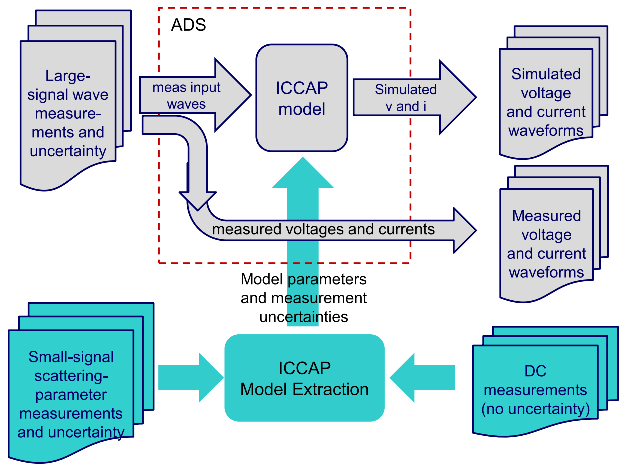
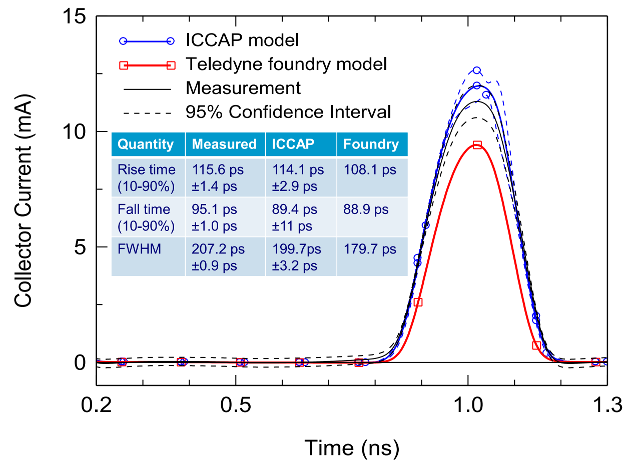
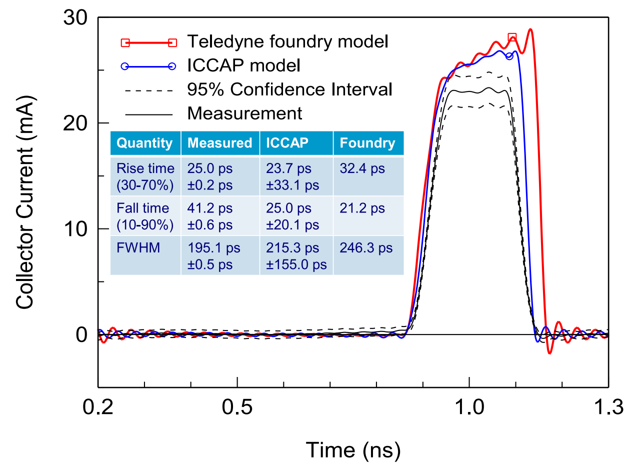


Fig. 2. Refined verification approach. Process variations were eliminated from the verification procedure by performing model extraction on the same transistor used in the verification procedure. Measurement uncertainties were accounted for in both the model extraction and verification procedures.



Quantity	Measured	ICCAP	Foundry
Rise time (10-90%)	115.6 ps ±1.4 ps	114.1 ps ±2.9 ps	108.1 ps
Fall time (10-90%)	95.1 ps ±1.0 ps	89.4 ps ±11 ps	88.9 ps
FWHM	207.2 ps ±0.9 ps	199.7ps ±3.2 ps	179.7 ps

Fig. 3. Transistor collector current, pulse parameters, and uncertainties in deep class A/B at a -5-dBm drive level with bias $V_c = 1$ V and $I_c = 2$ mA.



Quantity	Measured	ICCAP	Foundry
Rise time (30-70%)	25.0 ps ±0.2 ps	23.7 ps ±33.1 ps	32.4 ps
Fall time (10-90%)	41.2 ps ±0.6 ps	25.0 ps ±20.1 ps	21.2 ps
FWHM	195.1 ps ±0.5 ps	215.3 ps ±155.0 ps	246.3 ps

Fig. 4. Transistor collector current, pulse parameters, and uncertainties in deep compression at a $+5$-dBm drive level with bias $V_c = 1.8$ V and $I_c = 8$ mA. The differences in the shapes of the measured and simulated collector current waveforms are much greater in deep compression. The uncertainties in the collector current derived from simulations based on the ICCAP model are shown in Fig. 5 for clarity.

the transistor's dc bias state and the drive level of the 1-GHz fundamental. Finally, we used the Keysight ADS software package to emulate our measurement setup, drive the transistor model with the same incoming waves we measured, and simulate the output waves generated by the transistor and the voltages and currents at the transistor terminals.

Throughout this process, we used the NIST Microwave Uncertainty Framework [17] to propagate our measurement uncertainties through both the ICCAP model extraction procedure and the ADS model verification procedure. This allowed us to track and account for correlations at all stages of the measurements and analysis (see the Appendix). Finally, we calculated the voltage and current waveforms at the transistor terminals from our measurements and simulations and compared them with each other.

IV. Model Verification

We measured the response of our HBTs to a 1-GHz drive signal under large-signal operating conditions at a number of bias states. We varied the drive level of that signal from -25 dBm to $+5$ dBm, sweeping through regions of linear operation, deep class A/B operation, and finally deep compression. We explored the behavior of the ICCAP model extracted from the transistors and the foundry model provided by Teledyne Scientific in all of these regions of operation.

A. Deep Class A/B Operation

We found excellent agreement between the measured and predicted base and collector voltage and current waveforms up to a transistor drive level of about -5 dBm. Fig. 3 shows an example at a -5-dBm drive, which exhibited the worst performance over this range and corresponds to deep class AB operation. Here, we see that the ICCAP model does a better job of reproducing the measured results in Fig. 3 than the foundry model, as we might expect. Furthermore, the differences between the ICCAP simulations and measurements are comparable to the uncertainties we estimated.

Nevertheless, the agreement between the ICCAP simulations and the measurements in Fig. 3 could be better. Furthermore, the inset table of Fig. 3 reveals that the differences between the measured and the collector current rise time, fall time, and full-width-half-maximum (FWHM) simulated with the ICCAP model cannot be entirely explained by our estimates of the uncertainty in the measurements.

B. Deep Compression

When the drive level exceeded 0 dBm, the discrepancies between simulations and our verification measurements became quite observable. Fig. 4 compares the measured collector currents and their uncertainties at a drive level of $+5$ dBm to ADS simulations based on the two models.

The simulated collector current in Fig. 4 rings with an approximately 0.05-ns period. This ringing is due to the finite number of harmonics (25 in this case) we used in the measurements and simulations. This ringing is also observable at a lower level in the measurements. This ringing is especially

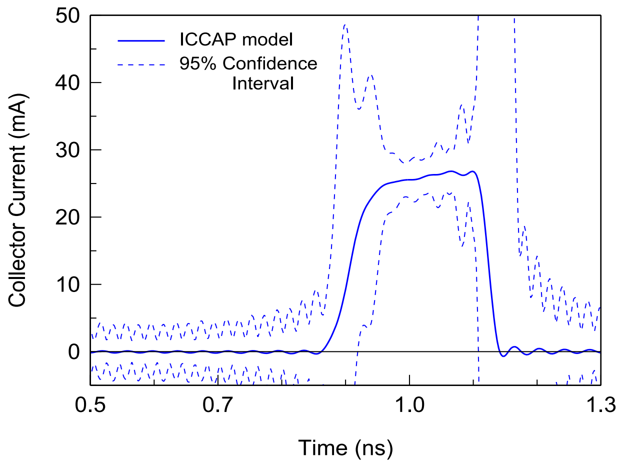


Fig. 5. Uncertainties of the transistor collector current waveform derived from simulations based on the ICCAP model in deep compression at a +5-dBm drive level with bias $V_c = 1.8$ V and $I_c = 8$ mA. The large uncertainty levels are due to instability in the extraction procedure.

pronounced in the simulations based on the Teledyne model because of the very fast collector current fall time predicted by this model. While we were capable of including more harmonics in the harmonic balance simulations performed by ADS, we found that convergence was difficult to realize when we increased the number of harmonics beyond 25.

Ignoring the ringing, we can still clearly see that the model we extracted from ICCAP does a better job of matching the rise time, fall time, and duration of the collector current pulse than the foundry model we investigated in [15]. This could be because the ICCAP model was built from the same transistor used in the model verification process.

In any case, we see that both simulations fall well outside of the uncertainties of the measured collector current waveform. In the case of the foundry model, these differences could be attributed to an imperfect model or process variations, or both. However, in the case of the ICCAP model, these differences cannot be attributed to process variations or measurement errors. In this case, we must conclude that the ICCAP parameter extraction procedure and/or the HBT model we used were imperfect.

The uncertainties in the collector current rise time, fall time, and FWHM simulated with the ICCAP model listed in the inset table of Fig. 4 are significantly larger than those in Fig. 3.[4]

Fig. 5 shows the uncertainties in the collector current waveform calculated from the ICCAP model, and they are also considerably larger than the uncertainties in Fig. 3. These uncertainties in the simulations based on the ICCAP model seem unexpectedly high, at least when compared with the uncertainties in our measurements.

C. Interpretation of Uncertainty in Simulated Results

We certainly expect that errors in the measurements used to extract models and errors in the measurements of the large-signal drive level and impedances presented to the transistor during the verification process will propagate through our analysis and impact the accuracy of our simulations. The procedure we used in Fig. 2 was designed to propagate our estimates of these measurement errors (our uncertainties) through the entire analysis, including our simulations.

What is interesting about Figs. 4 and 5 are that the uncertainties in our simulated results due to measurement errors are plotted in the same collector current waveform space as our direct measurements, making it easy to compare our measured and simulated uncertainties. The same can be said of the collector current pulse parameters listed in the inset table of Fig. 4.

Normally, we would expect that fitting a model to measured data would smooth out and average over errors in measured data. Thus, we would normally expect the resulting uncertainties in our simulated collector current waveforms to be comparable to or lower than our measured uncertainties in those waveforms.

However, in this case, the uncertainties in our simulated collector current waveforms, as defined by the curves in Figs. 4 and 5 and the metrics listed in the inset table of Fig. 4, are clearly much larger than the uncertainties in the measurements. From this, we conclude that there must be some instability in the model or parameter extraction procedure used in ICCAP. This could be due to insufficient measurement data used during the extraction procedure or due to the use of redundant and/or nonphysical parameters in the model [10].[5]

D. Uncertainty Propagation Through the ICCAP Model Extraction Procedure

No measurements are perfect, including the measurements we used in ICCAP to extract the HBT model parameters. Thus, the errors in these measurements will add error to the HBT model parameters extracted by ICCAP. We used the NIST Microwave Uncertainty Framework to propagate our measurement uncertainties through the ICCAP model extraction procedure. That allowed us to estimate the uncertainties of the model parameters determined by ICCAP due to the errors in the measurements used in the model parameter extraction procedure. Table I lists a few representative parameters and their uncertainties.

We first investigated the impact of the specific physical parameters responsible for the errors in Table I. We were not able to identify a single physical parameter that stood out as the overall driver behind the uncertainties listed in Table I. Rather, a relatively small number of errors in the on-wafer

[4]We show 30%–70% rise times in Fig. 4 because the 90% point on the rising edge of the collector current pulse is situated on the gently upward sloping top of the simulated pulses. This makes it difficult to compare the simulated and measured rise times with each other.

[5]Insufficient data used in the extraction procedure may render the extraction procedure very sensitive to noise or other small errors in the measurements. For example, if we restricted the measurement data used to fit $y = a + bx$ to very small values of x, we would be able to determine a accurately, but may not be able to determine b accurately in the presence of measurement errors. In extreme cases, insufficient data may even result in underdetermined problems, leading to multiple solutions.

Likewise, nonphysical models, particularly if they include a large number of nonphysical parameters to describe phenomena that can be described with only a few physical parameters, can render the extraction procedure very sensitive to small measurement errors as well, and even lead to multiple solutions in extreme cases.

TABLE I
EXTRACTED ICCAP MODEL PARAMETERS

Parameter	Units	Nominal Value	Standard Uncertainty	Relative Uncertainty
IS	fA	1.39	± 0.09	6 %
CJC	fF	12.1	± 1.1	9 %
TFC0	fs	355	± 55	15 %
TCMIN	fs	74	± 43	58 %
IKRK	mA	46	± 161	350 %

TRL calibration, including probe placement and transmission line geometries, seemed to play roughly equal roles in generating the uncertainties listed in Table I. This is not surprising, given that the multiline calibrations we use are highly redundant and errors are spread out over a number of calibration standards and error mechanisms.

Table I shows that ICCAP did a good job of extracting model parameters like the transistor's saturation current IS, collector capacitance CJC, and low-current transit time TFC0 despite the errors in the small-signal measurements that we used in the extraction procedure. These parameters are needed to simulate small-signal and high-frequency transistor behaviors as well as transit times when current flow through the transistor is low.

However, Table I also reveals that the ICCAP extraction procedure did not do nearly as good a job of determining the high-current transit time TCMIN from our measured data and completely failed to determine the Kirk effect critical current IKRK accurately. These model parameters are used to calculate transit times when current flow through the transistor is very high, such as with the high currents generated in deep compression, as plotted in Figs. 4 and 5.

These results point to difficulty in the ICCAP extraction procedure used to determine TCMIN, IKRK, and other parameters used to predict the collector transit time in deep compression. It appears that the underlying problem may be related to a nonphysical fit used to model the collector transit time in the Kirk effect region. Further study indicated that adjusting the parameters that determine the collector transit time in the Kirk effect region to better match our large-signal measurements led to a distinct lack of fit with the small-signal measurements used in the ICCAP model parameter extraction process. Thus, we see that propagating measurement uncertainties through the parameter extraction process can also be useful in identifying specific deficiencies in both the construction of the transistor model and the associated parameter extraction procedure.

Finally, we examined the probability density functions we calculated for the various parameters in Table I. We found that the probability density functions for IS, CJC, and TFC0 were quite smoothly distributed about the mean, as we might expect. However, the probability density functions associated with TCMIN and IKRK were quite irregular. This is another indication of instability in the model parameter extraction process.

V. CONCLUSION

We verified the ability of the ICCAP model extraction procedure to generate models that predict the performance of HBTs under deep class A/B operating conditions. However, we found that the model we extracted was not able to accurately predict transistor behavior in deep compression.

After eliminating process variations as significant contributors to the differences we observed, we were able to show that the difficulty in predicting transistor behavior in deep compression was related to instability in the ICCAP parameter extraction procedure.

We then propagated our uncertainties through the ICCAP extraction procedure and assigned uncertainties to the model parameters extracted by ICCAP. This in turn led to the identification of the parameters that were determined accurately in the extraction procedure and those that were not.

In this particular case, we found that ICCAP determined most of the parameters of the model quite accurately. However, an examination of the uncertainties in the model parameters we extracted with ICCAP showed that we were not able to accurately determine some parameters in the model needed to characterize the transit time and Kirk effect in deep compression, where the fits used to model the transit time appeared to not be physical. This offered an explanation for the differences we observed between our large-signal verification measurements and simulations in deep compression.

These results illustrate the utility of propagating measurement uncertainties through the model extraction and verification procedure and suggest a general strategy for leveraging correlated measurement uncertainties in model validation. Not only does the uncertainty analysis aid in clarifying the results of the verification process, but it can identify the accuracy with which individual model parameters were extracted.

A full uncertainty analysis will require adding process variations to the model. This should not be difficult at all in the framework we have adopted for propagating uncertainty. However, additional work will also be required to better quantify errors due to a lack of physicalness of the model, perhaps relying on cross-validation approaches. Even so, we expect to be able to propagate measurement uncertainties all the way through the circuit design process and predict the accuracy of circuit simulations based on models extracted from the measurement.

APPENDIX
UNCERTAINTY PROPAGATION

Fig. 6 illustrates how the NIST Microwave Uncertainty Framework allowed us to track and account for correlations in the measured and simulated voltage and current waveforms we compared. Fig. 6 illustrates how calculations are performed with a single input and a single output. However, the NIST Microwave Uncertainty Framework allows for multiple inputs as well and includes algorithms for ensuring that elements in the sensitivity analysis are not double counted.

At each stage of the calculation, each result and its uncertainty is represented by a single vector containing a nominal measurement or simulation result, a series of vectors containing measured or simulated results from a sensitivity analysis, and a series of vectors containing measured or simulated results from a Monte Carlo simulation. This structure is

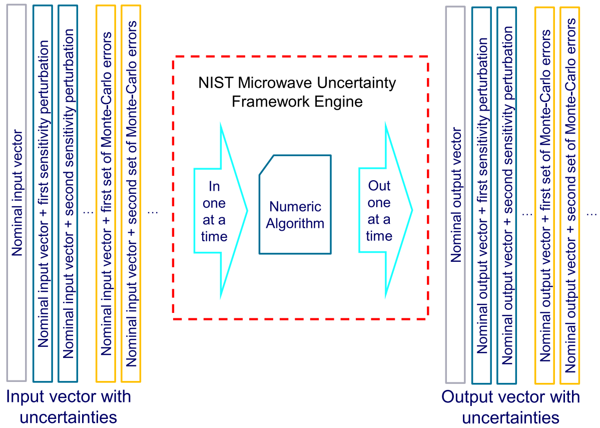


Fig. 6. Approach used for uncertainty propagation by the NIST Microwave Uncertainty Framework. (Image courtesy of [15].)

designed to maintain frequency-domain and temporal correlations between the elements of these vectors.

Depending on the stage of the analysis, these vectors contained lists of complex wave parameters measured by the vector network analyzer at the first 25 harmonics of the 1-GHz drive frequency, temporal voltage or current waveforms at the transistor terminals, or various metrics determined from these waveforms.

Over 400 sources of uncertainty were required in the uncertainty analysis to separately capture all the individual error mechanisms in the measurements. Each of these uncertainty sources modeled a single physical error mechanism in the experiment and was assigned a unique name. These names were used by the NIST Microwave Uncertainty Framework to "turn ON" each error mechanism once and only once at each stage of the sensitivity analysis. These names also serve to capture and track the impact of each physical error mechanism throughout the experiment, even when artifacts are used repeatedly in different steps of the analysis.

The NIST Microwave Uncertainty Framework generates unique seeds for use in the Monte Carlo analyses from the name assigned to each error mechanism in the analysis. This allows the uncertainties for each error mechanism in an artifact to be generated separately in different parts of the analysis and still be properly correlated when combined later into a single result.

This attention to correlations is important in this application. The errors in measuring the small-signal scattering parameters used in the ICCAP model extraction process must be propagated through the simulation process before the simulated voltages and currents can be calculated and compared with the measured voltage and current waveforms at the transistor terminals. In addition, the errors in measuring the large-signal amplitudes and phases of the incoming and outgoing waves during the model verification must be tracked as well.

As in [15], we tracked correlations in our measurement uncertainties through the Fourier transform to generate temporal results (e.g., collector current waveforms) and to the various metrics describing those waveforms (e.g., collector current rise and fall times). However, in this paper, we also tracked correlations in our measurement uncertainties through the parameter extraction procedure to the model parameters we examined (e.g., HBT saturation current and collector capacitance). Finally, we used the same on-wafer calibration artifacts in both the model parameter extraction and model verification procedures. Again, we used the NIST Microwave Uncertainty Framework and its built-in correlation tracking capabilities to track and correctly account for all of these correlations throughout the analysis.

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References

[1] Q. Liang *et al.*, "A simple four-port parasitic deembedding methodology for high-frequency scattering parameter and noise characterization of SiGe HBTs," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 11, pp. 2165–2174, Nov. 2003.

[2] Q. Liang, W.-M. Kuo, J. D. Cressler, A. J. Joseph, and D. L. Harame, "Accurate AC transistor characterization to 110 GHz using a new four-port self-calibrated extraction technique," in *Proc. IEEE Topical Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Sep. 2004, pp. 282–285.

[3] X. Wei *et al.*, "An improved on-chip 4-port parasitics de-embedding method with application to RF CMOS," in *Proc. Topical Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Dec. 2007, pp. 24–27.

[4] L. F. Tiemeijer, R. J. Havens, A. B. M. Jansman, and Y. Bouttement, "Comparison of the 'pad-open-short' and 'open-short-load' deembedding techniques for accurate on-wafer RF characterization of high-quality passives," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 723–729, Feb. 2005.

[5] K. Yau, E. Dacquay, I. Sarkas, and S. P. Voinigescu, "Device and IC characterization above 100 GHz," *IEEE Microw. Mag.*, vol. 13, no. 1, pp. 30–54, Jan./Feb. 2012.

[6] A. Rumiantsev, P. Sakalas, N. Derrier, D. Celi, and M. Schroter, "Influence of probe tip calibration on measurement accuracy of small-signal parameters of advanced BiCMOS HBTs," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Sep. 2011, pp. 203–206.

[7] A. Rumiantsev, S. L. Sweeney, and P. L. Corson, "Comparison of on-wafer multiline TRL and LRM+ calibrations for RF CMOS applications," in *72nd Autom. RF Techn. Group Conf. Dig.*, Dec. 2008, pp. 132–136.

[8] A. Rumiantsev, P. L. Corson, S. L. Sweeney, and U. Arz, "Applying the calibration comparison technique for verification of transmission line standards on silicon up to 110 GHz," in *Autom. RF Techn. Group Conf. Dig.*, vol. 73. Dec. 2009, pp. 1–6.

[9] M. Lin and Y. Zhang, "Covariance-matrix-based uncertainty analysis for NVNA measurements," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 1, pp. 93–102, Jan. 2012.

[10] F. Lenk and M. Rudolph, "Extraction of GaAs-HBT equivalaent circuit considering the impact of measurement errors," *Innov. Microw. Light, Res. Rep. Ferdinand-Braun-Institut fur Hochstrfrequenztechnik*, vol. 3, pp. 95–103, 2015.

[11] J. M. Miranda, C. Fager, H. Zirath, P. Sakalas, S. Munoz, and J. L. Sebastian, "Influence of the calibration kit on the estimation of parasitic effects in HEMT devices at microwave frequencies," *IEEE Trans. Instrum. Meas.*, vol. 51, no. 4, pp. 650–655, Aug. 2002.

[12] D. F. Williams, A. C. Young, and M. Urteaga, "A prescription for sub-millimeter-wave transistor characterization," *IEEE Trans. THz Sci. Technol.*, vol. 3, no. 4, pp. 433–439, Mar. 2013.

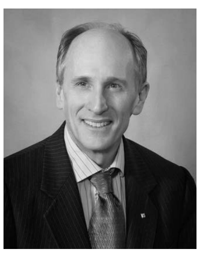
[13] D. F. Williams *et al.*, "Calibration-kit design for millimeter-wave silicon integrated circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2685–2694, Jul. 2013.

[14] G. Avolio, A. Raffo, J. Jargon, P. D. Hale, D. M. M.-P. Schreurs, and D. F. Williams, "Evaluation of uncertainty in temporal waveforms of microwave transistors," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 7, pp. 2353–2363, Jul. 2015.

[15] D. Williams, W. Zhao, R. Chamberlin, J. Cheron, and M. Urteaga, "Verification of a foundry-developed transistor model including measurement uncertainty," in *87th ARFTG Microw. Meas. Conf. Dig.*, May 2016, pp. 1–4.

[16] M. Iwamoto *et al.*, "Avanzo, "Large-signal HBT model with improved collector transit time formulation for GaAs and InP technologies," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2. Jun. 2003, pp. 635–638.

[17] D. F. Williams and A. Lewandowski. (2011). NIST Microwave Uncertainty Framework. Nat. Inst. of Standards and Technol. [Online]. Available: http://www.nist.gov/ctl/rf-technology/related-software.cfm



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