

New Methods for Series-Resistor Calibrations on Substrates With Losses Up to 110 GHz

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Abstract—We present two new methods to perform series-resistor calibrations on substrates with losses. Lossless calibration substrates, which are required by the traditional calibration comparison technique, are not needed. The proposed methods rely on multilayer thru-reflect-line-calibrated series-resistor and series-capacitor data. The first method uses closed-form equations and the second method is based on multifrequency optimization. The proposed methods are based on a fundamental assumption that the resistance and the inductance of series-resistor standards fabricated with thin-film technologies are frequency-independent. In addition, an improved version of the traditional calibration comparison technique is proposed and is used as the benchmark technique. By measurement results on a high-resistivity silicon substrate up to 110 GHz, the validity of the proposed approaches is demonstrated.

Index Terms—Calibration, calibration comparison, impedance standards, millimeter wave measurement, series-resistor, silicon.

I. INTRODUCTION

ON-WAFER multilayer thru-reflect-line (MTRL) calibration is an accurate calibration method for characterizing transistors, circuits, and systems [1] at millimeter wave frequencies. On-wafer series-resistor calibration provides a broadband calibration comparable with MTRL calibration with a more compact area and smaller number of measurements [2], [3]. Once the series-resistor and the reflect standards are characterized, only the thru, the series-resistor,

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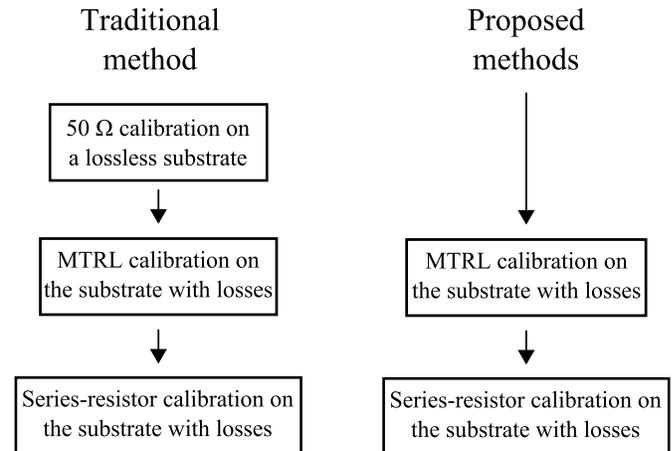


Fig. 1. Flowchart of performing series-resistor calibrations on substrates with losses using the traditional method (left) and the proposed methods (right).

and the reflect standards need to be measured to calibrate the vector-network-analyzer. The number of measurements is thus only three, which saves measurement time compared with performing MTRL calibrations.

Series-resistor calibration standards are normally characterized by an MTRL calibration on the same calibration substrate. Since the TRL method gives calibrated data referenced to the line impedance [4], a separate measurement of the line impedance has to be performed. For a lossless and dispersionless substrate, the line impedance can be measured with the series-resistor at low frequencies [3]. For substrates with losses and dispersion, the line impedance has to be measured with the calibration comparison technique, which requires a separate lossless and dispersionless substrate [5]. As a result, how to perform series-resistor calibrations on substrates with losses and dispersion without using extra substrates remains a question.

In this paper, we propose two general methods to perform series-resistor calibrations. The proposed methods do not require any extra calibration substrates and apply to both lossless substrates and substrates with losses. A simple flowchart of doing series-resistor calibrations on substrates with losses is shown in Fig. 1. Our methods directly extract all the model parameters of the series-resistor calibration standards from MTRL-corrected data. The proposed methods make use of a fundamental assumption that in the gigahertz frequency range, the resistance and the inductance of thin-film series-resistors are frequency-independent. The resistance of thin-film series-resistors is dominated by the resistance of the resistive filament. Because of the high resistivity

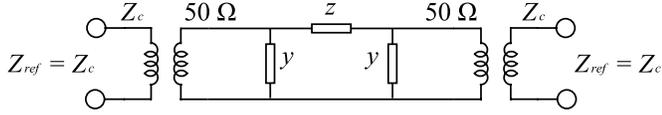


Fig. 2. Pi-network with reference impedance equal to Z_c .

and the low thickness of the resistive filament, in a normal on-wafer measurement frequency range, e.g., dc-110 GHz, its resistance is equal to its dc value. Although the resistive filament is not affected by the skin effect, the ground conductors next to the resistive filament are slightly affected because of their higher thickness and conductivity. However, in the gigahertz frequency range, the introduced inductance dispersion is very small, only a few percent of the total inductance of the series-resistor [6]. As a result, in this paper, both the resistance and the inductance of thin-film series-resistors are assumed to be frequency-independent. We compare series-resistor calibrations produced using the proposed new methods and using the traditional calibration comparison method (“cal comp”), and show that they are similar up to 110 GHz.

This paper is organized as follows. The general series-resistor model for lossless substrates and substrates with losses is presented in Section II. A closed-form equation method is proposed in Section III of this paper, followed by a multifrequency optimization method (“multifreq”) presented in Section IV. Section V presents the experimental validation of the proposed methods. In the end, some conclusions are drawn. In the Appendix, an improved calibration comparison method is presented, which is used as the benchmark method.

II. CALIBRATION STANDARD MODELING

In this section, general lumped element models of the series-resistor and the series-capacitor standard are introduced. First, a general Pi-network with the complex reference impedance equal to Z_c is shown in Fig. 2. The relationship between its S -parameters and the circuit model parameters can be described as follows [7]:

$$\begin{aligned} S_{21} &= \frac{2}{(y \cdot Z_c + 2)(y \cdot z + 2) + \frac{y \cdot z}{y \cdot Z_c} - 2} \\ S_{11} &= \frac{1 - y \cdot Z_c}{1 + y \cdot Z_c} - S_{21} \end{aligned} \quad (1)$$

where y and z are the admittance and the impedance in the network. Due to symmetry, only half of the S -parameters need to be considered.

From (1), $y \cdot Z_c$ and $y \cdot z$ can be straightforwardly solved as follows:

$$\begin{aligned} y \cdot Z_c &= \frac{1 - S_{11} - S_{21}}{1 + S_{11} + S_{21}} \\ y \cdot z &= \frac{\frac{2}{S_{21}} - 2 \cdot (y \cdot Z_c + 1)}{2 + y \cdot Z_c + \frac{1}{y \cdot Z_c}}. \end{aligned} \quad (2)$$

Fig. 3 shows a schematic of the series-resistor standard used for calibrations embedded in coplanar waveguides (CPWs). In the frequency range of interest (dc-110 GHz), when calibrated to the resistive filament in the middle of the figure, the series-resistor is electrically small compared with the

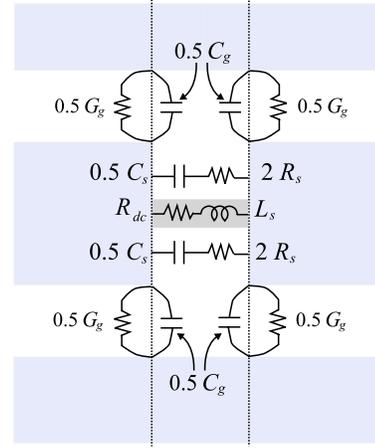


Fig. 3. Schematic of the series-resistor standard with its parasitics defined at the reference plane indicated by the dashed lines. The resistive filament is modeled by its dc resistance R_{dc} and its frequency-independent parasitic inductance L_s . The parasitic coupling between the CPW center conductors is modeled by the series-capacitor C_s . R_s in series with C_s models the substrate losses. Fringing capacitance between the CPW center conductors and the ground planes is modeled by C_g . In parallel with C_g , G_g also models the substrate losses.

wavelength, so it can be modeled by a network of lumped elements, as shown in the figure. In this paper, our previous model for lossless substrates [3] is extended for substrates with losses. The resistive filament is modeled by its dc resistance R_{dc} and its frequency-independent parasitic inductance L_s . Similar to the previous model, a series-capacitor C_s is used to account for the coupling between the CPW center conductors, and a shunt capacitor to ground C_g is used to model the fringing capacitance between the CPW center conductors and the ground planes. In this extended model, loss elements R_s and G_g are added to the capacitive part of the model to account for substrate losses. For the general case, the parasitic capacitances and their losses are modeled as frequency-dependent.

Fig. 4 shows the lumped models for the series-resistor and the series-capacitor. The series-capacitor has the same physical geometry as the series-resistor except for the resistive filament, so its lumped model is the same as the series-resistor, just without R_{dc} and L_s . The reference impedance of the S -parameters of the series-resistor and series-capacitor standards is equal to the characteristic impedance of the transmission lines connected to them, which is Z_c . In practice, these S -parameters are obtained after correcting the raw measurement data with an on-wafer MTRL calibration.

From (2), MTRL-corrected measurements of the series-resistor and the series-capacitor standards provide measurements of the following products:

$$\text{Series-capacitor: } p_1 = y_g \cdot Z_c \quad (3a)$$

$$p_2 = y_g \cdot z_s \quad (3b)$$

$$\text{Series-resistor: } p_3 = y_g \cdot Z_c \quad (3c)$$

$$p_4 = y_g \cdot \frac{1}{1/z_r + 1/z_s} \quad (3d)$$

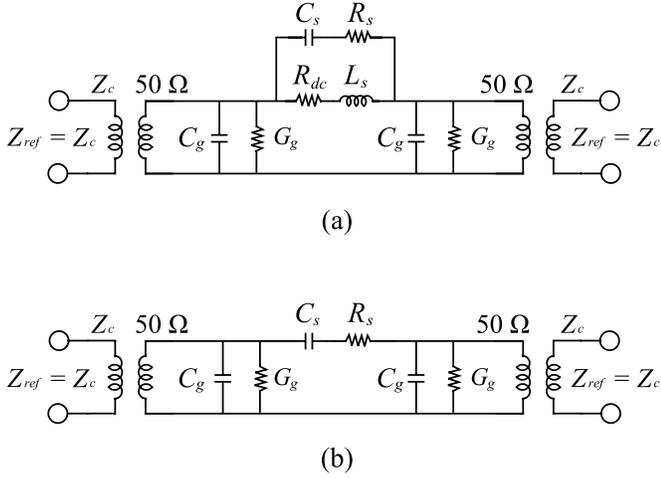


Fig. 4. Equivalent circuit models for (a) series-resistor standard and (b) series-capacitor standard. The reference plane location is indicated by the dashed line in Fig. 3.

where

$$y_g = j\omega \cdot C_g + G_g \quad (4a)$$

$$z_r = R_{dc} + j\omega \cdot L_s \quad (4b)$$

$$z_s = R_s + \frac{1}{j\omega C_s}. \quad (4c)$$

III. CLOSED-FORM EQUATIONS METHOD

In this section, closed-form equations solving the series-resistor and series-capacitor model parameters in Fig. 4 from MTRL-corrected products in (3) are presented. Several assumptions are made regarding the loss elements in the standards to ease the model extraction procedure without losing much accuracy. These assumptions will be checked in the validation section for the example presented and are proven to be reasonable in the frequency range of interest.

Simple manipulations on the products in (3) result in the following important quantity:

$$p_5 = \frac{1}{\frac{p_3}{p_4} - \frac{p_1}{p_2}} \cdot \gamma = \frac{z_r}{Z_c} \cdot \gamma \quad (5)$$

where γ is the propagation constant of the transmission lines connected to the series-resistor standard measured from the MTRL calibration. Since γ and Z_c are related to each other through the following relationship:

$$Z_c = \frac{\gamma}{j\omega \cdot C_{\text{unit}} + G_{\text{unit}}} \quad (6)$$

where C_{unit} and G_{unit} are the capacitance and conductance per unit length on the calibration substrate, the product p_5 can be expanded as follows:

$$\text{Re}(p_5) = R_{dc} \cdot G_{\text{unit}} - \omega^2 L_s \cdot C_{\text{unit}} \quad (7a)$$

$$\text{Im}(p_5) = \omega(L_s \cdot G_{\text{unit}} + R_{dc} \cdot C_{\text{unit}}). \quad (7b)$$

Next, the procedures to extract the line capacitance per unit length C_{unit} , the conductance per unit length G_{unit} ,

and the load inductance L_s are explained. Expanding (7b), the following equation about C_{unit} is obtained:

$$C_{\text{unit}} = \frac{\text{Im}(p_5)}{\omega R_{dc}} \cdot \left(1 - \frac{\omega L_s \cdot G_{\text{unit}}}{\text{Im}(p_5)}\right) \quad (8)$$

which allows C_{unit} to be approximated by

$$C_{\text{unit}} \approx \frac{\text{Im}(p_5)}{\omega R_{dc}} \quad (9)$$

with a relative error of

$$\begin{aligned} \frac{\Delta(C_{\text{unit}})}{C_{\text{unit}}} &= \frac{\omega L_s \cdot G_{\text{unit}}}{\text{Im}(p_5)} \\ &= \frac{\omega L_s \cdot G_{\text{unit}}}{\omega L_s \cdot G_{\text{unit}} + \omega R_{dc} \cdot C_{\text{unit}}} \\ &= \frac{\frac{L_s \cdot G_{\text{unit}}}{R_{dc} \cdot C_{\text{unit}}}}{1 + \frac{L_s \cdot G_{\text{unit}}}{R_{dc} \cdot C_{\text{unit}}}}. \end{aligned} \quad (10)$$

In practical situations, the ratio $(L_s \cdot G_{\text{unit}})/(R_{dc} \cdot C_{\text{unit}})$ is small, so the above expression is approximated to be

$$\frac{\Delta(C_{\text{unit}})}{C_{\text{unit}}} \approx \frac{L_s \cdot G_{\text{unit}}}{R_{dc} \cdot C_{\text{unit}}}. \quad (11)$$

The loss tangents of the substrate and the series-resistor are defined as

$$\tan \delta_{C_{\text{unit}}} = \frac{G_{\text{unit}}}{\omega C_{\text{unit}}} \quad (12a)$$

$$\tan \delta_{R_{dc}} = \frac{R_{dc}}{\omega L_s} \quad (12b)$$

which allow (11) to be rewritten as

$$\frac{\Delta(C_{\text{unit}})}{C_{\text{unit}}} = \frac{\tan \delta_{C_{\text{unit}}}}{\tan \delta_{R_{dc}}} \quad (13)$$

which is a small number in practice.

Once C_{unit} is extracted with high precision, the load inductance L_s can be estimated. Since the reactance of an inductor increases with frequency, it is beneficial to extract L_s at high frequencies. By expanding (7a), an expression for the load inductance can be obtained

$$L_s = -\frac{\text{Re}(p_5)}{\omega^2 C_{\text{unit}}} \cdot \left(1 - \frac{R_{dc} \cdot G_{\text{unit}}}{\text{Re}(p_5)}\right). \quad (14)$$

From the above expression, L_s can be estimated as

$$L_s \approx -\frac{\text{Re}(p_5)}{\omega^2 C_{\text{unit}}} \quad (15)$$

with a relative error of

$$\begin{aligned} \frac{\Delta(L_s)}{L_s} &= -\frac{R_{dc} \cdot G_{\text{unit}}}{\text{Re}(p_5)} \\ &= -\frac{R_{dc} \cdot G_{\text{unit}}}{R_{dc} \cdot G_{\text{unit}} - \omega^2 L_s \cdot C_{\text{unit}}} \\ &= -\frac{\tan \delta_{C_{\text{unit}}} \cdot \tan \delta_{R_{dc}}}{\tan \delta_{C_{\text{unit}}} \cdot \tan \delta_{R_{dc}} - 1}. \end{aligned} \quad (16)$$

The product $\tan \delta_{C_{\text{unit}}} \cdot \tan \delta_{R_{dc}}$ is a quantity, which decreases with frequency. Suppose that it is reasonable to assume that $\tan \delta_{C_{\text{unit}}} \cdot \tan \delta_{R_{dc}} \ll 1$ at high frequencies. In that case, $(\Delta(L_s)/L_s)$ is reduced to

$$\frac{\Delta(L_s)}{L_s} \approx \tan \delta_{C_{\text{unit}}} \cdot \tan \delta_{R_{dc}}. \quad (17)$$

Once estimates for the capacitance per unit length C_{unit} and the load inductance L_s have been obtained, the conductance per unit length G_{unit} can be obtained from $\text{Re}(p_5)$ as follows:

$$G_{\text{unit}} = \frac{\text{Re}(p_5) + \omega^2 L_s \cdot C_{\text{unit}}}{R_{\text{dc}}}. \quad (18)$$

The characteristic impedance Z_c can then be calculated using (6). By using (3), the parasitic capacitances C_s and C_g , together with their losses R_s and G_g , can be easily calculated. For convenience, the loss tangents of the parasitic capacitances are defined as

$$\tan \delta_{C_s} = \omega C_s \cdot R_s \quad (19a)$$

$$\tan \delta_{C_g} = \frac{G_g}{\omega C_g}. \quad (19b)$$

In the end, the termination impedances of the reflect standard can be obtained from MTRL-corrected measurement of the reflect standard and the line impedance Z_c .

IV. MULTIFREQUENCY OPTIMIZATION METHOD

For a given parameter estimation problem, besides methods based on explicit equations, optimization programs can be used to solve the underlying system of nonlinear equations. In case of complicated equations, using optimization programs is simpler compared with deriving analytical equations, because one just has to formulate the equations describing the relationships between the measurement quantities and the parameters to be determined, and run the optimization routine. Multifrequency optimizations are especially attractive for solving problems with both frequency-dependent and frequency-independent parameters, because single variables can be used to define frequency-independent parameters, and all the parameters can be optimized by a single-optimization run. However, the optimization problem becomes large scale if all the parameters are to be optimized at once. Even with increasing computation power of modern CPUs, large-scale optimization problems can still be time-consuming. A multifrequency approach is proposed in this paper for the determination of series-resistor calibration parameters. In the next paragraph, the techniques of this approach are discussed.

Like any single-frequency optimization problem, the multifrequency approach starts with describing the functional relationships between the measured S -parameters and the model parameters of the series-resistor and the series-capacitor standards, which are C_s , R_s , C_g , L_s , C_{unit} , and G_{unit} . Among the parameters, L_s is assumed to be frequency-independent and others are assumed frequency-dependent because of the dispersive substrate under consideration. The loss of the fringing capacitance G_g is set to zero, because it is a small quantity. When executing the least-square optimizer “lsqcurvefit” in MATLAB, a finite-difference method is used internally to derive the Jacobian, whose elements are the partial derivatives between the output quantities, which are the S -parameters, and the optimized quantities, which are the model parameters of the calibration standards. For N frequency points, the number of parameters to be optimized is $5N + 1$, and the number of measured quantities is $8N$,

i.e., real and imaginary parts of S_{11} and S_{21} of the series-resistor and capacitor standards, respectively. For a 512-point broadband sweep from 100 to 110 GHz, the Jacobian to be determined by the finite-difference method is 2561 by 4090. It has around 10 million elements, which requires heavy calculations. In order to reduce the computation time, the “lsqcurvefit” optimizer is supplied with analytically computed Jacobian. The Jacobian is computed taking advantage of two properties of the multifrequency optimization problem. The first property is that at each frequency, the functional relationships describing the measured S -parameters and the circuit parameters of the calibration standards are the same. This means that the analytical equation for calculating the Jacobian has to be derived only once. The single-frequency Jacobian is calculated analytically and straightforwardly using the symbolic tool box in MATLAB. Then, this single-frequency Jacobian is extended to the multifrequency case taking into account the second property of the multifrequency optimization problem, i.e., the sparsity of the Jacobian. The sparsity of the Jacobian comes from the fact that the measured S -parameters at frequency i do not depend on the frequency-dependent circuit parameters at frequency j , but only depend on the frequency-dependent parameters at its own frequency and one frequency-independent parameter, L_s . In this way, the number of elements in the Jacobian to be calculated reduces to 0.024 million from 10 million. The total computation time on a 3-GHz CPU (45-nm quad-core CPU with only one core used by the program) is around 2 h for the example presented in Section V.

V. EXPERIMENTAL VALIDATION

The proposed series-resistor calibration methods are validated by calibration structures on a high-resistivity silicon substrate. This section first introduces the calibration substrates used in this paper, and then presents the measurement results using the proposed methods and the benchmark method. It will be shown by calibration comparison that the series-resistor calibrations produced with the proposed methods and the benchmark method are close to each other.

A. Calibration Substrates and Measurement Setup

CPW series-resistor calibration standards were fabricated on a silicon substrate and a lossless quartz substrate. The used silicon substrate was a high-resistivity silicon substrate and has a resistivity larger than $18 \text{ k}\Omega \cdot \text{cm}$. Fig. 5 shows microphotographs of the series-resistor, the series-capacitor, and the short on the fabricated silicon substrate. A 9-nm-thick palladium-gold resistive filament of lateral dimensions $10 \mu\text{m}$ by $10 \mu\text{m}$ was fabricated as the series-resistor. CPW conductors were fabricated by gold evaporation. The measured gold thickness is around 500 nm. The geometries of the gold conductors in the series-capacitor standard shown in Fig. 5(b) were designed to be exactly the same as the series-resistor standard. The dimensions for the series-resistor standards are listed in Table I. The names of the dimensions, i.e., “ w ,” “ s ,” “ g ,” and “ l ” are defined in Fig. 5(a). The dc resistances of the series-resistor standards on the quartz and the silicon substrate are measured to be 56.55 and 61.53 Ω , respectively.

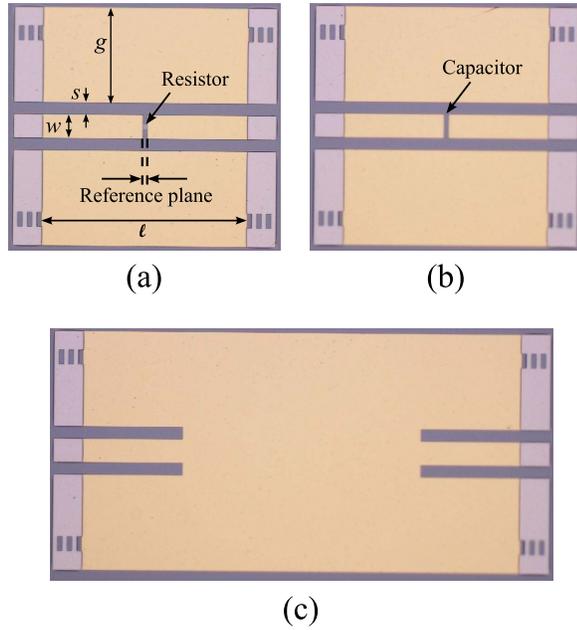


Fig. 5. Microphotographs of (a) series-resistor standard, (b) series-capacitor standard, and (c) short standard on the silicon substrate.

TABLE I
GEOMETRIES OF THE SERIES-RESISTOR STANDARDS
ON THE QUARTZ AND SILICON SUBSTRATES

	w (μm)	s (μm)	g (μm)	l (μm)	thickness (μm)
Quartz substrate	100	10	290	430	500
Silicon substrate	50	25	200	430	500

MTRL calibration standards were also fabricated on the same quartz and silicon substrate, respectively. The line lengths used for the quartz substrate are 0.42 (thru), 1, 2.155, 3.135, 4.2, 7.615, and 11.57 mm, defined between the two alignment markers furthest away from the probing positions [Fig. 5(a)]. The lengths for the silicon substrate are 0.42 (thru), 1, 1.735, 3.135, 4.595, 7.615, and 9.970 mm. Both sets have a short standard of 0.21 mm.

During the measurement, the two calibration substrates were placed on the top of 8 mm of sapphire spacers to avoid the unwanted parasitic microstrip mode between the CPW conductors and the metal chuck. The substrates were measured with 100- μm pitch ground-signal-ground wafer probes with 1.0-mm coaxial connectors, a manual probe station, and a broadband network analyzer. Log frequency sweeps from 100 MHz to 110 GHz with 512 points were performed to measure the raw S -parameters.

B. Measurement Results

Fig. 6 shows the model parameters of the series-resistor standards on the high-resistivity silicon substrate. The capacitance per unit length C_{unit} is plotted in Fig. 6(a). A clear dispersion is observed across the whole measured frequency range, which is due to the native oxide layer, which is a few nanometer thick on the top of the silicon substrate

with losses [8]. C_{unit} extracted with the proposed methods accurately replicate calibration comparison up to 80 GHz. Above 80 GHz, the proposed methods become slightly unstable. Fig. 6(b) shows the loss tangent of the capacitance per unit length $\tan \delta_{C_{\text{unit}}}$. Similar to C_{unit} , the proposed methods replicate calibration comparison method at low frequencies. However, all the methods become unstable at high frequencies with the benchmark calibration comparison method being the most stable method. The reason for the observed instability is under investigation. Characteristic impedance of the CPW lines Z_c is calculated with the help of the measured propagation constant γ from (6). It can be seen from Fig. 6(c) and (d) that the slightly unstable behaviors of C_{unit} and $\tan \delta_{C_{\text{unit}}}$ only have a small effect on the extracted characteristic impedance around 90 GHz.

The load inductance L_s is plotted in Fig. 6(e) for the different methods. L_s values measured with the closed-form equation method (hollow squares) deviate from the benchmark calibration comparison method. The deviation is large at low frequencies and becomes smaller as frequency increases, because the relative error in the load inductance estimation, which is equal to $\tan \delta_{C_{\text{unit}}} \cdot \tan \delta_{R_{\text{dc}}}$ (17), decreases with frequency. To reduce the measurement error on the load inductance, L_s values at high frequencies are averaged. Although more complex load inductance averaging approaches exist in the literature [9]–[11], in this paper, without detailed knowledge of the error of load inductance, a simple averaging approach is adopted. The starting frequency for the averaging is based on the calculated dc inductance, which is around 8.5 pH. The calculation is made using the CPW model in NIST Microwave Uncertainty Framework [6], [12]. At 50 GHz, the impedance of the load inductance is about 5% of the load resistance, so it is assumed that above this frequency, the load inductance can be measured with a relatively high accuracy. The CPW model predicts that the dc-110-GHz dispersion of the load inductance is around 7%, so using the dc inductance to calculate the starting frequency for the inductance averaging seems to be reasonable. The model also predicts that the 1–110-GHz inductance dispersion is around 0.3 pH, which gives only 0.2 Ω at 100 GHz, so, assuming that the gigahertz load inductance is constant over frequency also seems to be reasonable. As is clear from Fig. 6(e), measurement uncertainties of the load inductance is much larger than the intrinsic load inductance dispersion.

Once an estimate of the load inductance is obtained, the relative error in the second-order assumptions made to derive C_{unit} and L_s can be calculated for checking purposes. The relative error in estimating the capacitance per unit length C_{unit} and the load inductance L_s using the closed-form equations at 1, 20, 50, and 100 GHz is tabulated in Table II. It is clear from the table that the estimation error for C_{unit} is always low and the error for L_s drastically decreases to the order of 10% above 50 GHz. When calculating the estimation error using the proposed closed-form equations, C_{unit} and $\tan \delta_{C_{\text{unit}}}$ from the benchmark calibration comparison method are used. Since the extracted $\tan \delta_{C_{\text{unit}}}$ is not stable at high frequencies, its values between 0.1 and 64 GHz are fitted and extrapolated up to 110 GHz for making the

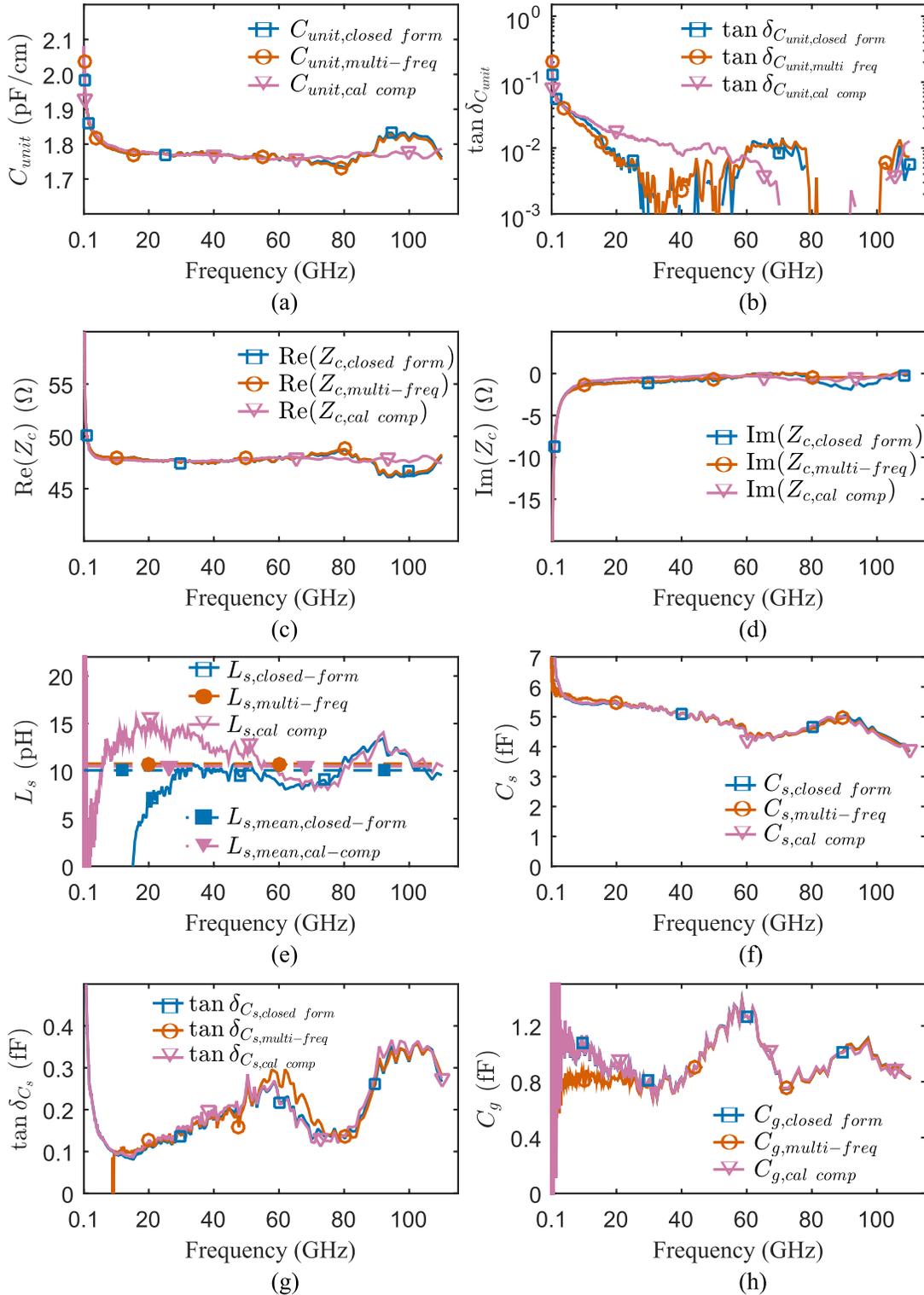


Fig. 6. Extracted model parameters on the high-resistivity silicon substrate using different methods. (a) Capacitance per unit length C_{unit} (pF/cm) of the CPW transmission lines and (b) loss tangent of the capacitance per unit length $\tan \delta_{C_{unit}}$. (c) Real $\text{Re}(Z_c)$ and (d) imaginary $\text{Im}(Z_c)$ parts of the characteristic impedance of the CPW lines. (e) Load inductance L_s of the series-resistor together with its mean-value between 50 and 110 GHz. (f) Series-capacitance C_s of the series-resistor and (g) its loss tangent $\tan \delta_{C_s}$. (h) Fringing capacitance C_g between the CPW center conductors and the ground planes on the series-resistor standard. Fig. 3 shows the locations of model parameters listed above on the series-resistor standard.

error calculations. In addition, the average load inductance value from the closed-form equations is used instead of inductance values extracted at each frequency.

The average load inductance values from the different methods are tabulated in Table III and are compared with the benchmark calibration comparison method. Both the

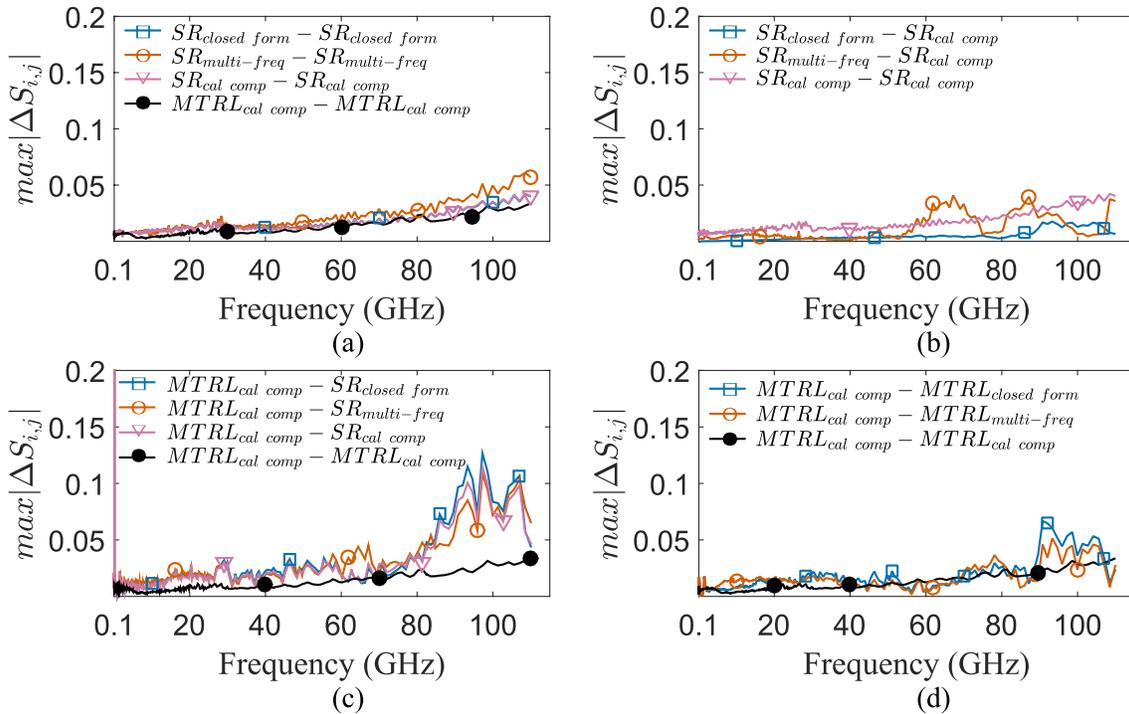


Fig. 7. Calibration comparisons on the high-resistivity silicon substrate. (a) Nonreproducibility of series-resistor calibrations and the MTRL calibration. $SR_{closed\ form}$ and $SR_{multi-freq}$ are the series-resistor calibrations using the proposed closed-form equation method and the multifrequency method, respectively. $SR_{cal\ comp}$ is the benchmark series-resistor calibration. Its model parameters are obtained from MTRL-corrected S -parameters of the series-resistor standards with the reference impedance of the S -parameters determined using the calibration comparison technique mentioned in the Appendix. $MTRL_{cal\ comp}$ is the MTRL calibration on the silicon substrate with its reference impedance determined using the calibration comparison technique. (b) Comparison between the proposed series-resistor calibrations with the benchmark series-resistor calibration. (c) Comparison between series-resistor calibrations and the MTRL calibration. (d) Comparison between MTRL calibrations. $MTRL_{closed\ form}$ and $MTRL_{multi-freq}$ are MTRL calibrations on the silicon substrate with the reference impedance determined through the proposed closed-form equation method and the proposed multifrequency method, respectively.

TABLE II

RELATIVE ERROR(%) IN ESTIMATING THE CAPACITANCE PER UNIT LENGTH C_{unit} USING (9) AND IN ESTIMATING THE LOAD INDUCTANCE L_s USING (15) AT DISCRETE FREQUENCIES

error	1 GHz	20 GHz	50 GHz	100 GHz
$\frac{\Delta(C_{unit})}{C_{si}}$ (13)	0.0074%	0.0347%	0.0554%	0.0795%
$\frac{\Delta(L_s)}{L_s}$ (17)	6873%	80.1%	21%	7.4%

TABLE III

AVERAGE VALUE OF LOAD INDUCTANCE FROM 50 TO 110 GHz ON THE HIGH-RESISTIVITY SILICON SUBSTRATE USING DIFFERENT METHODS

L_s	Closed form	Multi-freq	Cal comp
Average value	10.09 (pH)	10.79 (pH)	10.51 (pH)
Difference with cal comp	4.00%	2.76%	0

closed-form equation method and the multifrequency method give load inductance values close to the benchmark method. The extracted load inductances are higher than the calculated dc inductance by about 2 pH. The reason is that the dc inductance calculation was based on a CPW model that neglects the parasitic inductance due to the center conductor width

change on the series-resistor standard. Calculations of a similar CPW discontinuity in the literature show that one discontinuity gives about 1 pH of parasitic inductance [13], which explains the observed difference. Since the discontinuity inductance is one order of magnitude smaller than the CPW inductance, its dispersion is also one order of magnitude smaller than the CPW inductance dispersion, making the discontinuity inductance dispersion negligible.

Fig. 6(f)–(h) shows the parasitic capacitances from the different methods and their values are close to each other.

C. Calibration Comparison With the Benchmark Technique

The first-tier series-resistor calibrations obtained with the proposed methods are compared with the benchmark method using the calibration comparison technique [14]. The calibration comparison technique compares two sets of calibration coefficients and calculates the worst case difference in the calibrated S -parameters of an arbitrary passive device-under-test. The calculated difference indicates how close the two sets of calibrations are.

Two consecutive sets of measurements of the series-resistor standards and the MTRL standards are performed. The two sets of measurements are performed within 1.5 h, and the lab is under constant temperature control, so instrument drift is assumed to be negligible. Each set of measurement is processed by the proposed series-resistor calibration methods

and the benchmark method. The series-resistor calibrations in the second set recalculate the series-resistor model parameters, instead of using the parameters calculated in the first set. The results of calibration comparison between various calibrations are plotted in Fig. 7.

Fig. 7(a) shows the calibration nonreproducibility of different methods, which are the results of calibration comparison between two consecutive calibrations. MTRL calibration on the silicon substrate with the reference impedance measured by the calibration comparison technique (MTRL_{cal comp}) shows the lowest nonreproducibility. The proposed closed-form equation method (SR_{closed form}) gives almost the same nonreproducibility as the benchmark series-resistor calibration (SR_{cal comp}), which is slightly higher than the MTRL nonreproducibility. The model parameters of the benchmark series-resistor calibration are obtained from MTRL-corrected S -parameters of the series-resistor standards with the reference impedance of the S -parameters determined through the calibration comparison technique discussed in the Appendix. The proposed multifrequency method (SR_{multifreq}) is also highly reproducible, only slightly worse than the closed-form equation method. Fig. 7(b) shows the calibration comparison between the proposed series-resistor calibrations and the benchmark series-resistor calibration. The closed-form equation method produces a series-resistor calibration, which is almost the same as the benchmark series-resistor calibration. This is not surprising because as is shown in Fig. 6, the model parameters calculated using the closed-form equations are almost the same as the parameters calculated with the benchmark technique. The multifrequency method deviates slightly from the benchmark series-resistor calibration. The reason is most likely that in the multifrequency program, the loss of the fringing capacitance is set to zero as an approximation.

Fig. 7(c) shows the comparison between series-resistor calibrations and the MTRL calibration on the silicon substrate. Below 80 GHz, the difference between series-resistor calibrations and the MTRL calibration is comparable with the nonreproducibility of MTRL calibrations, in which case series-resistor calibrations can safely replace the MTRL calibration without sacrificing calibration accuracy. Above 80 GHz, the difference between the two algorithms starts to grow, indicating that the series-resistor calibrations deviate further away from the MTRL calibration. Even the benchmark series-resistor calibration deviates strongly from the MTRL calibration above 80 GHz. The maximum calibration comparison difference is around 0.11 at 97 GHz. The reason for the relatively large deviation above 80 GHz is under investigation.

In the end, also the case when the proposed methods are used for only measuring the characteristic impedance on the silicon substrate is considered. The reference impedance of the MTRL calibration on the silicon substrate is transformed to 50 Ω by using the characteristic impedance measured with the proposed methods. The resulting calibrations using the closed-form equation method and the multifrequency method are denoted as MTRL_{closed form} and MTRL_{multifreq}, respectively. The low errors indicate that the proposed methods can be used for measuring the characteristic impedance on substrates with losses.

VI. CONCLUSION

We have presented two new methods to perform series-resistor calibrations on substrates with losses. Through first-tier measurement results on a high-resistivity silicon substrate, we have shown that the series-resistor calibrations produced using the new methods are comparable with the one produced using the traditional calibration comparison technique. Compared with the traditional technique, our proposed methods only require MTRL and series-resistor calibration structures on the same substrate and thus eliminate the need for extra lossless substrates.

APPENDIX

IMPROVED CALIBRATION COMPARISON METHOD FOR THE BENCHMARK SERIES-RESISTOR CALIBRATION

In this appendix, an improved version of the calibration comparison technique [5] for characterizing substrates with losses is described. The series-resistor calibration with model parameters characterized through the calibration comparison technique is used as the benchmark series-resistor calibration in this paper. The calibration comparison technique has been the popular method for measuring the characteristic impedance on substrates with losses [15]–[19]. What it requires are a first-tier calibration with a known reference impedance and a second-tier calibration on the substrate with losses and an unknown reference impedance. The error box obtained from the second-tier calibration describes the difference between the two calibration substrates, so it is called the “trans-wafer” error box. However, the existing methods in the literature [16], [17] neglect the fact that S_{12} and S_{21} of the trans-wafer error box cannot be measured separately. In fact, only their products are available. Neglecting the above fact will lead to errors on the extracted characteristic impedance and calibrated S -parameters.

A. ABCD Representation of a General One Side-Impedance-Transformed Two-Port Network

$ABCD$ representation is preferred over other representations of linear networks, because it simplifies the extraction procedure without losing any accuracy. By assuming, the reference impedance of the trans-wafer error box equal to 50 Ω and transforming its wave-cascading matrix into the $ABCD$ form can greatly simplify the extraction procedure.

First, the $ABCD$ transformation from 50- Ω wave-cascading matrix [7] of a two-port network can be defined as follows [20]:

$$\begin{aligned} A &= \frac{r_{11} + r_{12} + r_{21} + r_{22}}{2} \\ B &= 50 \cdot \frac{-r_{11} + r_{12} - r_{21} + r_{22}}{2} \\ C &= \frac{1}{50} \cdot \frac{-r_{11} - r_{12} + r_{21} + r_{22}}{2} \\ D &= \frac{r_{11} - r_{12} - r_{21} + r_{22}}{2} \end{aligned} \quad (20)$$

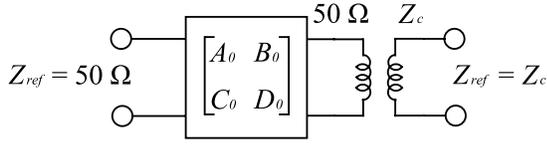


Fig. 8. Schematic representation of a two-port network with the reference impedance at the second port transformed to Z_c .

where r_{ij} ($i, j = 1, 2$) are elements of the wave-cascading matrix

$$R = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} \quad (21)$$

and A , B , C , and D are the elements of the $ABCD$ matrix.

Next, a general two-port network with the reference impedance at port 1 equal to 50Ω and the reference impedance at port 2 equal to some unknown Z_c is considered. The schematic of the network is shown in Fig. 8, where A_0 , B_0 , C_0 , and D_0 represent the $ABCD$ matrix elements of the two-port network without the impedance transformer. A_0 , B_0 , C_0 , and D_0 are transformed to the wave-cascading matrix form by using the inverse transform of (20), and the result is called R_0 . The wave-cascading matrix of the complete network shown in Fig. 8 can be derived by multiplying the wave-cascading matrix of the wave impedance transformer [7] with R_0 . In the end, $ABCD$ representation of the whole network in Fig. 8 can be obtained by transforming its wave-cascading matrix using (20) and the result is shown as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \sqrt{1 - j \frac{\text{Im}(Z_c)}{\text{Re}(Z_c)}} \cdot \begin{bmatrix} \sqrt{\frac{Z_c}{50}} \cdot A_0 & \sqrt{\frac{50}{Z_c}} \cdot B_0 \\ \sqrt{\frac{Z_c}{50}} \cdot C_0 & \sqrt{\frac{50}{Z_c}} \cdot D_0 \end{bmatrix}. \quad (22)$$

B. Calibration Comparison

Fig. 9 shows the schematic of the trans-wafer error box mentioned above between the high-resistivity silicon substrate and the lossless quartz substrate. In this paper, the interaction between the wafer probes and the CPW conductors are modeled by a resistor and an inductor in series. The resistor accounts for the contact resistance and the inductor accounts for the current path from the wafer probes to the CPW lines. The effect of the short stub behind the probes when the probes are landed is modeled by a shunt capacitor and a shunt conductance, which accounts for substrate losses. In Fig. 9, “ d ” in the names of the lumped elements indicates that the lumped elements represent the difference in the probing parasitics. Z_c in the figure denotes the characteristic impedance of the transmission lines on the silicon substrate.

To obtain measurements of the error box shown in Fig. 9, first, a $50\text{-}\Omega$ calibration is performed on the lossless substrate with the reference plane shifted to the probe tips. In the experiment, MTRL calibration on the quartz substrate is used. The reference impedance of the MTRL calibration on the quartz substrate is obtained by measuring the capacitance per

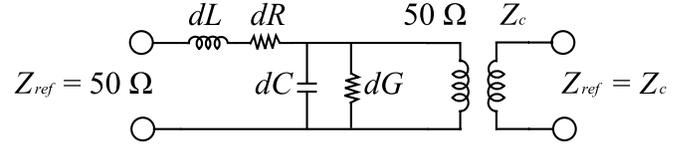


Fig. 9. Schematic of the trans-wafer error box.

unit length with a series-resistor at low frequencies [3], [21]. A second-tier MTRL calibration on the silicon substrate is performed using first-tier-corrected data. The reference plane of the second-tier MTRL calibration is also shifted back to the probe tips. The calibration error box from the second-tier MTRL calibration contains the trans-wafer information. Its S -parameters are written as follows:

$$S_{\text{trans-wafer}} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}. \quad (23)$$

C. Determination of Model Parameters of the Trans-Wafer Error Box

First, the $ABCD$ matrix of the $50\text{-}\Omega$ network, which only consists of dL , dR , dC , and dG in Fig. 9, is derived as follows:

$$\begin{bmatrix} A_0 & B_0 \\ C_0 & D_0 \end{bmatrix} = \begin{bmatrix} 1 + y \cdot z & z \\ y & 1 \end{bmatrix} \quad (24)$$

where

$$\begin{aligned} y &= j\omega \cdot dC + dG \\ z &= j\omega \cdot dL + dR. \end{aligned} \quad (25)$$

In practical situations, the product $y \cdot z$ is much smaller than 1, as a result, the above $ABCD$ matrix is simplified as follows:

$$\begin{bmatrix} A_0 & B_0 \\ C_0 & D_0 \end{bmatrix} \approx \begin{bmatrix} 1 & z \\ y & 1 \end{bmatrix}. \quad (26)$$

Note that under the assumption $y \cdot z \ll 1$, if the positions of the series network $dL - dR$ and the shunt network $dC // dG$ are interchanged, the resulting $ABCD$ matrix is unchanged, which is shown below

$$\begin{bmatrix} A'_0 & B'_0 \\ C'_0 & D'_0 \end{bmatrix} = \begin{bmatrix} 1 & z \\ y & 1 + y \cdot z \end{bmatrix} \approx \begin{bmatrix} 1 & z \\ y & 1 \end{bmatrix} \quad (27)$$

where A'_0 , B'_0 , C'_0 , and D'_0 are $ABCD$ matrix elements of the interchanged two-port network. Having obtained A_0 , B_0 , C_0 , and D_0 , the $ABCD$ representation of the trans-wafer error box can be written down as follows using (22):

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} \approx \sqrt{1 - j \frac{\text{Im}(Z_c)}{\text{Re}(Z_c)}} \cdot \begin{bmatrix} \sqrt{\frac{Z_c}{50}} & \sqrt{\frac{50}{Z_c}} \cdot z \\ \sqrt{\frac{Z_c}{50}} \cdot y & \sqrt{\frac{50}{Z_c}} \end{bmatrix}. \quad (28)$$

Since calibration comparison only measures the product $S_{12} \cdot S_{21}$ of the trans-wafer error box shown in Fig. 9, only ratios of the $ABCD$ matrix elements in (28) are available. But still, the model elements of the trans-wafer error box

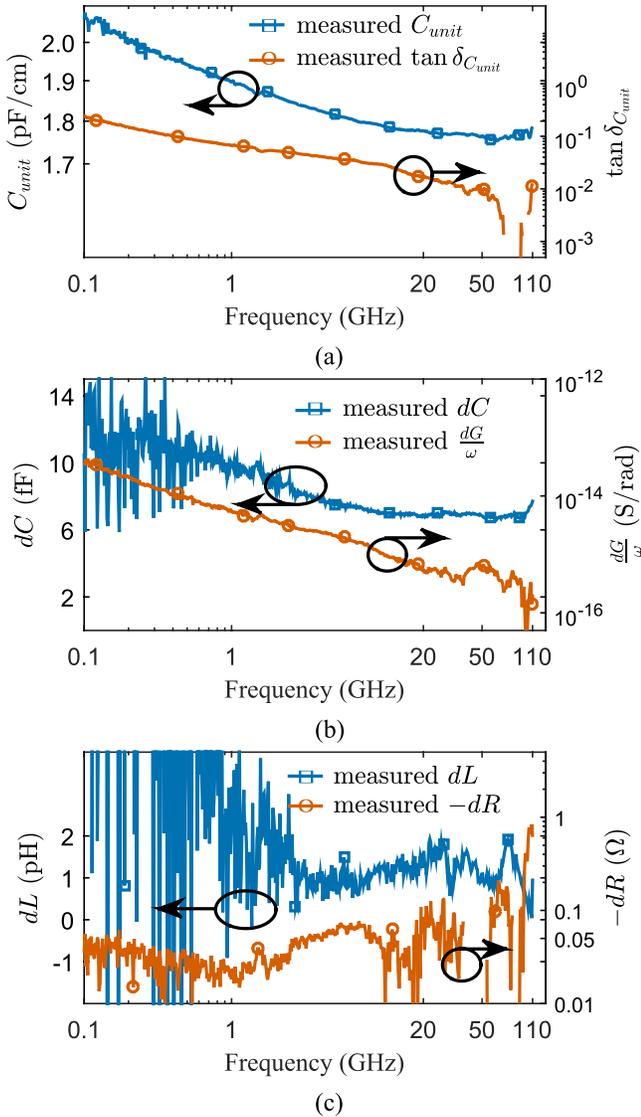


Fig. 10. Measured (a) capacitance per unit length C_{unit} and its loss tangent $\tan \delta_{C_{unit}}$ of the CPW lines on the high-resistivity silicon substrate, (b) trans-wafer capacitance dC and conductance divided by frequency $(dG)/\omega$, and (c) trans-wafer inductance dL and resistance dR .

can be extracted due to the redundancy in the $ABCD$ matrix. The extraction is as follows:

$$Z_c = \frac{A}{D} \cdot 50$$

$$= 50 \cdot \frac{(1 + S_{11}) \cdot (1 - S_{22}) + S_{12} \cdot S_{21}}{(1 - S_{11}) \cdot (1 + S_{22}) + S_{12} \cdot S_{21}} \quad (29)$$

$$y = \frac{C}{A} = \frac{1}{50} \cdot \frac{(1 - S_{11}) \cdot (1 - S_{22}) - S_{12} \cdot S_{21}}{(1 + S_{11}) \cdot (1 - S_{22}) + S_{12} \cdot S_{21}} \quad (30a)$$

$$z = \frac{B}{D} = 50 \cdot \frac{(1 + S_{11}) \cdot (1 + S_{22}) - S_{12} \cdot S_{21}}{(1 - S_{11}) \cdot (1 + S_{22}) + S_{12} \cdot S_{21}} \quad (30b)$$

which allows the lumped elements to be further extracted using

$$dR = \text{Re}(z) \quad (31a)$$

$$dL = \frac{\text{Im}(z)}{\omega} \quad (31b)$$

$$dG = \text{Re}(y) \quad (31c)$$

$$dC = \frac{\text{Im}(y)}{\omega} \quad (31d)$$

The capacitance per unit length C_{unit} and the conductance per unit length G_{unit} of the CPW lines on the silicon substrate can be calculated using

$$j\omega \cdot C_{unit} + G_{unit} = \frac{\gamma}{Z_c} \quad (32)$$

where γ is the propagation constant measured with the MTRL calibration on the silicon substrate.

Fig. 10 shows the calibration comparison extraction results for the silicon substrate described in Section V. The extracted capacitance per unit length C_{unit} in Fig. 10(a) shows a clear dispersion due to the native oxide layer on the top of the silicon substrate with losses [8]. The extracted trans-wafer capacitance dC is around 7 fF and is quite stable at high frequencies. The trans-wafer inductance dL is in the order of 1 pH and is very sensitive to measurement errors at high frequencies. A separate study shows that the inductance introduced by probe-position uncertainties is already 0.3 pH/ μm on the quartz substrate. Given the above fact, it is difficult to measure inductances on-wafer in the order of 1 pH with manual probe positioners. Measured difference in contact resistance dR is around -0.04Ω , which might be due to the fact that the quartz substrate has been used while the silicon substrate is a new one. The product $y \cdot z$ is calculated to verify the assumption made in the extraction. Its maximum value is 0.005 at 110 GHz, which proves that the assumption $y \cdot z \ll 1$ is valid.

After the characteristic impedance on the high-resistivity silicon substrate has been measured, series-resistor model parameters can be calculated from (3), based on which the benchmark series-resistor calibration is performed.

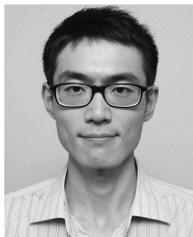
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