A ROUND ROBIN EXPERIMENT TO SUPPORT BOND VOID MEASUREMENT STANDARDS

Richard A. Allen[1], David T. Read[1], Victor H. Vartanian[2], Winthrop A. Baylies[3], William Kerr[4], Mark Plemmons[4], Noel Poduje[4], and Kevin Turner[5]

[1]National Institute of Standards and Technology, [2]SEMATECH, [3]Baytech-Resor, [4]Evergreen Enhancement, and [5]University of Pennsylvania

Abstract

A round robin experiment to compare the sensitivities of various metrology tools to small voids between bonded wafers such as are used in three-dimensional stacked integrated circuits (3DS-ICs) and MEMS packaging. Participants received a set of four bonded wafer pairs with programmed voids from 0.5 µm to 300 µm in the bond plane; each wafer pair had different void depth ranging from 40 nm to 1200 nm. This experiment highlighted the capabilities and limits of various infrared (IR) and acoustic microscopies, including factors such as speed of measurement and resolution.

Introduction

To support the growing application of wafer bonding to three-dimensional stacked integrated circuits (3DS-ICs) and MEMS devices, the SEMI 3DS-IC Committee initiated a round robin experiment to compare the sensitivities of various metrology tools to small voids between wafers. Bond voids have been a long-standing concern in MEMS packaging, which rely on bonding to provide a hermetic seal isolating mechanical devices from the environment, and are a major roadblock to the implementation of direct wafer bonding for 3DS-ICs.

Random inhomogeneities, such as particles, trapped gasses, or non-uniformities in the surface layer, are typical sources of bond voids. The diameter and depth of any particular void is highly dependent on small variations in the inhomogeneity. Thus, this experiment used test wafers with programmed voids.

Also, the original goal of this experiment was a standard **Test Method** for measuring voids [1]. As the project advanced it became clear that the individual capabilities of the variety of metrology tools available were complementary and it made sense to develop the initial standard as a **Guide** document [2].

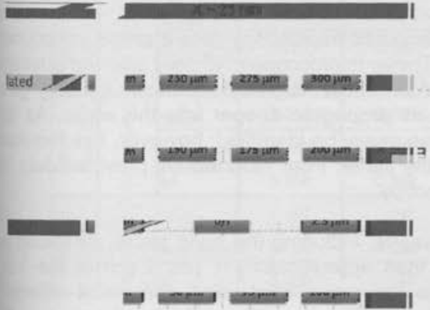

Figure 1. Layout of a single test chip

Test Wafer Design and Fabrication

A 25 mm by 32 mm test chip, incorporating a set of 18 test structures, was developed for this experiment (Figure 1). The individual test structures consist of an array of patterned voids, arranged so that there are isolated (>> 5:1 space to width), semi-dense (5:1), and dense (1:1) voids. The design dimensions of these voids range from 0.5 µm to 300 µm.

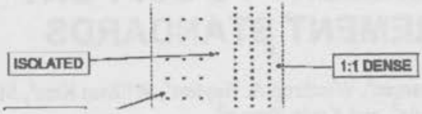

Figure 2. Isolated, semi-dense, and dense programmed voids within a block in the test chip

A thermal oxide, nominally 5 nm thick was grown on approximately 25 sets of four pairs of 300 mm silicon wafers. Photoresist was deposited onto one wafer from each pairs and the test chip was imaged on 51 sites on each wafer. The pattern was transferred into the oxide and the photoresist was then removed. One pair of wafers (one patterned, one unpatterned) was set aside. The pattern on the remaining three patterned wafers was then etched into the underlying silicon, using the oxide as a hard mask. The additional etch on the three wafers was 400 nm, 900 nm, and 1200 nm, respectively. After etching, each patterned wafer was bonded to an unpatterned cap wafer using an oxide bond process. A cross-section of the process is shown in Figure 3

Round Robin Experiment

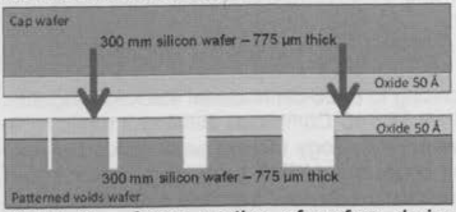

Figure 3. Cross section of wafers during bond process

A number of laboratories involved in MEMS and 3DS-IC packaging research and production volunteered to participate in the experiment. These laboratories included device manufacturers, metrology tool suppliers, and academic. The experiment was described to the laboratories and they were asked to measure these devices using any tool at their disposal. The tools in the experiment broadly fell into three categories: those using ultrasonic inspection to identify and/or characterize voids, those that use infrared light, and those that use x-rays. Reports were returned from ten laboratories, with two reporting null results and the other eight providing data from one or more of the wafers [3].

Ultrasonic techniques in this experiment included full-wafer resonance at frequencies around 40 kHz. This technique involves inducing vibrations in the bonded wafer pair and monitoring the response signal. Differences in the frequency response between a void-free bonded pair and the bonded pair under inspection were used to identify the presence of void. This technique provides a fast, qualitative indication of bond voids. One of the laboratories utilized this technology. Scanning acoustic microscopy uses a single transducer as source and to measure the return signal. These microscopes typically use transducers with resonant frequencies between 5 MHz and 500 MHz. Higher frequencies typically give better spatial resolution while lower frequencies propagate deeper into the wafer. As air gaps reflect 100 % of the signal, bond voids can easily be identified; however, this requires a coupling fluid between the transducer and the wafer. Four laboratories provided data to the experiment using scanning acoustic microscopy.

Infrared light is used to image the interior of wafers, including the bond plane, as silicon is transparent to light with wavelengths longer than approximately 1 µm. Each of the four laboratories contributing IR measurements to the experiment used somewhat different technologies including infrared interferometry, whole wafer IR, and IR microscopy. IR microscopy perhaps gives the most detailed images of voids [4]; however, the time to

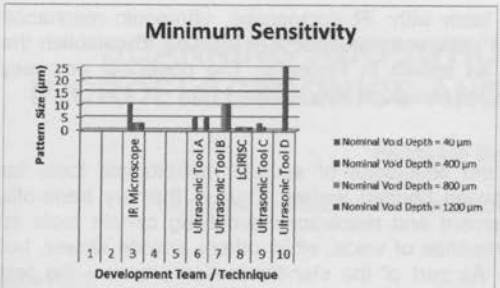

Figure 4. Minimum sensitivities for three measurement methods.

capture images using IR microscopy make it best used for characterizing voids identified using other techniques. The final IR tool was the grey-field polariscope. This technique captures the polarization of IR light transmitted through a bond wafer pair, which in turn is a function of stress in the wafer. This tool showed a limitation of the artificial voids used in this experiment: while voids *in situ are* caused by processes that invariably introduce stress around the void, this metrology was not sensitive to the artificial voids, which do not induce stress in the wafers.

The metrology tool used by the final laboratory was X-ray tomography. This technique has been shown to be useful for imaging various buried features in 3D stacked integrated circuits [5], [6]; however, since these samples, composed only of silicon and SiO_2, were transparent to x-rays, yielding no usable data.

Experimental Results: Defect Detection

Three systems will be considered for defect detection and location correlation: ultrasonic resonance spectroscope, infrared microscope, and Low Coherence InfraRed Interferometry SCanning (LCIRISC) system. The measurement techniques employed yield different results based on film thickness and measurement technique. Figure 4 shows the minimum sensitivities range from 1 µm to 25 µm for all of the teams that reported results. The LCIRISC system shows a consistent 1 µm minimum sensitivity for all void depths. Ultrasonic Tool C also shows a 1 µm minimum sensitivity for 400 µm void depth. The other systems had greater than 1 µm minimum sensitivity on all void depths.

Experimental Results: Location Correlation

Three sets of sister wafers were established for the purpose of location correlation. One set

Tools	Sister Wafer Sets	Metric	X-Location Correlation	Y-Location Correlation
Tool A - Tool B	Set 1 - Set 2	Slope	1.020	0.997
		Intercept	-0.160	-0.080
		R^2	0.998	0.999
Tool A - Tool C	Set 1 - Set 3	Slope	1.016	0.989
		Intercept	-0.102	-3.350
		R^2	0.998	0.945
Tool B - Tool C	Set 2 - Set 3	Slope	0.997	0.991
		Intercept	0.057	-3.266
		R^2	1.000	0.945

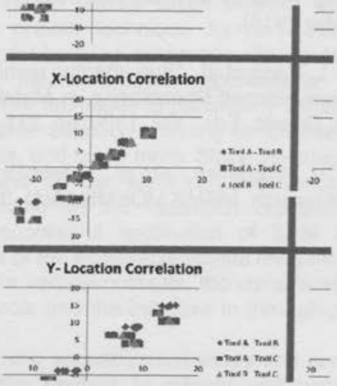

Figure 5. X-Y correlation results, where Tool A = LCIRISC, Tool B = IR microscope, Tool C = Acoustic microscope. All units in micrometers.

of sister wafers was provided to each team with: IR microscope, ultrasonic resonance spectroscope, and LCIRICS. These tools were correlated for X-Y location to establish the positional consistency across platforms as shown in Figure 5. The positional accuracy across systems correlates well with $R^2 > 0.99$ and slope approaching 1.0.

Conclusions and Future Work

These results highlight the strengths and limitations of several metrological tools for identifying and characterizing voids between bonded wafers. One of the key trade-offs observed is between speed of measurement and resolution, identifying certain tools as being better for quickly identifying the presence of voids, while others provide slower, but more detailed characterization of voids. As part of the standardization process, the test structure is being developed into a separate standard for use in characterizing void metrology tools. Several laboratories were unable to complete their measurements in time for inclusion in the first version of SEMI 3D13; as data from these laboratories becomes available it will be incorporated into the document. Finally, as these different metrologies and processes become more mature, it is likely that one or more will be adopted into stand-alone **Test Method** documents.

Acknowledgements

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