

3-D Thermal Component Model for Electrothermal Analysis of Multichip Power Modules With Experimental Validation

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Abstract—This paper presents for the first time a full three-dimensional (3-D), multilayer, and multichip thermal component model, based on finite differences, with asymmetrical power distributions for dynamic electrothermal simulation. Finite difference methods (FDMs) are used to solve the heat conduction equation in three dimensions. The thermal component model is parameterized in terms of structural and material properties so it can be readily used to develop a library of component models for any available power module. The FDM model is validated with a full analytical Fourier series-based model in two dimensions. Finally, the FDM thermal model is compared against measured data acquired from a newly developed high-speed transient coupling measurement technique. By using the device threshold voltage as a time-dependent temperature-sensitive parameter (TSP), the thermal transient of a single device, along with the thermal coupling effect among nearby devices sharing common direct bond copper (DBC) substrates, can be studied under a variety of pulsed power conditions.

Index Terms—Compact thermal model, component thermal model, electrothermal, multichip modules, soft switching inverter.

I. INTRODUCTION

IN order to further increase power densities within multichip power modules containing single-phase and three-phase inverter bridges, soft switching techniques are required along with dense packaging. Soft switching techniques such as the technique described in [1] allow for the reduction or elimination in switching loss by turning a device on under zero voltage switching (ZVS). Modules like the one in [1] contain multiple insulated gate bipolar transistor (IGBT), MOSFET, and diode chips mounted on a common direct bond copper (DBC) and baseplate layers. As a result of the close proximity of the IGBT, MOSFET, and diode chips, lateral heat spread due to thermal

coupling between chips must be considered within the electrothermal models.

Modeling the heat diffusion equation for thermal model development is extensive in research and publications. The most widely published electrothermal models in past literature assume single-chip configurations where assumed one-dimensional (1-D) heat conduction is all that is required to predict junction temperatures. The authors in [2]–[4] use Cauer networks, which contain R and C values with true physical meaning contrary to the widely used Foster cells. The R and C values are determined from thermal transient measurements generated from a heat source caused by a down-step variation of heating power.

Each of the methods described in [2]–[4] results in compact models parameterized in terms of structural and material properties. But these models are only valid for a 1-D thermal profile where only a single chip is considered and an additional model synthesis step is required from measurement or three-dimensional (3-D) FEM analysis. In order to model lateral heat spread due to thermal coupling within multichip modules, a method that includes multidimensional (>1 -D) heat conduction has to be considered.

Fourier series-based thermal models proposed in [5]–[9] are parameterized in terms of structural and material properties and use feedback loops to force the appropriate boundary conditions between multiple layer interfaces involving different materials. Material interfaces with different cross-sectional area are accounted for by increasing or decreasing the number of Fourier terms appropriately [9]. Each of these proposed methods are not full analytical solutions to the heat conduction equation and still rely on some numerical solution to determine the Fourier coefficients. Therefore, an ordinary differential equation (ODE) solver is still required from a simulator such as MATLAB Simulink. The increased simulation speed that typically results from a Fourier-based solution is further decreased by requiring an additional feedback loop to ensure the proper boundary conditions between material interfaces. The accuracy of the solution is therefore determined by the size of the feedback gain, which results in longer simulation time as the gain is increased. While Fourier-based methods are advertised to be much quicker than finite difference methods (FDMs), the computation savings may not be as obvious once a full 3-D multichip chip configuration is considered requiring large feedback gains and a large number of Fourier terms solved numerically for accurate solutions. In addition, the Fourier-based solutions do not consider the imperfect contact that may exist between materials that can result in

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significant temperature differences. Also, it is not easy to include temperature-dependent properties such as the nonlinear thermal conductivity of silicon.

The most widely used method for thermal modeling of multichip power modules involve curve fitting Foster RC cell networks from data sheet provided thermal transient curves or 3-D FEM solvers like Kojima *et al.* [10]–[16]. Kojima *et al.* [10], [11] present an RC compact thermal model of a high-voltage inverter module containing multiple chips based on Foster network cells. The Foster network cells are determined from a thermal impedance matrix extracted from a 3-D FEM solver. The impedance matrix describes the self-heating of each chip within the module and the heating of a single chip due to the heating of neighboring chips. Therefore, a full 3-D model that faithfully represents the lateral thermal interaction among neighboring chips is achieved. This method faithfully describes a 3-D module and the strong thermal coupling between chips but requires a full 3-D FEM and model extraction for any new module configuration resulting in an extra model synthesis step.

Walkey *et al.* [17], [18] present a multichip compact thermal model using voltage controlled voltage sources to represent chip to chip thermal coupling. The generation of the model still involves extraction of parameters from either an analytical or numerical solution to the heat equation to generate a per device thermal model.

In [19] the addition of current sources representing chip to chip coupling are inserted at various locations into a foster network. The locations of these current sources are determined from 3D FEM.

The method presented in [20] results in a compact thermal model where 3-D heat flow is accounted for by using appropriate symmetry in the discretization of the heat equation. The thermal package model, for example, describes the two-dimensional (2-D) later heat spreading by considering an effective heat flow area approach. This method was extended to thermal component models for multichip considerations in [21] where neighboring chips sharing a common DBC were assumed to have the same power dissipation. However, in conditions where there are multiple chips with varying power dissipation sharing a common DBC, the effective heat flow area is not well known ahead of time. And in these cases, 1-D heat flow cannot necessarily be assumed.

In [27] an analytical based solution to the heat equation based on a greens function representation of the temperature field of a three dimensional system was presented. However the solution requires matrices to be determined through a least squares fit to a thermal transient heating curve.

FDMs offer the most flexibility in representing thermal component models parameterized in terms of structural and material properties that faithfully can represent chip to chip thermal coupling. The results are compact thermal models that can be used as building blocks for any multichip module configuration without requiring additional modeling synthesis steps involving thermal transients or 3-D FEM models. It is often referenced in literature that FDM methods require too much computing time and cannot coexist with an electrical simulation making dynamic electrothermal models impossible. A recent method

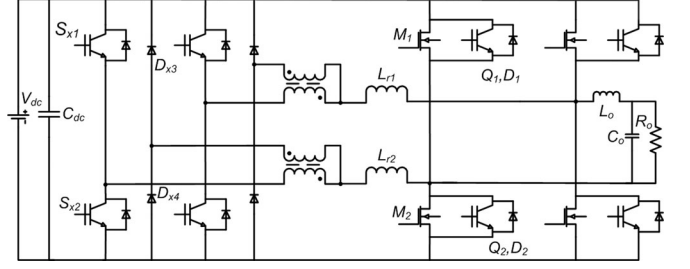


Fig. 1. Circuit diagram of a full-bridge-coupled magnetic type ZVS inverter module.

where increased computation time of an FDM-based model was desired was proposed in [29]. A set of N first-order finite difference equations describing the heat equation was converted to a set of M equations, where $M \ll N$. This is done by applying a generalized minimized residual (GMRES) algorithm where the reduced number of equations can be represented by equivalent M Foster cells. The application of the GMRES algorithm is another synthesis step, however, and may not be easily included in a compact thermal model.

This paper presents a 3-D FDM similar to the techniques used in [23] and [24] as a solution to the heat conduction equation for a multichip module. However, a full 3-D multilayered package describing the DBC layers is considered beneath the silicon chips. In addition, the imperfect thermal contact between materials is also included and thermal-dependent parameters such as the nonlinear thermal conductivity of silicon are considered.

Finally, the FDM model is also validated against measured data resulting from a newly developed high-speed double chip temperature-sensitive parameter (TSP) transient measurement developed in [22]. By using the device threshold voltage as a time-dependent TSP, the thermal transient of a single device, along with the thermal coupling effect among nearby devices sharing common (DBC) substrates, can be studied under a variety of pulsed power conditions. This technique allows hardware model validation under short-term high-power dissipation levels to be captured along with the thermal time constants resulting from the chip to chip coupling over longer term power dissipations without the use of thermal couples.

II. THERMAL MODEL DEVELOPMENT

A. Application

The device considered in this paper is a half-bridge power module made up of MOSFETs and IGBTs operated in parallel along with auxiliary devices made up of IGBTs for enabling the ZVS condition. The application, shown in Fig. 1, is a single-phase, full-bridge coupled magnetic ZVS inverter [1]. The magnetic elements L_{r1} and L_{r2} in Fig. 1 store energy enabled by the auxiliary devices, allowing discharge of the main device parasitic capacitance aligning the device with zero volts prior to turn on. The turn-on switch loss is eliminated with this technique, thereby drastically decreasing the overall switch loss resulting in increased module efficiency and minimizing EMI within the system.

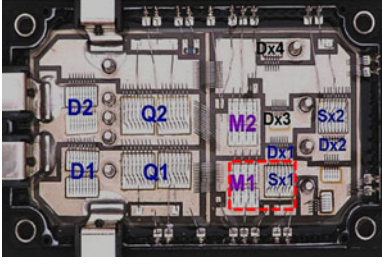


Fig. 2. Module components of soft switching module.

TABLE I
CONSTANTS OF THERMAL PROPERTIES

Material	Thermal conductivity (W/(cm·K))	Density (g/cm ³)	Specific heat (J/(g·K))
Silicon	1.56	2.328	0.712
ALN	2.17	3.24	1.05
Copper	4.01	8.98	0.385
Solder	0.57	8.17	0.159

The circuit in Fig. 1 is made up of two independent half-bridge modules. Referring to Fig. 1, each module contains the main switching elements of the inverter circuit made up of IGBTs Q_1 and Q_2 operated in parallel with MOSFETs M_1 and M_2 respectively. Free-wheeling diodes for the main switching elements are also included and designated D_1 and D_2 in Fig. 1. In addition, to the main switching elements, auxiliary IGBTs S_{x1} and S_{x2} are also included in each module.

B. Packaging

Each module utilizes DBC technology where copper is directly bonded to a ceramic substrate such as ALN. The thermal analysis in this paper focuses on two chips exhibiting strong thermal coupling due to their proximity to each other and different power distributions. The different power distributions are a result of the different circuit function each chip performs in the inverter circuit. The power distribution of M_1 and Q_1 exhibit the traditional inverter switch loss minus the turn-on loss due to ZVS condition. The power distribution of S_{x1} is much different and has a very large peak power for a short duration to charge the resonant element used for enabling ZVS of the main switch. The chips that are the focus of this paper are the auxiliary IGBT S_{x1} and main switching MOSFET M_1 in Fig. 1. Both chips share a common DBC and are relatively close together shown in Fig. 2 outlined in the dotted dashed line.

It is desired to have a compact thermal model parameterized in terms of structural and material properties. Table I shows the material information for each layer of the DBC.

The DBC materials and associated material thicknesses and dimensions for the two chips S_{x1} and M_1 are shown in Fig. 3. The individual power distribution for each chip is assumed evenly distributed at the top of each chip, but the two chips do not have the same power distribution.

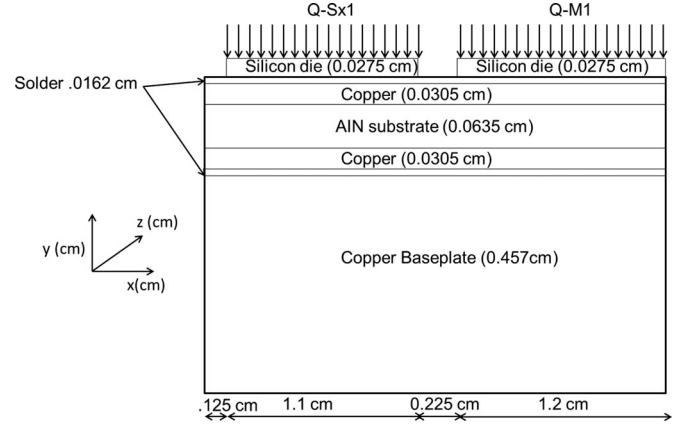


Fig. 3. DBC stack up of soft switching module.

C. Heat Equation

Referring to Fig. 3, the heat is assumed to be generated on top of the silicon chip and conducted through the different layers. This is a multilayer, multidimensional heat conduction problem. The resulting 3-D transient heat diffusion equation, assuming no internal heat generation, at a particular layer i in Cartesian coordinates is shown as follows:

$$\frac{\partial}{\partial x} \left(k_i \frac{\partial T_i(x, y, z, t)}{\partial x} \right) + \frac{\partial}{\partial y} \left(k_i \frac{\partial T_i(x, y, z, t)}{\partial y} \right) + \frac{\partial}{\partial z} \left(k_i \frac{\partial T_i(x, y, z, t)}{\partial z} \right) = \rho_i c_i \frac{\partial T_i(x, y, z, t)}{\partial t},$$

$$i = 1, \dots, m. \quad (1)$$

In (1), ρ_i is the thermal density, c_i the specific heat of the material, respectively, and m represents the number of layers. It is often possible to simplify (1) if the thermal conductivity k_i of the material is constant. However, in silicon, the thermal conductivity is nonlinear and is modeled by [20]

$$k_i(T_i(x, y, z, t)) = 1.5486 \left(\frac{300}{T_i(x, y, z, t)} \right)^{4/3}. \quad (2)$$

To solve (1) for the module considered in this paper, certain boundary conditions are required. A constant surface temperature is maintained at bottom of the module resulting in a Dirichlet boundary condition as shown

$$T_m(x, y, z, t)|_{y=y_{m+1}} = T_A. \quad (3)$$

The top layer of the module corresponds to the heat flux (Watt per square centimeter) generated from the power distribution of each chip where all the heat is assumed to flow into the top boundary of the silicon chip resulting in a Neuman condition shown as follows:

$$-k_1 \frac{\partial T_1(x, y, z, t)}{\partial y} \bigg|_{y=y_1=0} = q''(t). \quad (4)$$

The sides of the module and in the areas with no heat flux generated on the top of the module, adiabatic boundary conditions exist and result in a special case of the Neuman condition

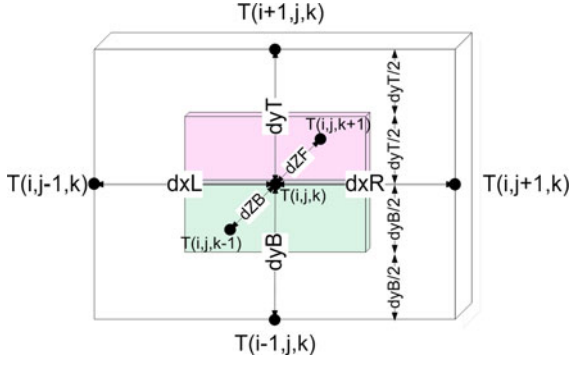


Fig. 4. Interior control volume at a material interface.

shown as follows:

$$\left. \frac{\partial T_1(x, y, z, t)}{\partial y} \right|_{y=y_1=0} = 0. \quad (5)$$

Finally, if perfect thermal contacts exists between layers of different materials

$$T_i(x, y_{i+1}, z, t) = T_{i+1}(x, y_{i+1}, z, t) \quad (6)$$

and

$$k_i \left. \frac{\partial T_i(x, y, z, t)}{\partial y} \right|_{y=y_{i+1}} = k_{i+1} \left. \frac{\partial T_{i+1}(x, y, z, t)}{\partial y} \right|_{y=y_{i+1}}. \quad (7)$$

D. 3-D FDM Thermal Model

The finite difference form of the heat equation in (1) is used to solve the corresponding 3-D temperature distributions within the multichip module shown in Fig. 2. The finite difference equations are derived using the energy balance method described in [26]. This approach enables one to analyze many different phenomena such as problems involving multiple layers and exposed surfaces that do not align with an axis of the coordinate system [26]. The finite difference equation for a node is obtained by applying conservation of energy using simplified forms of Fourier's law to a control volume about the nodal region. Therefore, the entire volume of the package is discretized into a finite number of nodes. The number of nodes in the y -direction is $size_y$, the number of nodes in the x -direction is $size_x$ and the number of nodes in the z -direction is $size_z$. A variable grid size is used for determining the number of nodes and results in an optimized computation time.

A finite difference equation using the conservation of energy is written to a control volume about an interior node $T(i,j,k)$ in (8) where $i = 1:size_y$, $j = 1:size_x$ and $k = 1:size_z$. The implicit form of a finite difference equation is used to approximate the time derivative, while evaluating all other temperatures at the new $(p+1)$ time, instead of the previous (p) time. Relative to the explicit method, the implicit formulation has the advantage of being unconditionally stable [26]. The corresponding control

volume and associated dimensions are shown in Fig. 4

$$\begin{aligned} & k_{avg} A_{yz} \frac{(T_{i,j+1,k}^{p+1} - T_{i,j,k}^{p+1})}{d_{xR}} + k_{i-1} A_{xz} \frac{(T_{i-1,j,k}^{p+1} - T_{i,j,k}^{p+1})}{d_{yB}} \\ & + k_{avg} A_{yz} \frac{(T_{i,j-1,k}^{p+1} - T_{i,j,k}^{p+1})}{d_{xL}} \\ & + k_{i+1} A_{xz} h_{ci} \frac{(T_{i+1,j,k}^{p+1} - T_{i,j,k}^{p+1})}{h_{ci} d_{yT} + k_{i+1}} b_c \\ & + k_{avg} A_{xy} \frac{(T_{i,j,k+1}^{p+1} - T_{i,j,k}^{p+1})}{d_{zF}} \\ & + k_{avg} A_{xy} \frac{(T_{i,j,k-1}^{p+1} - T_{i,j,k}^{p+1})}{d_{zB}} \\ & = E_{xyz} \frac{T_{i,j,k}^{p+1} - T_{i,j,k}^p}{\Delta t} + q'' A_{xz} (b_c - 1). \end{aligned} \quad (8)$$

In (8), $b_c = 1$ for interior nodes and $b_c = 0$ for the top of the silicon chips where a heat flux q'' is present. For this model, the heat flux is determined simultaneously by the electrical simulator representing the instantaneous dissipated power of a particular device and is an input port to the model. The areas A_{yz} , A_{xz} , and A_{xy} represent the cross-sectional areas of the control volume

$$\begin{aligned} A_{yz} &= \left(\frac{d_{yT} + d_{yB}}{2} \right) \left(\frac{d_{zB} + d_{zF}}{2} \right), \\ A_{xz} &= \left(\frac{d_{xL} + d_{xR}}{2} \right) \left(\frac{d_{zB} + d_{zF}}{2} \right), \\ A_{xy} &= \left(\frac{d_{xL} + d_{xR}}{2} \right) \left(\frac{d_{yT} + d_{yB}}{2} \right). \end{aligned} \quad (9)$$

The stored energy E_{xyz} within the control volume is given as

$$\begin{aligned} E_{xyz} &= \frac{1}{8} (d_{zF} + d_{zB}) (d_{xL} + d_{xR}) (\rho_{i-1} c_{i-1} d_{yB} \\ & + \rho_{i+1} c_{i+1} d_{yT}). \end{aligned} \quad (10)$$

The average thermal conductivity taking into account the average thermal conductivity at material interfaces is given by

$$k_{avg} = \frac{d_{yB} k_{i-1} + d_{yT} k_{i+1}}{d_{yT} + d_{yB}}. \quad (11)$$

As mentioned earlier, contact resistance represents the imperfect thermal contact between materials. The existence of a finite contact resistance is due to surface roughness effects between materials resulting in a temperature drop across the interface. In high-power applications, this drop is not negligible and can result in significant temperature rise and should be accounted for in the thermal model. The contact resistance is included in (8) by including the thermal contact conductance coefficient h_{ci} . This coefficient is a function of the two interface materials and the medium between the materials (i.e., air or thermal grease,

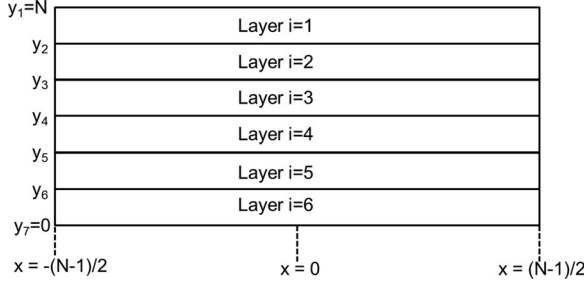


Fig. 5 2-D, 6 six-layer validation model.

etc.). The model in this paper included thermal contact resistance between the DBC and the module baseplate. In addition, thermal resistance was included between the module and the temperature-controlled heat sink.

To determine the unknown nodal temperatures at $t + \Delta t$, the corresponding nodes must be solved simultaneously at each time step. The nodal equations in this paper were implemented in MATLAB, and the matrix inversion technique was used to solve the corresponding nodal equations at each time step. In this manner, materials with nonlinear thermal conductivities such as silicon given by (2) can be updated at each time step.

III. MODEL VALIDATION

A. 2-D Discrete Fourier Series Model

A discretized, 2-D temperature field was used to model (1), since it lends itself to a straightforward, approximate specification of an arbitrary, dynamic heat flux at the upper surface boundary. The temperature grid was $N \times N$, N odd, with a sufficiently high grid resolution to reduce approximation error. In this particular application, a square wave function was used to model the applied surface heat flux distribution. It was modeled using a discrete Fourier series (DFS). Due to the extremely fine grid resolution used in the validation modeling, all discrete derivatives were approximated using continuous derivatives. Fig. 5 illustrates the geometry that was used in the development of the 2-D, six-layer validation model.

The total solution to (1) was sought that contained both a transient T_{rr} and a steady-state T_{ss} solution, i.e.

$$T(x_m, y_n, t) = T_{TR}(x_m, y_n, t) + T_{SS}(x_m, y_n). \quad (12)$$

A 2-D, DFS form of the transient solution can be written as

$$T_{TR}(x_m, y_n, t) = \sum_{jk} C_{jk} \cdot \sin(\lambda_j \cdot y_n) \cdot \cos(\lambda_k \cdot x_m) \cdot e^{-\kappa \cdot \lambda_{jk}^2 \cdot t} \quad (13)$$

where $\lambda_{jk}^2 = \lambda_j^2 + \lambda_k^2$ and the individual eigenvalues satisfy the applied homogenous boundary conditions, i.e., zero heat flux at the upper and lateral sides of the chip, and zero temperature at the base of the chip. The DFS coefficient C_{jk} satisfies the initial boundary condition for the transient solution at time $t = 0$.

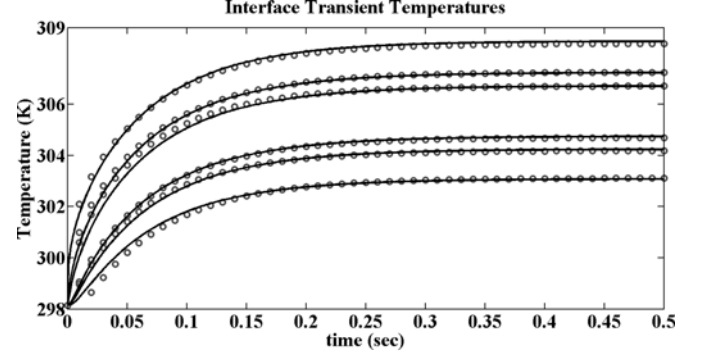


Fig. 6. Transient interface temperatures.

A 2-D, DFS form of the steady state solution for a certain layer (i) can be written as

$$\begin{aligned} i = 1 : T_{SS,1}(x_m, y_n) &= 1/2 \cdot (a_{10} \cdot y_n + b_{10}) \\ &+ \sum_{j=1}^{N-1} \left(a_{1j} \cdot \sinh \left(j \cdot 2\pi \cdot \frac{y_n - y_1}{N} \right) \right. \\ &\quad \left. + b_{1j} \cdot \cosh \left(j \cdot 2\pi \cdot \frac{y_n - y_1}{N} \right) \right) \\ &\quad \cdot \cos \left(j \cdot \frac{2\pi}{N} \cdot x_m \right) \end{aligned} \quad (14)$$

$$\begin{aligned} i > 1 : T_{SS,i}(x_m, y_n) &= 1/2 \cdot (a_{i0} \cdot y_n + b_{i0}) \\ &+ \sum_{j=1}^{N-1} \left(a_{ij} \cdot \sinh \left(j \cdot 2\pi \cdot \frac{y_n - y_{i+1}}{N} \right) \right. \\ &\quad \left. + b_{ij} \cdot \cosh \left(j \cdot 2\pi \cdot \frac{y_n - y_{i+1}}{N} \right) \right) \\ &\quad \cdot \cos \left(j \cdot \frac{2\pi}{N} \cdot x_m \right). \end{aligned} \quad (15)$$

The DFS coefficients in (14) and (15) are solved by satisfying the interfacial boundary conditions, i.e., matching heat flux and temperature at each of the layer interfaces; and the surface and bottom boundary conditions, including Fourier's Law of heat conduction and a constant base temperature, respectively. The insulated boundary conditions at $x_m = +(N-1)/2, -(N-1)/2$ are satisfied using the $\cos((2\pi j/N) \cdot x_m)$ function.

B. Model Validation

The DFS model is used for validation of the FDM model under controlled dimensions and boundary conditions for a two-chip asymmetrical heating condition. The 3-D FDM model was reduced to 2-D for this validation. This was done by applying the appropriate heat flux boundary condition on the top surface of the module that results in a two dimensional heat conduction problem. Figs. 6 and 7 show a surface temperature versus time

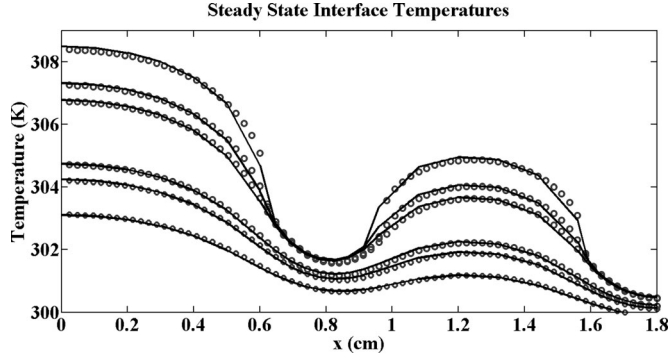
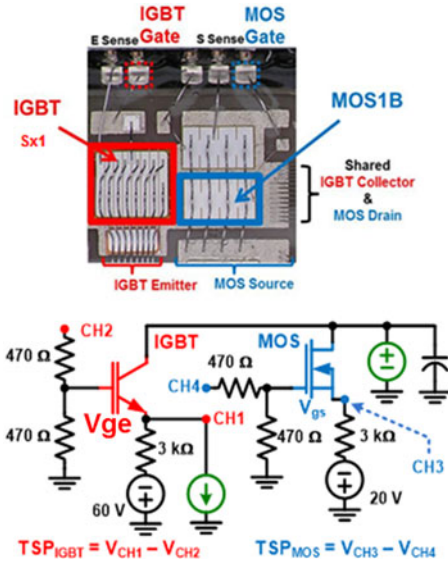

 Fig. 7. Steady-state interface temperatures versus x dimension.


Fig. 8. Thermal coupling TSP measurement circuit.

plot, and a temperature versus x dimension plot, respectively, at each layer interface. Both Figs. 6 and 7 illustrate excellent agreement between both the FDM model and the DFS validation model.

IV. MEASURED AND SIMULATED RESULTS

A. Test Circuit

For the thermal cross-coupling experiment, an auxiliary IGBT S_{x1} and a main bridge MOSFET M_1 are chosen due to their close proximity and common DBC layers. M_1 is made up of two chips—MOS1A and MOS1B—and is shown in Fig. 8. Also, shown in Fig. 8 is the test circuit used to measure the transient heating and lateral coupling where the IGBT and MOS under test are the chosen devices S_{x1} and MOS1B, respectively.

S_{x1} and MOS1B are biased with small auxiliary currents comprised of the 60 and 20 V power supplies along with the 3 k Ω resistors to establish an initial threshold voltage measurement shown as V_{ge} and V_{gs} in Fig. 8 and provide the corresponding TSPs for S_{x1} and MOS1B. The 470 Ω gate resistor serves as a damping resistor to prevent oscillation. The threshold mea-

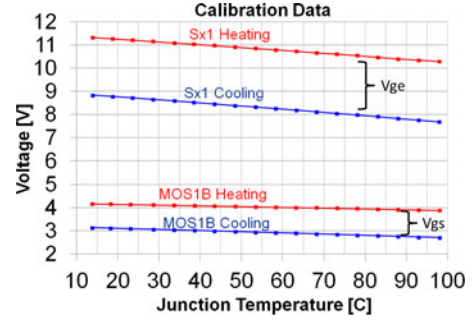


Fig. 9. Calibration data double TSP experiment.

surements are set up as differential measurements from the data acquisition system because a substantial common mode voltage spike appears on the gate and cathode during switching. This is due to gate charging current interacting with the gate resistor used to prevent oscillation. The small bias currents also provides for the capability of using the TSP measurement during the cooling phase. A heavily bypassed voltage power supply is used to maintain a constant voltage across both the S_{x1} and MOS1B. S_{x1} is pulsed from the small bias current to a large current from a custom-made precision current source that features high-speed gating and current control in 0.1 A increments up to 25.5 A [25].

The power dissipation in S_{x1} due to the large pulsed current and constant device voltage causes the device to heat up causing the TSP of S_{x1} to change. At the same time, the TSP of MOS1B changes due to the heat source provided by the dissipation in S_{x1} . The measured temperature rise in MOS1B due to the power dissipation in S_{x1} allows model validation of lateral thermal heat coupling between chips in close proximity.

B. Test Procedure

The measurement of the IGBT and MOSFET transient heating requires two parts. First, the TSP of each device must be calibrated at known operating conditions and at a series of known temperatures. Second, with the heat sink at a fixed and known temperature, the IGBT is subjected to a longer transient heating pulse where the IGBT temperature increase will result in the MOSFET temperature increase through thermal coupling within a common DBC. The TSP for the IGBT S_{x1} is the measured gate to emitter voltage V_{ge} in Fig. 8. The TSP for the MOSFET MOS1B is the measured gate to source voltage V_{gs} in Fig. 8. Fixed temperatures are achieved by having the DUT mounted on a temperature-controlled heat sink. The same test circuit shown in Fig. 8 can be used for the calibration and transient heating measurement; the difference between these is determined by the pulsewidth.

For the calibration curve, the operating conditions that need to be specified include the collector to emitter voltage and collector current. Using a temperature-controlled baseplate temperature, a very short pulsewidth is applied to the IGBT to avoid significant chip heating and the TSP of the IGBT and MOSFET are recorded over temperature. The result is shown in Fig. 9 for S_{x1}

and MOS1B. The TSP is measured for each device during a heating and cooling phase. The heating phase refers to the TSP that is measured during the pulse duration and the cooling phase refers to the TSP that is measured after the pulse is removed. The result of this calibration curve is an established relationship between chip temperature and the corresponding TSP values of the IGBT and MOSFET.

For the transient heating measurement, the current and voltage conditions are the same as was for the TSP calibration. The temperature of the heat sink is held constant at one temperature for all heating measurements. The current pulsewidth of S_{x1} is increased long enough to show significant chip heating of both S_{x1} and MOS1B. The TSP values for both S_{x1} and MOS1B are recorded as a function of time, and the voltage waveforms are mapped into temperature as a function of time by using the calibration data. Each IGBT and MOSFET operating condition requires a new calibration. Due to the time consuming process of calibration, a fully automated system has been developed at NIST.

C. Operating Conditions

S_{x1} is pulsed with a peak power of 100 W under a variety of pulsewidth conditions to provide multiple points of validation for both S_{x1} and MOS1B. The TSP of S_{x1} and MOS1B are monitored while S_{x1} is pulsed. The average power applied to the IGBT is varied by using different power pulsewidths of constant power amplitude and multiple successive pulses are also used to capture dynamic transient heating of the IGBT and neighboring MOSFET. The pulse repetition frequency is made low enough to capture and study the thermal time constant of the heat propagation from the IGBT to the MOSFET. Much higher speed shorter pulses can be used to capture the resolution required to validate the silicon chip thermal model under a high-power short condition. This has been done in previous works by the authors of this study [25].

In [25], the cooling effects had not been measured and only transient heating was studied under very short power duration. The new system with cooling functionality allows successive pulse trains to be generated where the temperature of the device does not return to the heat sink temperature before the next pulse. Therefore, a thermal steady state can be generated and used for further model validation and study of thermal coupling.

D. Measured Data Versus FDM Model Prediction

The FDM compact model was simulated with the dimensions from Fig. 3 and the material properties from Table I. A pulsed heat flux was applied to S_{x1} and the junction temperature of S_{x1} and MOS1B were monitored in the model under the same peak power and duty cycle conditions from the experiment. The module was mounted onto a baseplate constructed of two copper plates with piping and heaters installed in the bottom plate. The two copper plates are joined together by thermal grease and screws. Cold water is run through the piping and the heater is controlled by applying a voltage to the heater. This voltage is the output from a feedback controller measuring the tempera-

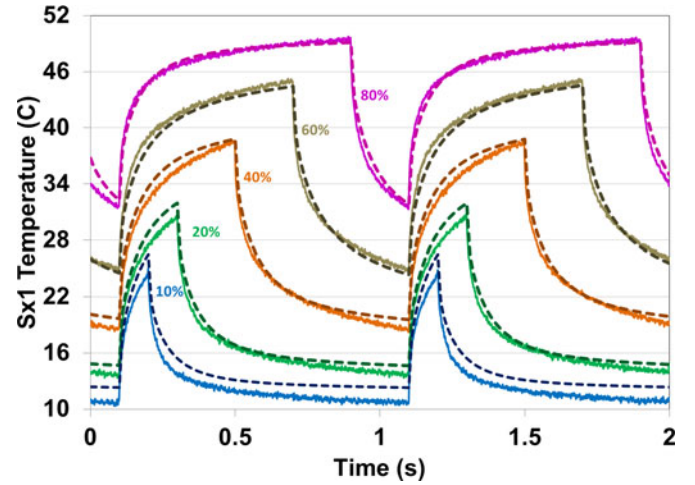


Fig. 10. S_{x1} transient heating measured versus simulated.

ture of a thermal couple located in the bottom baseplate. For our experiment, we chose not to run the heater and applied the highest water pressure possible to bring the baseplate temperature below room temperature. This, however, does not guarantee the entire baseplate is at the same temperature. Therefore, the thermal mass and resistance of the two copper plates were included as an additional layer in the model with a constant temperature assumed at the very bottom.

In addition, contact resistance was added to represent the poor thermal contact at the interface between the two copper baseplates. The thermal contact conductance coefficients were not determined experimentally. Therefore, an assumption on the conductance coefficient is assumed based on a copper to copper interface and then adjusted within reason to achieve the correct offset temperature resulting from the measured data. A copper to copper interface thermal conductance coefficient of $5.5 \text{ W}/(\text{cm}^2 \cdot \text{K})$ [28] was applied at the interface of the two copper baseplates and adjusted to $1.2 \text{ W}/(\text{cm}^2 \cdot \text{K})$. This implies very poor contact between the two copper to copper interfaces. Future measurements should remove this interface. The module to baseplate coefficient was adjusted from 5.5 to $10 \text{ W}/(\text{cm}^2 \cdot \text{K})$, which implies better thermal contact between the module and baseplate.

Fig. 10 shows the measured versus simulated data under a variety of pulsewidths of S_{x1} , and Fig. 13 shows the resulting MOS1B temperature resulting from the heating of S_{x1} . There is excellent agreement between the measurement and measured data with the biggest error within a few degrees. Both the heating and cooling portions of the curves show very good agreement thus validating the entire DBC under a variety of conditions. In addition, the thermal coupling temperature and time constant from S_{x1} to MOS1B are captured very nicely with the new model. It should be noted that the measurement points within the model were taken at the center of the chip. This may not be as accurate for capturing the MOSFET temperature due to coupling since there is a temperature gradient across the top of the chip. Therefore, computing the average temperature of the top of chip may result in a closer match in Fig. 11.

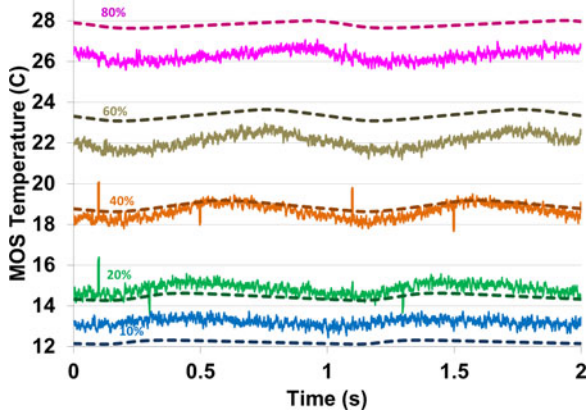


Fig. 11. MOS1B transient heating measured versus simulated.

V. INVERTER LOSS CONSIDERATION

The major losses in an inverter are due to conduction loss and switching loss. The major switching loss is due to diode reverse recovery induced turn-on loss and IGBT turn-off current induced turn-off loss. Turn-on switching loss due to voltage and current crossover during commutation can be reduced with soft switching control as suggested in [1]. The IGBT turn-off loss can result in large instantaneous power dissipation while the tail current is decaying and the IGBT is supporting a large voltage. This large instantaneous turn off loss can result in device failure in some cases due to a large instantaneous junction temperature. This effect is one of the major motivations behind dynamic electrothermal modeling. The thermal model proposed in this study can coexist with the physics-based device models in an electrical switching simulation and predict instantaneous junction temperature within a switching cycle. In addition, short-circuit or failure modes can be studied. The electrothermal model, therefore, becomes a valuable tool to the engineer during the design process and can help aid the engineer in predicting system efficiency and system reliability.

As an example of the capability of the thermal model proposed in this study, a dynamic power dissipation profile is used as an input to the thermal model. The power dissipation profile represents the instantaneous power dissipation of a typical IGBT in a switching inverter. Both turn-on and turn-off losses, in addition to conduction loss, are included in the instantaneous power dissipation. Therefore, the model can be tested with inputs containing the high-frequency content associated with switching loss within a switching cycle and the low-frequency content associated with the inverter line frequency. The profile models a dual modulation method for a 280 V, 55 kW full-bridge inverter with a switching frequency of 10 kHz and an inverter line frequency of 60 Hz. Assuming a 0.83 power factor, the peak phase current is 315 A. The average conduction loss for an IGBT is given by

$$P_{c-IGBT} = I_m V_t \left(\frac{1}{2\pi} + \frac{1}{8} M \cos \phi \right) + I_m^2 R_{ce} \left(\frac{1}{8} + \frac{M}{3\pi} \cos \phi \right) \quad (16)$$

where I_m is the peak output current, V_t is the IGBT fixed voltage drop under zero current condition, R_{ce} is the IGBT on-drop

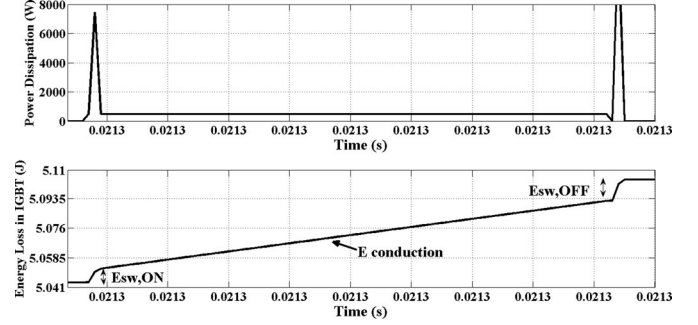


Fig. 12. Loss profile applied to FDM model. Power (top) and energy (bottom).

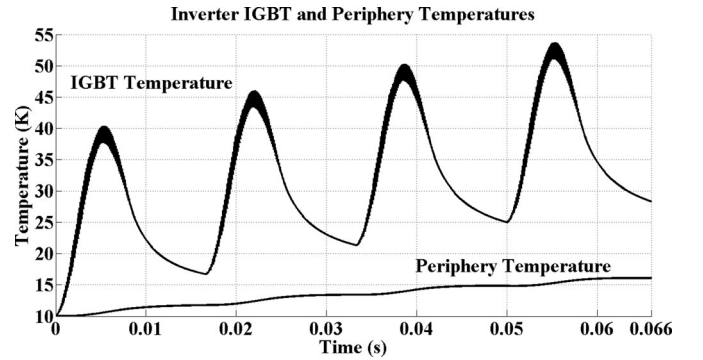


Fig. 13. Inverter IGBT and periphery temperature.

resistance, M is the modulation index, and φ is the power factor angle. The average switching loss for an IGBT is given by

$$P_{sw-IGBT} = \alpha I_m^\beta k_g f_{sw} \frac{1}{2\sqrt{\pi}} \frac{V_{dc}}{V_{test}} \frac{\Gamma((\beta+1)/2)}{\Gamma((\beta/2)+1)} \quad (17)$$

where k_g is the gate drive stiffness factor, f_{sw} the switching frequency, α and β are the turn-on and turn-off energy coefficients, and V_{dc} and V_{test} represent the dc-bus voltage and test voltage for switching energy coefficients, respectively. The energy coefficients are readily available from the energy curves given by the IGBT data sheets. For this example the IGBT part number CM400DY-12NF is used. The calculated average conduction loss was approximately 120 W. The average turn-on and turn-off loss are 23 and 40 W, respectively. The total average device loss is therefore 183 W. All loss calculations were made at 25 °C. The average loss calculations resulting from (16) and (17) were mapped into an instantaneous power dissipation profile and used as an input to the thermal model. Fig. 12 shows the IGBT instantaneous power dissipation and energy during a single switching cycle of the inverter. E_{sw} represents the energy at turn on and turn off.

Fig. 13 shows the IGBT junction temperature in addition to the lateral peripheral temperature of the package. This shows that the thermal model predicts a lateral peripheral temperature rise due to thermal coupling as a result of power dissipated in the IGBT. As can be seen, there is not only the low-frequency content associated with the inverter frequency but also the higher frequency associated with switching loss.

VI. CONCLUSION

A full 3-D multilayer, multichip asymmetrical thermal compact model based on finite differences was presented. The model was first validated with a DFS-based model, including both a steady-state and transient solution. Excellent agreement was achieved between the DFS and FDM solutions. In addition, very good agreement was achieved between the FDM thermal model and measured data resulting from the newly developed high-speed double TSP method. The disagreement between the FDM prediction and measurement is most likely attributed to the uncertainty in the boundary condition at the bottom of the module and the location of the measurement point within the model.

The FDM thermal model was also simulated with a dynamic power dissipation profile of a typical IGBT showing its capability in response to both high- and low-frequency content.

In summary, the first attempt at a full 3-D thermal compact model using finite differences for use in electrothermal models was attempted and validated with very good results. Computers are improving in speed due to multicore processors and multi-thread capabilities making finite-difference-based compact thermal models possible. Future work will show a full electrothermal simulation of the soft switching inverter using the new compact FDM thermal model.

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