

Cryogenic Etching of High Aspect Ratio 400 nm Pitch Silicon Gratings

Houxun Miao, Lei Chen, Mona Mirzaeimoghri, Richard Kasica and Han Wen

Abstract— The cryogenic process and Bosch process are two widely used processes for reactive ion etching of high aspect ratio silicon structures. This paper focuses on the cryogenic deep etching of 400 nm pitch silicon gratings with various etching mask materials including polymer, Cr, SiO₂ and Cr on polymer. The undercut is found to be the key factor limiting the achievable aspect ratio for the direct hard masks of Cr and SiO₂, while the etch selectivity responds to the limitation of the polymer mask. The Cr on polymer mask provides the same high selectivity as Cr and reduces the excessive undercut introduced by direct hard masks. By optimizing the etching parameters, we etched a 400 nm pitch grating to ≈ 10.6 μm depth, corresponding to an aspect ratio of ≈ 53 .

Index Terms— Cryogenic silicon etching, deep reactive ion etching, high aspect ratio silicon grating

I. INTRODUCTION

ETCHING of high aspect ratio silicon structures is a crucial step in many fabrication processes with wide applications including micro-electro-mechanical-systems (MEMS) [1], deep trench capacitors [2], through-silicon-via (TSV) packaging [3], microfluidic devices [4] and x-ray optics [5-12]. In x-ray optics, high aspect ratio gratings [5-9] and zone plates [10-12] have broad applications in x-ray phase contrast imaging [13-15], x-ray astronomy [9], and high resolution x-ray microscopy [16]. The performance of these devices relies on the aspect ratio, the size and the profile of the structures. We focus on the etching of high aspect ratio, a few hundred nm period silicon gratings. The aspect ratio is defined as the ratio between the etching depth and half pitch of the grating throughout the study. The narrow trench/wall structures of gratings impose significantly more difficulties than the etching of isolated narrow lines or trenches, since the undercut and the negative taper can damage the thin walls and closely placed thin walls are prone to collapse due to electrostatic forces from charging effects.

Both wet and dry processes have been developed for high-aspect ratio silicon grating etching. Potassium hydroxide (KOH) etch and metal assisted chemical etch (MacEtch) are

two well developed wet processes. KOH etching requires proper alignment between the trenches and the crystal orientation of a $\langle 110 \rangle$ silicon wafer and has been used to etch 200 nm pitch gratings down to 6 μm , corresponding to an aspect ratio of 60 [9, 17]. Vertical directionality controlled MacEtch, working with properly designed pattern and balancing structures, has been demonstrated to etch 200 nm pitch gratings down to 6.6 μm (aspect ratio of 66) [12]. Despite of certain advantages of the wet processes, we focus on dry processes. The Bosch process [18] and the cryogenic process [19] are two best known deep silicon reactive ion etching (RIE) processes [20]. Bosch process alternates isotropic etch and passivation steps to achieve directional etching. By carefully tuning the etch parameters, the intrinsic scallops on the sidewall can be reduced. The Bosch process has been used to etch 200 nm-pitch gratings to 6 μm in depth (aspect ratio of 60) [21]. The cryogenic process utilize a plasma of combined sulfur hexafluoride (SF₆) and oxygen (O₂) to passivate the sidewall (where a layer of SiO_xF_y is formed) and etch the bottom of silicon simultaneously [22-24]. The etching is typically carried out at -130 to -100 °C. The continuous process eliminates sidewall scallops and provides vertical sidewalls without observable roughness. The cryogenic process has been used to etch 200 nm pitch gratings to 4 μm in depth with regular shape and smooth sidewalls, without the need of any supporting cross bridges as has been used in the other three etching techniques [8].

Here we describe the optimization of the cryogenic recipes for high aspect ratio submicron silicon structure etching using the example of 400 nm pitch gratings. In particular, a etch mask of Cr on polymer was found to perform the best among several options. The effects of etching parameters [22, 23, 25, 26] and mask materials [26, 27] on cryogenic etching of silicon have been extendedly studied. However, most of the studies were made in the low aspect ratio regime, under the situations of either deep etch of large micron scale structures or light etch of small nanometer scale structures [22, 23, 28]. Although valuable information can be extracted, the constraints imposed by small feature size and high aspect ratio are yet to be addressed. We first observed the etching characteristics of different mask materials at a moderate aspect ratio of around

Manuscript submitted on October 9, 2015. This work was supported by the the Intramural Research Program of the National Heart, Lung, and Blood Institute, National Institutes of Health.

H. Miao, M. Mirzaeimoghri and H. Wen are with the National Institutes of Health, Bethesda, MD 20892 USA (e-mail: houxun.miao@nih.gov, mona.mirzaeimoghri@nih.gov, han.wen@nih.gov).

L. Chen and R. Kasica are with the National Institute of Standards and Technology, Gaithersburg, MD 20899 USA (e-mail: lei.chen@nist.gov, richard.kasica@nist.gov).

18. The undercut represents a severe problem for the direct hard masks and its response to the gas flow ratio (the most sensitive parameter) [22-25] was studied for the direct hard masks and Cr-on-polymer mask. Then with the Cr-on-polymer mask, the response of the etching profile to the tuning of other individual etching parameters was studied. Based on the knowledge obtained, recipes were developed for the silicon gratings to attain an aspect ratio of 53 with the Cr-on-polymer mask.

II. METHODS

Figure 1 shows the cross-section scanning electron microscopy (SEM) images of the four types of grating masks with a same period of 400 nm. The polymer mask (ZEP520) was directly patterned using electron-beam lithography. Limited by the cost of electron-beam lithography, the grating area of each sample is 3 mm x 20 μm . The width of the grating line immediately above the silicon surface is ≈ 160 nm (Fig. 1A). The thickness of the resist is ≈ 540 nm. The other three masks were patterned via nanoimprint lithography with NXR-1025 nanoimprint resist (Nanonex corp.). The grating master template is a 150 mm silicon wafer, patterned via optical interference lithography and RIE of silicon. The template grating has approximately rectangular trenches of ≈ 150 nm depth. For the Cr mask, 30 nm Cr was coated on a silicon wafer via electron-beam evaporation. For the SiO_2 mask, 300 nm SiO_2 was first grown on a silicon wafer in a wet oxidation furnace and then 30 nm Cr was coated. The grating pattern is transferred to the resist spin coated on silicon or Cr via nanoimprint lithography. For the Cr and the SiO_2 masks, the residual layer of the nanoimprint lithography was first removed via O_2 plasma, then 30 nm Cr was ion milled through. The Cr mask (Fig. 1B) was formed after the resist was cleaned. The SiO_2 mask (Fig. 1C) was created by etching through the 300 nm SiO_2 layer with a C_4F_8 - O_2 recipe and cleaning the Cr mask with O_2 plasma. For the Cr-on-polymer mask (Fig. 1D), 10 nm Cr was deposited via electron beam evaporation at a 30° incident angle to the wafer surface from each side of the grating lines. The residue resist layer of the nanoimprint lithography was

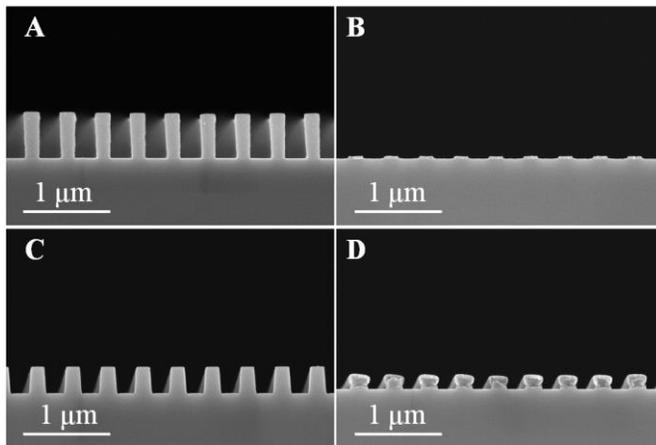


Fig. 1. Cross-section SEM images of 400 nm period grating masks on silicon with different materials of ZEP520 (A), Cr (B), SiO_2 (C) and Cr on nanoimprint resist (D).

removed via O_2 plasma. The grating line widths above the silicon surface are ≈ 200 nm for these three types of masks.

The wafers were cleaved into 1 cm x 1 cm squares for the etching test. We also carried out an experiment with a 5 cm x 5 cm square sample masked by Cr on polymer, which yielded similar etching rate and profile as the smaller sample, suggesting that etching of small samples can be used to calibrate the etcher before etching large samples. The cryogenic etch process was carried out on an inductively-coupled plasma (ICP) etcher from Oxford Instruments (Oxford Plasmalab 100). The samples were bonded using pump oil on a 100 mm silicon wafer with thermally-grown SiO_2 on top, which is a reliable approach for heat dissipation during the etching. The etching results were characterized by SEM.

III. RESULTS

The cryogenic temperature was controlled to $-110 \pm 2^\circ\text{C}$ throughout the study. We first studied the etching characteristics of 400 nm pitch gratings with different mask materials. The parameters of the optimized etching recipe were: ICP power of 1000 W, RF power of 10 W, pressure of 8 mT, SF_6 flow rate of 52 sccm, and O_2 flow rate of 8 sccm. The etching time is 2 min. Figure 2 shows the SEM images of the etching profiles corresponding to various mask materials. The depths of the trenches were 3.9, 3.8, 3.7 and 3.5 μm , the widths at the half depth were ≈ 185 , 200, 190 and 205 nm, for polymer, Cr, SiO_2 and Cr-on-polymer masks, respectively. The slightly higher etching rate with the polymer mask is due to the slightly wider trenches. From Figs. 1 and 2, the etching selectivity is estimated to be ≈ 15 , > 500 , and ≈ 60 for polymer, Cr and SiO_2 masks. The selectivity of the Cr-on-polymer mask is the same

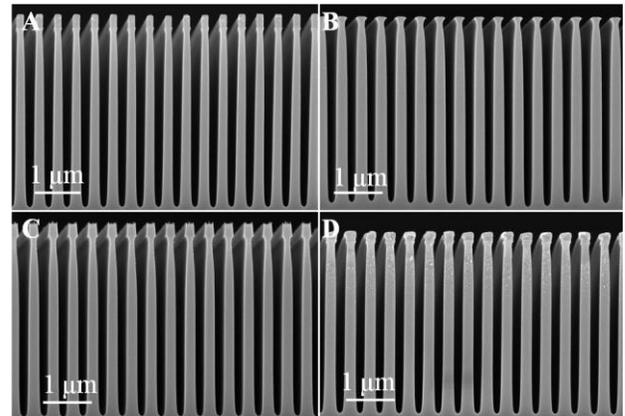


Fig. 2. Profiles after 2 min etch with the recipe of 1000 W ICP power, 10 W RF power, 8 mT pressure, 52 sccm SF_6 and 8 sccm O_2 flow rates. The mask materials are ZEP 520 (A), Cr (B), SiO_2 (C) and Cr on nanoimprint resist (D).

as Cr mask before the Cr is etched away.

More severe undercut was observed beneath the mask materials for the Cr and SiO_2 masks. These are shown in Fig. 3 by SEM of the region around the masks. The width of the polymer mask shrank from ≈ 160 nm to ≈ 125 nm for the initial 2 min etching and did not further shrink much for longer etching. The smallest width of the silicon wall was almost the same as the width of the resist, indicating that the undercut is

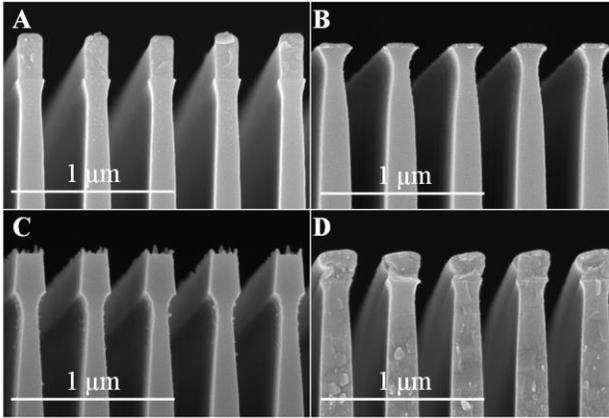


Fig. 3. Zoomed images of the region near the masks of Fig. 2.

negligible for the polymer mask. The undercut of the Cr-on-polymer mask was found to be close to the polymer mask for the 2 min etching. We studied the dependence of the undercut on the etching parameters for the masks of Cr, SiO₂ and Cr on polymer and found it to be most sensitive to the SF₆ and O₂ flow ratio. At a fixed SF₆ flow rate of 52 sccm, Fig. 4 illustrates how the undercut, the minimum silicon width at the neck and the silicon width at half depth varied with the O₂ flow rate. The undercut was measured as half the difference between the silicon width immediately under the mask and the minimum width of the neck below. Figure 5 shows the corresponding etching depth. With lower O₂ flow rates (< 8 sccm), the undercut increased and the width of the neck decreased rapidly for all the three mask materials. As a result, the sample with Cr mask did not survive a 2 min etching with 6.5 sccm O₂ flow rate. With higher O₂ flow rates (> 8 sccm), the undercut was reduced and the minimal width increased. Clearly increasing O₂ flow rate favors the formation of the lateral etching passivation layer SiO_xF_y on sidewalls. [J. Micromech. Microeng., 14 (2004), pp. 190–196]. The trade-offs were reduced etching depth (rate) (Fig. 5) [Journal of Applied Physics 52, 162 (1981); doi: 10.1063/1.328468] and increased width at half depth, which prevent deep silicon etching. The undercut of the Cr-on-polymer mask was substantially smaller than the Cr and SiO₂ masks. We attribute this to the formation of an additional sidewall passivation layer. Carbon in the resist underneath the Cr may react to F plasma and form (C_xF_y)_n polymer [Macromolecules Vol. 7, No. 3, May-June 1974], through the Si etching process. As shown in Fig. 5, The etching depth decreased monotonically with the increase of the O₂ flow rate according to the increased passivation.

Since the Cr-on-polymer mask provides both good selectivity and reasonably small undercut, it allows free tuning of the other parameters. We illustrate the recipe optimization with this mask for high aspect ratio silicon grating etching. We first studied the response of etching profiles to the other etching parameters including the chamber pressure, the ICP power and the RF power with 2 min etching time. The results are summarized in Fig. 6. Figures 6A and 6B show the etching profiles at 6 mT and 15 mT chamber pressure, respectively. At 6 mT, the lower pressure increased the kinetic energy of the ion flux, thus reduced the level of passivation and straightened the

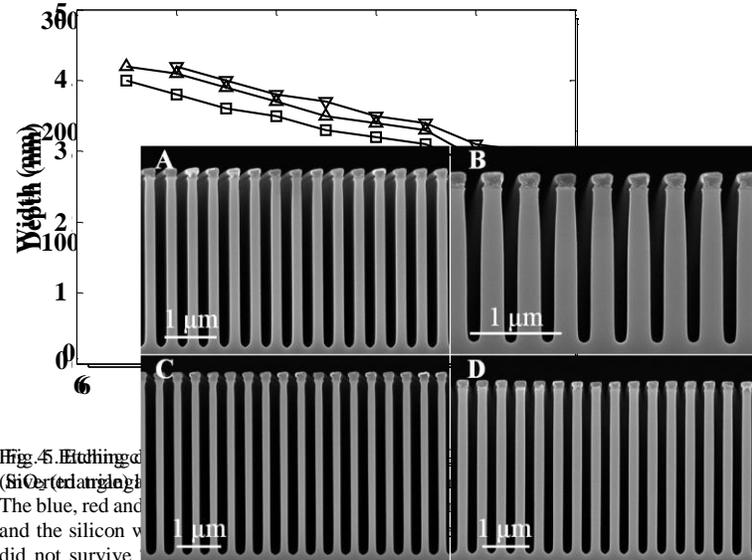


Fig. 5. Etching depth (SiO₂ etching) vs. O₂ flow rate. The blue, red and black symbols represent Cr, SiO₂ and the silicon width at half depth, respectively. The silicon width was taken as the average of the two sides of the trench. The images were taken after 2 min etching, where a single etching parameter was changed from the recipe used in Fig. 2D in each image. The tuned parameters were: (A) 6 mT chamber pressure, (B) 15 mT chamber pressure, (C) 1500 W ICP power and (D) 30 W RF power.

sidewall of the trenches. The etching depth decreased slightly to 3.2 μm in accordance with the reduction of the ion density. The silicon width at half depth was 185 nm, the undercut was ≈ 29 nm and the slope of the sidewall is ≈ 89.5°. At 15 mT chamber pressure, the kinetic energy of the ion flux was lower and the trenches were over-passivated. As a result, the etching depth was only 1.6 μm, the undercut was 13 nm and the slope of the sidewall is ≈ 88.7°. The ICP power was set to 700 W and 1500 W. At 700 W, the plasma failed to maintain after striking at higher (2500 W) ICP power. Figure 6C shows the etching profile at 1500 W ICP power. The etching depth was 4 μm, the silicon width at the half depth was 155 nm and the undercut was 34 nm. The walls had a marginal negative taper (slope of the sidewall ≈ 90.4°) due to a slight under-passivation. The increased ion density elevated the etching speed and reduced passivation. The RF power was tuned from the initial setting of 10 W to 30 W. Figure 6D shows the etching profile at 30 W power. The etch depth was 3.5 μm. The high kinetic energy of the ion straightened the sidewall profile. As a result, the slope of the sidewall is ≈ 90° and the undercut is ≈ 13 nm.

The overall recipe optimization involves adjusting the above parameters to balance etching against passivation within the allowance of the undercut. Choosing the optimal chamber pressure of 8 mT, we developed three recipes of different ICP and RF power combinations by adjusting the SF₆ to O₂ flow ratio. Figure 7A shows the etching profile of a recipe at 1000 W ICP power, 10 W RF power, 52 sccm SF₆ flow rate and 8 sccm O₂ flow rate. The etching time was 10 min and the etch depth was 10.6 μm, corresponding to an aspect ratio of 53. Figure 7B shows the etching profile of a recipe at 1500 W ICP power, 10 W RF power, 52 sccm SF₆ and 10 sccm O₂ flow rates. The etching time was 6 min and the trenches were etched to 8.3 μm depth. The slight under-passivation from higher ICP power was balanced by increasing the O₂ flow rate. Although the etching rate was higher than the recipe used in Fig. 7A, the more pronounced undercut prevented further etching. Figure 7C shows the etching profile of a recipe at 1000 W ICP power, 30 W RF power, 52 sccm SF₆ and 9 sccm O₂ flow rates. The etching time was 6 min and the depth was 8 μm. Again, the undercut limited the achievable aspect ratio. We noted that for 2 min etching, the recipe with 30 W RF power (Fig. 6D) produced the smallest undercut. We attribute the small undercut to the removing of the silicon bumpers extended out of the mask with high energy ions. For longer etching, the recipe with 10 W RF power (Fig. 7A) gave the smallest undercut for a given etching depth.

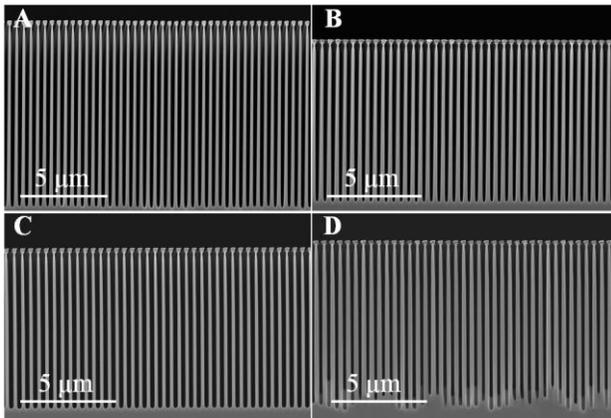


Fig. 7. Cross-section SEM images of deeply etched samples with recipes developed at 10 W RF power and 1000 W ICP power (A), 10 W RF power and 1500 W ICP power (B), and 30 W RF power and 1000 W ICP power (C). (D) An example showing that over passivation results in uneven depths during deep silicon etching. The undercuts were estimated to be ≈ 77 μm for (A) and (B), ≈ 72 μm for (C) and ≈ 54 μm for (D).

It is worth noting that the level of passivation tends to decrease as the etch proceeds deeper, such that a slight over-passivation (positive taper) at the beginning is preferred (Fig. 2D). A recipe that starts with a vertical or negatively tapered profile results in further narrowing of the walls which are mechanically less stable and susceptible to damage before reaching the desired etch depth. On the other hand, too much passivation resulted in uneven trench depths such as the example shown in Fig. 7D, which was etched for 10 minutes

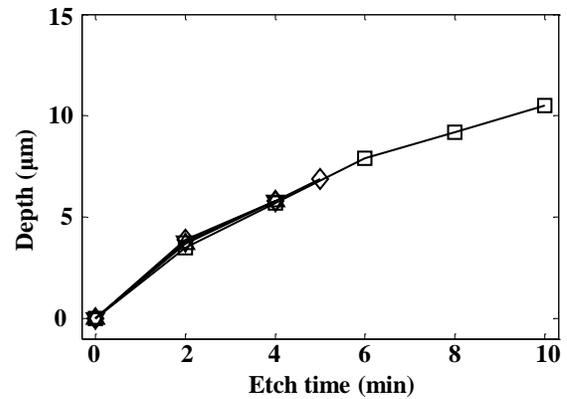


Fig. 8. Etching depth as a function of etching time for different masks: ZEP520 (diamond), Cr (inverted triangle), SiO₂ (triangle) and Cr on polymer (square).

using a recipe with 1000 W ICP power, 10 W RF power, 52 sccm SF₆ flow rate and 10 sccm O₂ flow rate.

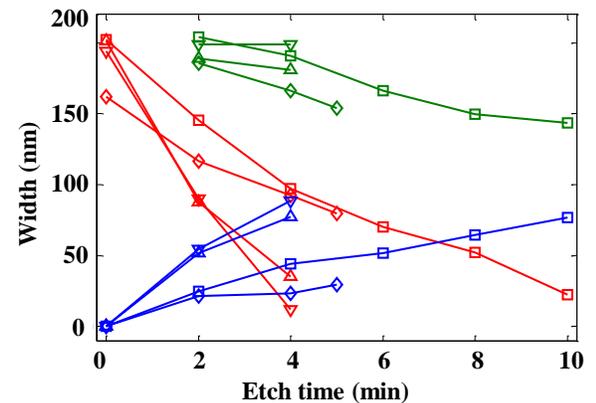


Fig. 9. Etch characteristic widths vs the etch time for the four types of masks: ZEP 520 (diamond), Cr (inverted triangle), SiO₂ (triangle) and Cr on polymer (square). The blue, red and green curves represent undercut, minimum silicon width and the silicon width at the half depth, respectively. For etch time of 0, the undercut was taken as 0 and the minimal silicon widths near the masks are taken as the mask widths immediately above silicon.

With the recipe used in Fig. 7A, we further tested the etching characteristics of the four different masks by varying the etching time. The etching depths are illustrated in Fig. 8. The ZEP520 mask did not survive 6 min etching due to the limited thickness and selectivity. The maximum depth achieved was 6.9 μm with 5 min etching, corresponding to an aspect ratio of ≈ 35 . The Cr and SiO₂ masked samples did not survive 5 min etching due to the undercut. The maximum depths achieved were both 5.8 μm with 4 min etching, corresponding to an aspect ratio of 29. The undercut, the minimum silicon width near the mask and the silicon width at half depth are illustrated in Fig. 9. For polymer mask, the undercut did not change much as the etching time increased. The selectivity was the key factor that limited the achievable aspect ratio. For Cr and SiO₂ masks, the undercuts increased rapidly with the etching time and the minimal silicon widths near the mask quickly dropped to below 40 nm after 4 min etching and did not allow further etching before the samples were damaged. The undercut of the Cr-on-

polymer masked sample increased slowly (slightly faster than the polymer only mask) with the etching time. The high etch selectivity and moderate undercut allowed 10 min etching, which yielded a depth of 10.6 μm , corresponding to an aspect ratio of 53.

IV. CONCLUSION AND DISCUSSION

We described the cryogenic process for deep etching of 400 nm pitch silicon gratings with various mask materials. For the polymer mask, the etching selectivity of silicon over resist limits the attainable aspect ratio. For the direct hard masks of Cr and SiO_2 , the undercut limits the achievable aspect ratio. The Cr-on-polymer mask relaxed both constraints. We optimized the recipe for the Cr-on-polymer mask to produce gratings of an aspect ratio of 53. The optimization process was guided primarily by the balance between the etching and passivation within the tolerance of the undercut. A similar approach may be useful for developing recipes of other high aspect ratio structures in silicon.

With the Cr-on-polymer mask, the etching depth is still limited by the undercut beneath the mask. It should be noted

REFERENCES

- [1] I. W. Rangelow, "Critical tasks in high aspect ratio silicon dry etching for microelectromechanical systems," *Journal of Vacuum Science & Technology A*, vol. 21, pp. 1550-1562, 2003.
- [2] G. Wang, *et al.*, "Scaling deep trench based eDRAM on SOI to 32nm and Beyond," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.
- [3] M. Motoyoshi, "Through-silicon via (TSV)," *Proceedings of the IEEE*, vol. 97, pp. 43-48, 2009.
- [4] E. Verpoorte and N. F. de Rooij, "Microfluidics meets MEMS," *Proceedings of the IEEE*, vol. 91, pp. 930-953, 2003.
- [5] D. Noda, *et al.*, "Fabrication of large area diffraction grating using LIGA process," *Microsystem Technologies*, vol. 14, pp. 1311-1315, 2008.
- [6] C. David, *et al.*, "Fabrication of diffraction gratings for hard X-ray phase contrast imaging," *Microelectronic Engineering*, vol. 84, pp. 1172-1177, 2007.
- [7] S. Rutishauser, *et al.*, "Fabrication of two-dimensional hard X-ray diffraction gratings," *Microelectronic Engineering*, vol. 101, pp. 12-16, 2013.
- [8] H. Miao, *et al.*, "Fabrication of 200 nm Period Hard X-ray Phase Gratings," *Nano letters*, vol. 14, pp. 3453-3458, 2014.
- [9] R. K. Heilmann, *et al.*, "Diffraction efficiency of 200-nm-period critical-angle transmission gratings in the soft x-ray and extreme ultraviolet wavelength bands," *Applied optics*, vol. 50, pp. 1364-1373, 2011.
- [10] L. Liu, *et al.*, "Fabrication of X-ray imaging zone plates by e-beam and X-ray lithography," *Microsystem Technologies*, vol. 16, pp. 1315-1321, 2010.
- [11] M. J. Wojcik, *et al.*, "X-ray zone plates with 25 aspect ratio using a 2- μm -thick ultrananocrystalline diamond mold," *Microsystem Technologies*, vol. 20, pp. 2045-2050, 2014.
- [12] C. Chang and A. Sakdinawat, "Ultra-high aspect ratio high-resolution nanofabrication for hard X-ray diffractive optics," *Nature communications*, vol. 5, 2014.
- [13] F. Pfeiffer, *et al.*, "Phase retrieval and differential phase-contrast imaging with low-brilliance X-ray sources," *Nature Physics*, vol. 2, pp. 258-261, 2006.
- [14] H. Miao, *et al.*, "Enhancing tabletop X-ray phase contrast imaging with nano-fabrication," *Scientific Reports*, vol. 5, p. 13581, 2015.
- [15] H. Miao, *et al.*, "A universal moiré effect and application in X-ray phase contrast imaging," *Nature Physics*, doi:10.1038, 2016.
- [16] Y. Chu, *et al.*, "Hard-x-ray microscopy with Fresnel zone plates reaches 40nm Rayleigh resolution," *Applied Physics Letters*, vol. 92, p. 103119, 2008.
- [17] M. Ahn, *et al.*, "Fabrication of 200 nm period blazed transmission gratings on silicon-on-insulator wafers," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 26, pp. 2179-2182, 2008.
- [18] F. Laermer and A. Schilp, "Plasma polymerizing temporary etch stop," ed: Google Patents, 1996.
- [19] S. Tachi, *et al.*, "Low-temperature reactive ion etching and microwave plasma etching of silicon," *Applied Physics Letters*, vol. 52, pp. 616-618, 1988.
- [20] B. Wu, *et al.*, "High aspect ratio silicon etch: A review," *Journal of Applied Physics*, vol. 108, p. 051101, 2010.
- [21] P. Mukherjee, *et al.*, "Plasma etch fabrication of 60: 1 aspect ratio silicon nanogratings with 200 nm pitch," *Journal of Vacuum Science & Technology B*, vol. 28, pp. C6P70-C6P75, 2010.
- [22] Y. Wu, *et al.*, "Cryogenic etching of nano-scale silicon trenches with resist masks," *Microelectronic Engineering*, vol. 88, pp. 2785-2789, 2011.
- [23] R. Dussart, T. Tillocher, P. Lefauchaux and M. Boufnichel, "Plasma cryogenic etching of silicon: from the early days to today's advanced technologies," *Journal of Physics D: Applied Physics*, vol. 47, p. 123001, 2014.
- [24] J. Pereira, *et al.*, "In situ X-ray photoelectron spectroscopy analysis of SiO_xF_y passivation layer obtained in a SF_6/O_2 cryoetching process," *Applied Physics Letters*, vol. 94, p. 071501, 2009.
- [25] T. Tillocher, *et al.*, "Oxidation threshold in silicon etching at cryogenic temperatures," *Journal of Vacuum Science & Technology A*, vol. 24, pp. 1073-1082, 2006.
- [26] A. Kamto, R. Divan, A. V. Sumant and S. L. Burkett, "Cryogenic inductively coupled plasma etching for fabrication of tapered through-silicon vias," *Journal of Vacuum Science & Technology A*, vol. 28, pp. 719-725, 2010.
- [27] L. Sainiemi and S. Franssila, "Mask material effects in cryogenic deep reactive ion etching," *Journal of Vacuum Science & Technology B*, vol. 25, pp. 801-807, 2007.

that the etching profile of the cryogenic process is highly dependent on the feature size. For example, the recipes described here were not suitable for etching of 200 nm pitch gratings[8]. Adding a low frequency bias to the electrode might help reduce the feature size dependence of the process [22], which needs to be further investigated for high aspect ratio structures.

DISCLAIMER

Certain commercial equipment, instruments, or materials are identified in this paper to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

ACKNOWLEDGMENT

The authors would like to thank the National Institute of Standards and Technology, Center for Nanoscale Science and Technology where this research was conducted.

- [28] Z. Liu, Y. Wu, B. Harteneck and D. Olynick, "Super-selective cryogenic etching for sub-10 nm features," *Nanotechnology*, vol. 24, p. 015305, 2013.