Electromagnetic Field Test Structure Chip for Back End of the Line Metrology*

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***Abstract* — A test chip to produce known and controllable gradients of surface potential and magnetic field at the chip surface and suitable for imaging with various types of scanning probe microscopes is presented. The purpose of the test chip is to evaluate various SPMs as metrology tools to image electromagnetic fields within nanoelectronic devices and multi-level interconnects, and as metrology tools to detect defects in back end of line (BEOL) metallization and packaging processes. Four different levels of metal are used to create different buried structures that, when biased, will produce varying electric field and magnetic field distributions. Contacts to the chip are made via wire bonds to a printed circuit board (PCB) that allows programed external biases and ground to be applied to specific metal levels while imaging with a SPM. DC and high frequency COMSOL simulations of the test structures were conducted to determine the expected field distributions. Electric field can be imaged via scanning Kelvin force microscopy (SKFM); magnetic field via scanning magnetic force microscopy (MFM); and the capacitance of buried metal lines via scanning microwave microscopy (SMM). The combination of precisely known structures and accurate simulations will allow the spatial resolution and accuracy of various SPMs sensitive to electric field (potential) or magnetic field to be determined and improved.**

Keywords—BEOL, electromagnetic field measurements, three-dimensional integrated circuits, SKFM, SMM.

I. MOTIVATION

Three dimensional stacked integrated circuits (3D-SICs) have attracted tremendous research interest as a method to add functionality and to scale beyond traditional two-dimensional single chip integration [1]. At the same time, the increasing complexity of back-end of the line (BEOL) multi-level metallization has created a structure like a "giant metallic forest" [2-4]. However, easy to use metrology techniques applicable to these interconnect processes for fault and defect localization, reliability determination, cross-talk and post-fabrication characterization are lacking. Traditional scanning probe microscopy (SPM) imaging techniques can measure surface topography and to a limited extent subsurface structure. In fact, several electrical SPMs, such as scanning microwave microscopy (SMM) and electrostatic force microscopy (EFM) have shown promising subsurface characterization capability on different semiconductor and metallization structures [5-6]. To determine the ultimate resolution, accuracy, and limitations of various modes of these electrically sensitive SPMs to subsurface interconnect structures, we have designed and fabricated a test chip containing devices capable of producing precisely calculable electric and magnetic fields whose intensity varies over sub-micrometer distances.

While detailed reconstruction of the source of electromagnetic fields originating from complex buried bias and current carrying structures may not be practically possible, much useful information may be accessible. Unexpected electrical shorts or opens could alter the pattern of the electromagnetic fields at the surface that can be revealed through subtractive comparison with images of known good circuits. This should allow faults to be spatial located, providing a powerful failure analysis tool. In a similar way, cross-talk faults could be identified from the frequency spectrum of coupled test structures. Few metrology techniques exist for reliability determination, pre-assembly test, and failure analysis for through silicon vias (TSVs) for 3D-ICs. An ability to measure the electromagnetic response of these structures as a function of frequency, prior to assembly and after various thermal, electrical or mechanical stresses has proven useful at the probe station level [7][8]. An SPM based approach would require no dedicated test structures in the semiconductor and could be performed before final packaging. Finally, precision measurements of electric fields and/or magnetic fields on sub-micrometer length scales are possible using a variety of scanned probe techniques. Improving the accuracy and utility of these techniques will require production of precisely constructed and characterized test structures.

II. DESIGN CONSIDERATIONS

Electromagnetic fields exist in three dimensions and their measurement with a point probe allows only a two-dimensional cross-section to be imaged. Furthermore, the probe itself is three-dimensional, so unless highly shielded, all parts of the probe beyond the point contact can contribute to the measurement of the electric or magnetic field. Since SPM probes display a wide range of probe-to-probe variability actual measurements of electric/magnetic fields and gradients could be highly probe shape dependent. To determine the relationship between the measured and real field requires knowing the tip shape, a model that includes the tip shape and reference materials for calibration. Fortunately, electro-

magnetism is well understood and precise calculations of field strength are possible if the shape of the generating conductors and applied voltages/currents are known. Because success requires a precisely known structure to calculate the electromagnetic fields, design of our own test structures was essential.

The chip is designed to be SPM friendly using the TSMC 0.35 micrometer technology available from MOSIS[1]. Bonding pads (big squares on the left side in Fig. 1) are placed on only one side of the chip to avoid the cantilever crashing into wire bonds. To keep a high density of bonding pads, two rows of I/Os were used. The wide (50-μm) metal bus stripes minimize the potential drop as a distance from the pads and keeps the fine features working under nearly the same bias. The structure has four metallization levels, which are noted as M1 to M4 from deepest to surface. The pads of the chip are wire bonded to a custom printed circuit board (PCB) which in turn is connected to a miniature connector and cable, allowing programmed external biases to be applied to different features to simulate a device under test (DUT). Hence, active electric and magnetic fields can be produced on the chip surface while imaging in an SPM.

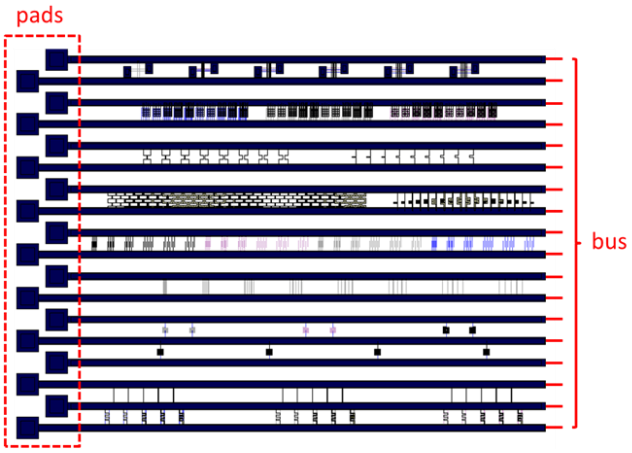


Fig. 1 Overview of part of the main structure of the test chip.

III. Test Structures

A. *Single metal-level magnetic field test structure*

A variety of simple test structures were fabricated. These should produce electric and magnetic fields that have a high spatial gradient within the typical field of view of an SPM image and that are also easy to simulate with off the shelf software. A few representative structures are shown in Figs. 2 and 3 below. Single pairs of parallel metal lines buried at each of the different levels within the intermetallic oxide are included to generate a simple magnetic or potential field distribution at the surface of the insulator. Geometries where parallel lines have current flowing in either the opposite (Fig. 2a) or the same directions (Fig. 2b) are included. Since all parameters are known (metal width and thickness, cover dielectric thickness and dielectric constant, applied currents) magnetic field can be calculated precisely as a function of tip position. The combination of a precisely known test structure, simulation results, and precision MFM measurements will allow evaluation of the accuracy and spatial resolution of magnetic field imaging techniques.

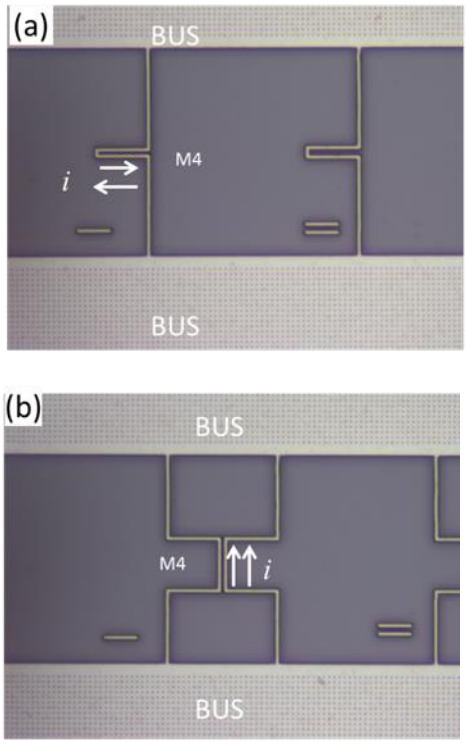
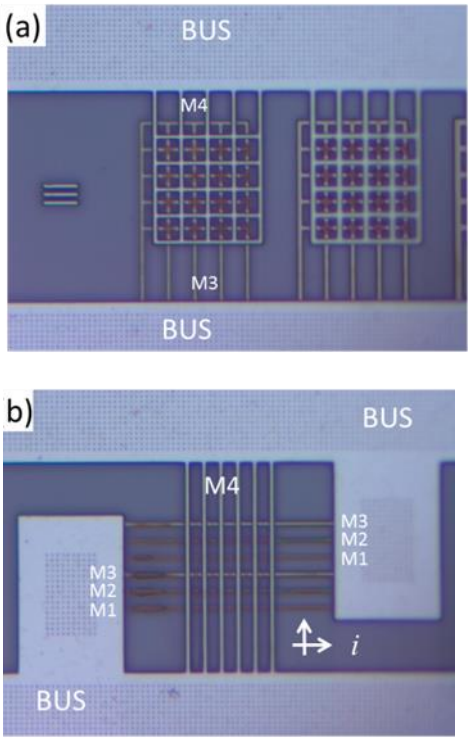


Fig. 2 Parallel wires at the same level layout for (a) opposed current flow and (b) parallel current flow.



[1] Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment used are necessarily the best available for the purpose.

Fig. 3 Perpendicular wires at different layers for (a) potential imaging and (b) magnetic field and cross talk measurements.

B. *Multiple metal-level potential field test structures*

In Fig. 3a, overlapping "waffle" structures at different depths can be biased at different potentials allowing complex surface potentials to be generated at the surface of the dielectric. Structures with a variety of metal line thicknesses, spacings and depths were fabricated. The surface potential information can be imaged by scanning Kelvin force microscopy (SKFM). In Fig. 3b, the metal lines are perpendicular to others at different levels, they are parallel at the same level. As the upper and lower stripes can be biased separately, the cross talk of multi-level lines can be simulated as a function of frequency. In addition, some parts of lines that are not crossed can be used as a reference. As all the metallization levels can be found in Fig. 3b, this structure can also be used for determining electric or magnetic field image resolution as a function of the subsurface depth of the source line.

IV. COMSOL SIMULATIONS

Here we show a COMSOL simulation of the surface potential from one test structure and how it should interact with the SKFM. The overall geometry modeled in COMSOL can be seen in Fig. 4a, while the details of the three-line test structure are shown in Fig. 4b. A photo of the relevant part of the test chip is found in the inset of Fig.4b. Figs. 4c and 4d show the surface potential distribution while the tip is "scanning" along the "observation line" in Fig. 4b. Both Figs. 4c and 4d simulate a line separation of 1.2 μm while the depth of the line varies from 0 μm to 4.8 μm. The outer lines are biased at +1V. The center line is grounded (0 V) in Fig. 4c while it is biased -1 V in (Fig.4d. Results show that the reversed bias (-1 V) center line gives better resolution at the same depth than the grounded center line case. For example, at the 3.2 μm depth, the reversed biased case shows a 200 mV potential variation, while the grounded case only provides a 2.5 mV potential difference

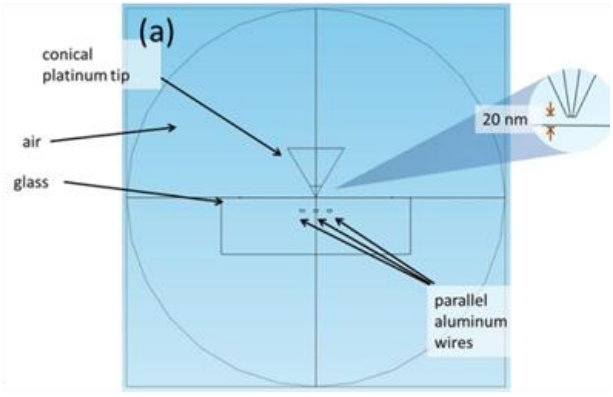


Fig. 4(a) Modeled tip and sample geometry.

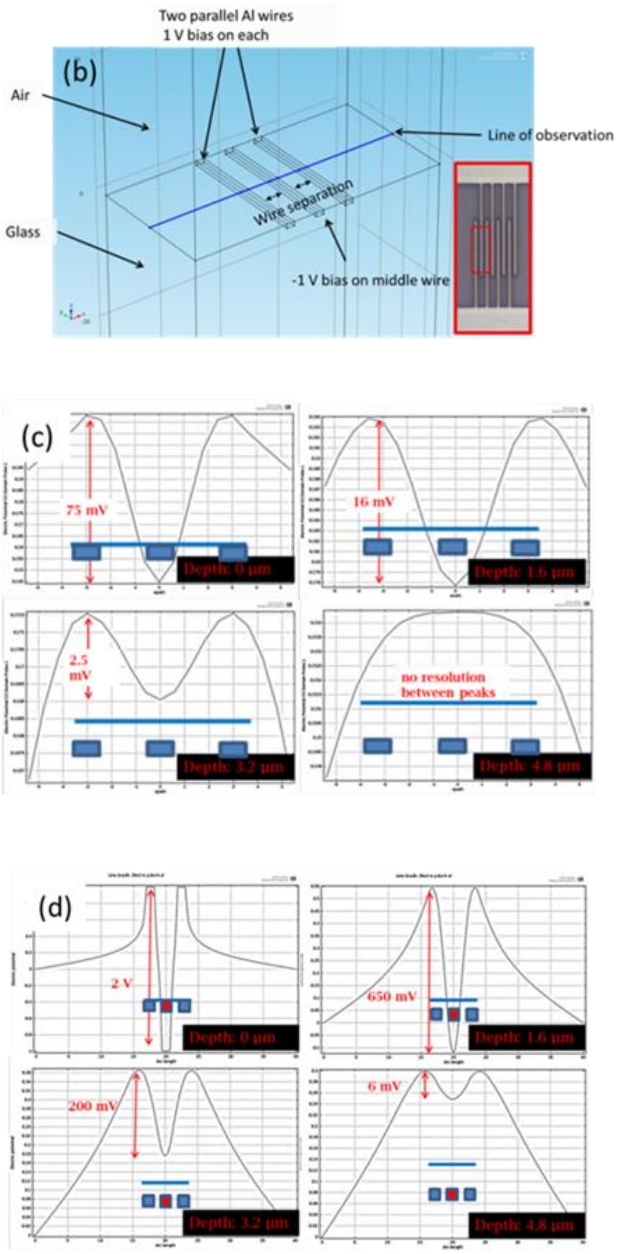


Fig. 4 (b)Measurement geometry and photo insert of relevant test structure, (c) Surface potential simulation along on the "observation" line at various depths with middle wire grounded, (d) simulation with middle wire biased at -1V

V. RESULTS

A. *Electric Field Imaging*

Here we show the surface potential distribution on an area that has several parallel lines buried beneath the silicon dioxide. Fig. 5(a) shows the AFM image of this area. Due to the manufacture process, a 5 nm step can be found between the metal line buried areas and non-metal line buried areas. In (b), no obvious surface potential contrast can be detected. This confirms that all the metal lines are buried in SiO_2. Otherwise, huge potential contrast would be expected due to the significantly electric properties difference between Al and SiO_2. In (c), the metal lines are alternatively biased with 1 V

and -1 V. The additional electric fields vary the surface potential, thus the contrastsshown. In (d), the averaged line profiles are shown, combining the metal line location and the potential variations. Detailed discussion will be made during the conference.

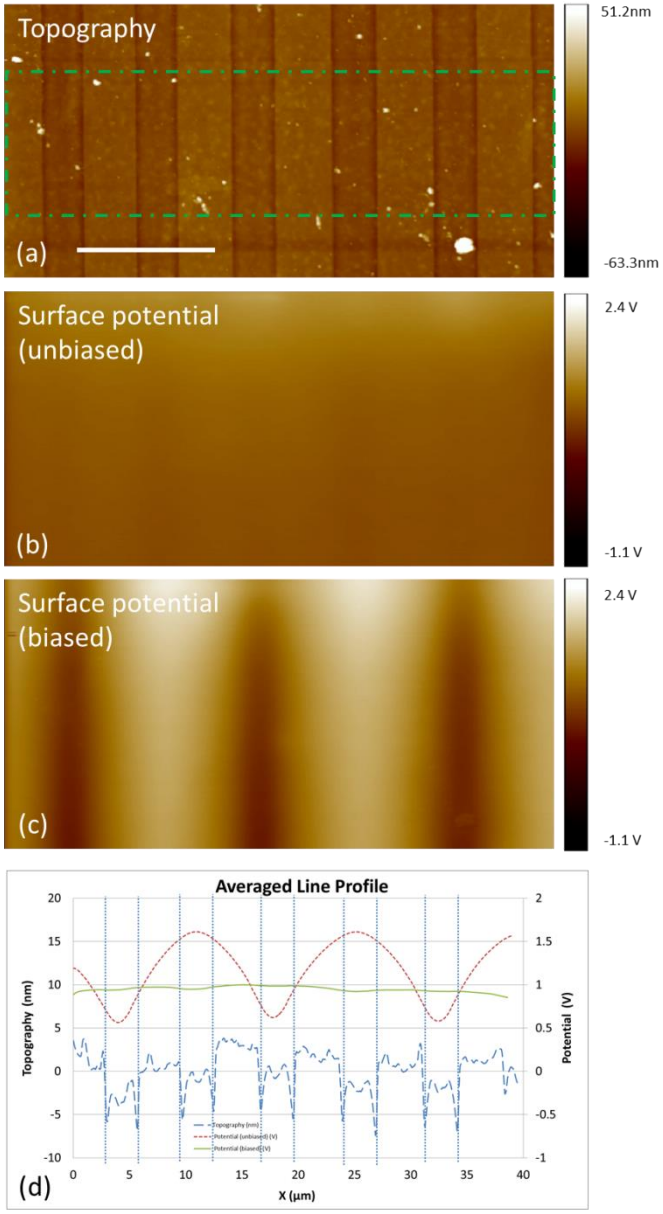


Figure 5 SKFM results on subsurface metal lines (M2) that are alternatively biased. (a) Topography of the scan area. (b) Surface potential distribution with NO bias applied on all lines. (c)Surface potential distribution with alternatively biased with 1 V and -1 V. (d) Averaged line profiles on areas marked in (a). The white short line in (a) is the scale bar for 10 μm.

B. Subsurface Imaging with Scanning Microwave Microscopy

A new implementation of scanning microwave microscopy (SMM) measures the magnitude and phase of the S11 reflected high frequency signal (incident signal minus signal transmitted through the tip into the sample) through use of a vector network analyzer (VNA). Shielding and coupling of the tip to the sample is essential to functional SMM. The input to the VNA is a transmission line terminated by the tip-to-sample impedance. The terminal impedance will be some combination of frequency dependent resistances and capacitances. With additional electronics the SMM can also measure the dC/dV signal between the tip and sample, allowing it to function in SCM mode for semiconductor dopant profiling. Additional details of the mechanism of SMM are available elsewhere [9][10]. Through the capacitive coupling of the tip to conductive structures in an insulating matrix it should be possible to measure the dimensions and integrity of metallization within low-k dielectrics for BEOL metrology.

A simple model of the SMM, considers the cable connecting the tip and VNA as a transmission line with the tip and the underlying structure of the sample as the terminal impedance. A transmission line terminated by its characteristic impedance (50 Ω) will transmit the entire incoming signal (no reflection); while an open will reflect all the signal in-phase, and a short will reflect all the signal 180^{o} out of phase. Simply, an insulating substrate would be seen as a high terminal resistance, while a metallic substrate would be seen as a low resistance. Buried metallic structures, whether grounded or floating will contribute a capacitive component. Our buried test structures will produce a complex set of reflection parameters as a function of frequency, but we expect our buried metallic structures to increase the capacitance of the transmission line termination and thus be detectable in the phase of the signal reflected back to the VNA (relative to regions with no buried metal). In contrast to SKFM, no bias is necessary to image buried metal lines with SMM. In Fig. 6, we plot the phase of the reflected signal as the tip is scanned across buried lines at a depth of a) ~1 μm and b) ~2 μm, confirming the predicted behavior.

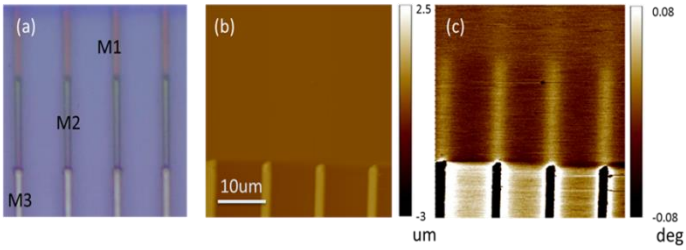


Figure 6 a) Optical microscopy image; metal M3 is on the surface, while M2 is buried beneath ~ 1 μm of low-k dielectric and M1 is buried beneath ~ 2 μm of low-k dielectric; b) AFM topography image shows that M2 and M1 are totally buried within oxide and that there is no topography change above them. (c) VNA phase images shows contrast from both the buried lines.

VI. Summary and Outlook

A SPM-friendly test chip for generating electromagnetic field gradients has been designed and fabricated. The test chip can be mounted on a customized PCB and biased to produce electromagnetic fields while being imaged by electrical scanning probe microscopes. COMSOL simulations of the electric fields, magnetic fields, and high frequency transmission/reflection characteristics of the various test structures have been developed. The SPM tip shape is

included in the simulations allowing the actual signal measured by the SPM to be modeled. Detection of biased buried structure with KFM expands this essential nano-characterization tool from material surface towards subsurface. Detailed electrical characterization of these test structures is underway which should lead to validation of the model of the various SPMs and quantification of the accuracy of electric and magnetic field gradient measurements with electrical SPMs. Ultimately, revised test structures will be produced, with associated models and procedures for calibration of electrical and magnetic field measurement on the nanoscale.

VII. Acknowledgments

Emily Hitz and Jonathon Michelson participated in this project supported by the National Science Foundation under Agreement No. EEC-1156409: "REU Site: SURFing Cross-Disciplinary Electronics Research at the National Institute of Standards and Technology."

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