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Field effects of current crowding in metal-MoS_2 contacts

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Gate assisted contact-end Kelvin test structures and gate assisted four-probe structures have been designed and fabricated to measure the field effects of current crowding at the source/drain contacts of top-gate MoS_2 field effect transistors. The transistors exhibited n-type transistor characteristics. The source/drain contact resistance was measured by using both gate-assisted Kelvin and gate-assisted four-probe structures. The values of contact resistance measured by these two test structures are significantly different. The contact-front contact resistance obtained from the four-probe structure is strongly influenced by field effects on current crowding, while the contact-end resistance obtained from the Kelvin test structure is not. The metal-MoS_2 contact current transfer length, L_T, can be determined from the comparison between these two measurements. L_T was observed to increase linearly with increasing gate voltage. This work indicates that the contact characteristics can be more precisely measured when both gate-assisted test structures are used. © *2016 AIP Publishing LLC*.
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Recently, transition metal dichalcogenides (TMDs), such as MoS_2 and WSe_2, have attracted intensive attention for applications in future electronics and photonics.[1,2] Monolayer and few-layer MoS_2 can be considered as two-dimensional (2D) semiconductors. They have an energy bandgap (E_g) ranging from 1.2 eV to 1.8 eV, which depends on the thickness of MoS_2.[3–5] In particular, monolayer MoS_2 has a direct bandgap ($E_g = 1.8$ eV) which leads to extraordinary electrical and optoelectronic properties.[6–12] For the consideration of short channel effects in metal-oxide-semiconductor field effect transistors (MOSFETs), the monolayer MoS_2, which has an intrinsic atomically thin body and well-passivated surfaces, represents the ultimate small medium for device scaling.[13] In addition, the transparent feature and robust lattice structure in 2D MoS_2 are very attractive for flexible electronics.[14–16]

MOSFETs are the basic building blocks for electronic circuits. High-performance MoS_2 FETs are considered a promising technological thrust for next-generation electronics.[1,2] Because the performance of 2D MoS_2 FETs is significantly influenced by the properties of source/drain (S/D) contacts, it is critical to fully understand and properly engineer contacts between metals and MoS_2. A variety of contact materials and structures have been proposed and studied to achieve effective Ohmic contacts on MoS_2.[16–27] And recently, the current distribution under the metal contacts has also been considered.[28,29] These results are mostly based on bottom-gated FETs where the channel current was not effectively tuned by the gate. This is not the case in top-gate MoS_2 FETs. A statistical study of MoS_2 transistors[30] indicated that top-gated FETs have a larger contact resistance as compared to back-gated ones. Because, unlike back-gated devices, the carrier density in MoS_2 under source/drain metal contacts will not change at higher positive gate bias in top-gated transistors. Our previous work has shown that using the gate-assisted test structures is an excellent approach to measure properties of the metal contacts to low-dimensional materials.[31] Here, we present a study on current crowding in metal-MoS_2 contacts determined by using both gate-assisted Kelvin structures and four-probe structures where the channel current is effectively tuned by a top gate.

We fabricated Ag-contacted bilayer MoS_2 transistors with Au/Ti/Al_2O_3 top gates on SiO_2/Si substrate. Our devices show good n-type current-voltage (I-V) characteristics. Then gate assisted Kelvin structure and four-probe method were used to analyze the contacts. The contact resistance extracted from both methods is significantly different because the position where the voltage is sampled is different. By comparing the contact resistance extracted from both methods, we found that the current transfer length (L_T) of Ag-contact on MoS_2 transistors ranged from 114.3 nm to 128.5 nm, which increased with increasing gate voltage. The channel sheet resistance, which is measured by the four-probe method, is larger than the contact resistance. This indicates that the MoS_2 transistors are channel-dominant. Our results have shown that the gate affects not only the channel resistance but also the current crowding at the contacts.

In this work, the MoS_2 was grown on a 285 nm SiO_2/Si substrate via chemical vapour deposition (CVD). During the CVD of MoS_2, MoO_3 and sulfur are used as the precursors. In detail, an alumina crucible with 5 mg MoO_3 powder was placed in the center a tube furnace. An alumina crucible with abundant amount of sulfur (≈1.5 g) was placed at the

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entrance location of the furnace. The substrate was placed in the downstream 2 cm away from the MoO_3 crucible. During the growth, the CVD furnace was maintained at 800 Torr (about 1.07×10^5 Pa) with 100 sccm ambient Ar as carrier gas. Before heating, the whole system was pumped to 200 mTorr and then flushed with Ar for 3 times. A stable pressure of 800 Torr was achieved before the heating processes. The heating processes included a 30-min ramp up to 850 °C and a hold at 850 °C for 30 min. After heating, the furnace was naturally cooled to room temperature. After growth, MoS_2 flakes are found to spread over the SiO_2/Si substrates. As shown in the optical image in Fig. 1(a), the MoS_2 flakes are typically triangular or hexagonal in shape. Fig. 1(b) shows a Raman map of the same location in Fig. 1(a). Plotted here is the integrated intensity from 340 cm^{-1} to 430 cm^{-1} including both the E_{2g} in plane and the A_{1g} out-of-plane modes. The optical contrast and Raman map suggest that the MoS_2 flake thickness is quite uniform. Raman spectrum of a representative point on the uniform MoS_2 flakes (Fig. 1(c)) shows that the separation between the two major peaks is 21 cm^{-1}, indicating these are two-layer MoS_2 flakes.[32]

To fabricate MoS_2 MOSFETs, first, the MoS_2 flakes on the substrate were located with an optical microscope. Conventional lithography processes were then applied to define the device structures. 5 nm Ag/50 nm Au was deposited on MoS_2 as the S/D contacts. Ag was chosen because it has been reported for forming a good contact on WSe_2,[33] which is a similar material to MoS_2. And our previous work shows that Ag forms a smooth and solid film on MoS_2 which makes the carrier transport efficiently across the contacts.[34] Five parallel metal contacts were deposited on a MoS_2 triangle flake to form the FETs, gate assisted Kelvin test structures and four-probe structures with the same contacts. Then, a rectangular MoS_2 channel was defined by O_2 plasma etching. To integrate the gate dielectric, 1 nm Al was deposited on MoS_2 and then oxidized in air as a seeding layer before the atomic layer deposition (ALD) of 30 nm Al_2O_3. This will promote gate dielectric quality.[35] The ALD of Al_2O_3 was performed at 300 °C with trimethylaluminum (TMA) and H_2O as precursors. Finally, 5 nm Ti/50 nm Au was deposited as top gate. The top gate covers the whole structure including the channels and five S/D contacts. Therefore, all four channels share a common gate. A schematic of device structure and scanning electron microscopic image of two adjacent channels and three contacts are shown in Figs. 2(a) and 2(b), respectively. The channel length (L_G) and width (W) are 370 nm and 4 μm, respectively. And the contact length (L_C) is 1.09 μm.

The devices were then measured by a semiconductor parameter analyser (Hewlett-Packard® 4156) in a probe station (Cascade® summit semi-automated probe station) at room temperature. Figs. 2(c) and 2(d) show the I-V characteristics of a typical MoS_2 FET with details mentioned above. The channel current is normalized to current per one μm in channel width. The transistor exhibits strong n-type device characteristics which is similar to those reported by other groups.[9,15–17] The small hysteresis in I_D–V_G measurement indicates a good quality of Al_2O_3 which is used as gate dielectric. Also, the On-state current of these FETs is quite large compared to the published results.[9,15–17,36,37] The threshold voltage and field effect mobility are extracted from the linear fitting of I_D–V_G curve measured at $V_D = 50$ mV. The threshold voltage is −10.2 V. At a small V_{DS}, the field effect mobility of the transistor can be extracted from the linear mode I_D, expressed as

$$\mu_{\text{eff}} = \frac{L}{W}\frac{1}{V_{DS}}\frac{1}{C_{ox}}\frac{\partial I_D}{\partial V_{GS}}. \quad (1)$$

Here, V_{GS} should be large enough and V_{DS} should be small to keep the transistor working in linear mode. The value of the field effect mobility of our device is 7.8 $cm^2\ V^{-1}\ s^{-1}$. This value is close to some recent publications using similar device structures.[37,38] The linear relationship between drain current (I_D) and drain voltage (V_D) at low voltage indicates good S/D contacts.

In order to evaluate the metal contacts on MoS_2, contact resistance measurements using both gate assisted Kelvin test structure and gated assisted four-probe test structure were performed on these MoS_2 FETs. Figs. 3(a)–3(c) show the contact resistance measured by the gate assisted Kelvin test structure. The measurement set-up is illustrated in Fig. 3(a). In the

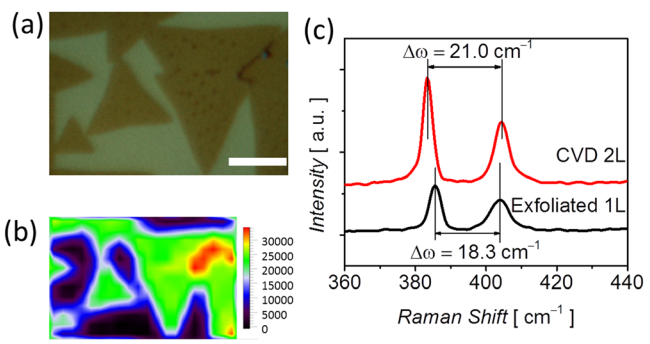

FIG. 1. MoS_2 crystal characterization: (a) Optical image of typical MoS_2 flakes grown on SiO_2/Si substrate. The scale bar is 5 μm. (b) Raman mapping of the MoS_2 flakes in (a). The intensity in the image is the integrated signal intensity from 340 cm^{-1} to 430 cm^{-1}. (c) Raman spectrum of a representative point on MoS_2 flakes, compared to exfoliated 1L MoS_2.

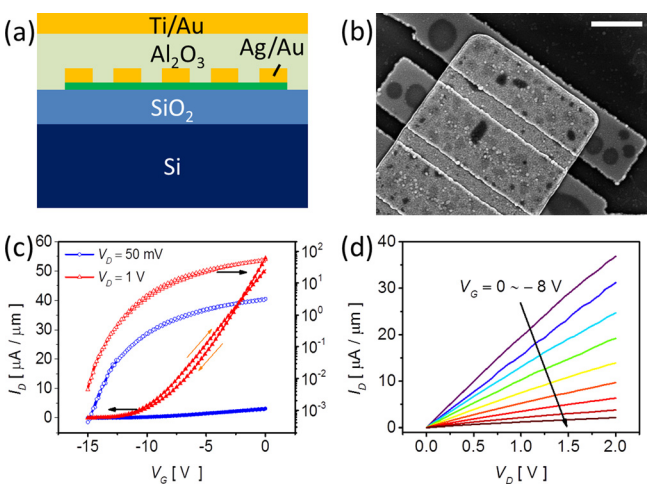

FIG. 2. Device structure and I-V characterization of a representative MoS_2 FET: (a) Schematics of MoS_2 FETs. (b) SEM image of a MoS_2 transistor. Scale bar in this image is 1 μm. (c) I_D-V_G, and (d) I_D-V_D characteristic. The orange arrows indicates the voltage sweeping direction during the measurement and the black arrows pointing to the corresponding scale labels for the data shown in linear and log scale.

Kelvin test structure, I_D is driven through the middle contact by the MoS_2 FET on the left. Non-local voltage (V_{23}) was measured between the middle and right electrodes. Since a common gate is applied to the whole test structure, both channels are biased to the same conditions. Because there is no current flowing through the right channel and contact on the right, V_{23} is measured as the voltage drop at the end edge of MoS_2 underneath the middle contact (source of the FET on the left). As shown in Fig. 3(b), the curves of V_{23} versus I_D at different gate voltage are quite linear, indicating an Ohmic contact. The overlap of the V_{23} curve at different V_G shows that the contact resistance obtained by Kelvin test method ($R_{C\text{-}K}$) is not affected by V_G. Fig. 3(c) shows the variation of $R_{C\text{-}K}$ which is the slope extracted from the linear fitting of V_{23}–I_D curves. The value of $R_{C\text{-}K}$ is only a little more than 20 Ω, which is much lower than the contact resistance extracted from other methods in previous publications.[22,28,29]

Then, a gate assisted four-probe measurement was carried out to obtain the contact resistance and further understand the contact behaviour. The measurement set-up is shown in Fig. 3(d). A voltage source was connected to the S/D contacts at the ends to drive the current through the channel under the gate voltage varying from −5 V to 0 V. The I_D and the voltage difference between the second and third contacts (V_{23}) are measured at the same time. Based on previous publications, the transfer length (L_T) is typically in hundreds of nm scale.[28,29] The contact length we used in the two middle contacts is comparably large. So, the voltage distribution across the two middle contacts must be accounted for.[39] The voltage drop on the two middle contacts would contribute a resistance of R_M to the total resistance we measured. So

$$R_{14} = 2R_C + 2R_M + 3R_{ch}, \tag{2}$$

$$R_{23} = R_M + R_{ch}. \tag{3}$$

R_{14} and R_{23} can be extracted by the linear fitting of V_D and V_{23} vs. I_D. R_C is the contact resistance. R_M can be viewed as parallel resistance of $2R_C$ and the resistance of MoS_2 under the contact. Theoretically, the sheet resistance of MoS_2 under the contacts should not change under different gate bias, because the contact metal shields it from the top gate.[30] But, as we will discuss later, it may not be the reality. To simplify the calculation, we assumed that the sheet resistance of MoS_2 under the contacts is the same with the one in the channel. So R_M and the channel resistance (R_{ch}) can be estimated

$$R_M = \frac{2R_C \cdot \frac{L_C}{W} R_{sh}}{2R_C + \frac{L_C}{W} R_{sh}}, \tag{4}$$

$$R_{ch} = \frac{L_G}{W} R_{sh}. \tag{5}$$

Combining Eqs. (2)–(5), we can solve R_C and R_{sh}

$$R_C = \frac{\left(1 - \frac{L_C}{L_G}\right)(R_{14} - 3R_{23}) + \sqrt{\left(1 - \frac{L_C}{L_G}\right)^2 (R_{14} - 3R_{23})^2 + \frac{4L_C}{L_G}(R_{14} - 3R_{23})(R_{14} - 2R_{23})}}{4}, \tag{6}$$

$$R_{sh} = \frac{W}{L_G}\left[(R_{14} - 2R_{23}) - \frac{\left(1 - \frac{L_C}{L_G}\right)(R_{14} - 3R_{23}) + \sqrt{\left(1 - \frac{L_C}{L_G}\right)^2 (R_{14} - 3R_{23})^2 + \frac{4L_C}{L_G}(R_{14} - 3R_{23})(R_{14} - 2R_{23})}}{2}\right]. \tag{7}$$

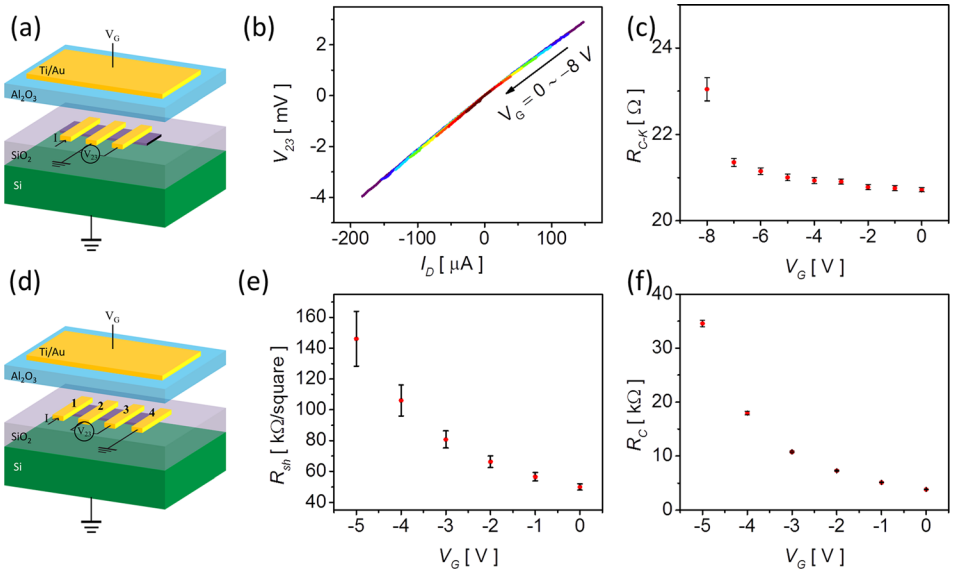

FIG. 3. Gate assisted contact measurement: (a) Set-up of gate assisted Kelvin measurement; (b) V_{23}-I_D measured at different V_G in Kelvin test structure; (c) $R_{C\text{-}K}$ extracted from the linear fitting of V_{23} and I_D at different V_G. (d) Set-up of gate assisted four-probe measurement; (e) Channel sheet resistance at different V_G measured by four-probe test structure; (f) Contact resistance (R_C) extracted from four-probe measurement.

Figs. 3(e) and 3(f) show the channel sheet resistance and contact resistance varying with gate voltage, respectively. The channel conductance is effectively tuned by the gate (see Fig. 3(e)) as expected. It is quite interesting that the contact resistance is also effectively tuned by the gate (see Fig. 3(f)). Compared to the channel resistance, the contact resistance is higher in these transistors, indicating that these are contact-dominated MoS_2 transistors.

It should be noted that R_C is much larger than $R_{C\text{-}K}$ and strongly depends on the gate voltage. This provides clear evidence of current crowding at metal-MoS_2 contacts. According to transmission line model (TLM),[40–43] illustrated in Fig. 4, the current transport in a contact is concentrated at the front of the contact. The voltage at the front of the contact is much higher than the voltage at the end of the contact. The voltage distribution in MoS_2 under a metal contact can be expressed as[40–43]

$$V(x) = \frac{\sqrt{\rho_C R_{sh}}\cosh\left((L_C - x)/L_T\right)}{W\sinh(L_C/L_T)} I_D, \tag{8}$$

where ρ_C is contact resistivity, x is the position on MoS_2 where the voltage is samples, L_C is the contact length (1.09 μm in our devices), R_{sh} is the sheet resistance of MoS_2 under contact, and L_T is current transfer length of MoS_2. It is the distance which the current would penetrate into the MoS_2 under the metal contact, i.e., the length of MoS_2 used as effective contact. In a conventional bulk FET, L_T is defined as

$$L_T = \sqrt{\rho_C / R_{sh}}. \tag{9}$$

Here we still use Eq. (8) to express the voltage distribution under the contact in our devices. In the Kelvin test structure, the non-local voltage at the middle contact (V_{23}) is measured at the end of the contact (i.e., $x = L_C$), so

$$R_{C-K} = \frac{V(L_C)}{I_D} = \frac{\sqrt{\rho_C R_{sh}}}{W\sinh(L_C/L_T)}. \tag{10}$$

However, in the four-probe method, the voltage on the contact is measured at the front of the contact (i.e., $x = 0$), so

$$R_C = \frac{V(0)}{I_D} = \frac{\sqrt{\rho_C R_{sh}}\cosh(L_C/L_T)}{W\sinh(L_C/L_T)}. \tag{11}$$

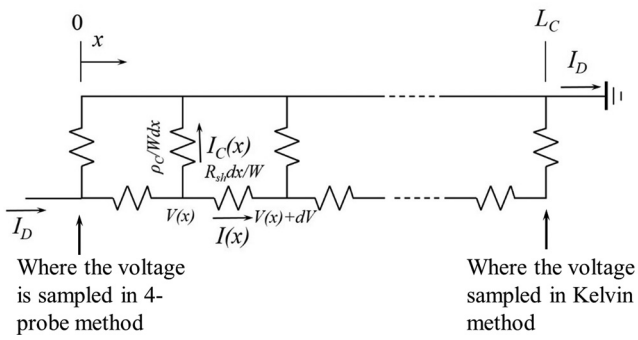

FIG. 4. TLM for contact resistance. The positions where the voltage is sampled in Kelvin method and four-probe measurement are pointed.

It is clear that the ratio of R_C to $R_{C\text{-}K}$ can be expressed as

$$\frac{R_C}{R_{C-K}} = \cosh(L_C/L_T). \tag{12}$$

Therefore, the ratio of R_C over $R_{C\text{-}K}$ is highly dependent on the ratio of the contact length over transfer length. Since R_C is much larger than $R_{C\text{-}K}$ in our devices, the L_C is much larger than L_T. The current is concentrated at the front part of the contact. As shown in Fig. 5(a), the L_T of the MoS_2 devices can be extracted from the ratio of R_C over $R_{C\text{-}K}$. The L_T is weakly affected by the gate bias: it increases from 114.3 nm when V_G equals to −5 V to 128.5 nm for V_G equals to 0 V. These values are slightly larger than those in the previous work which also shows L_T increased with increasing gate voltage in bottom gated MoS_2 transistors.[28]

In this work, L_C is much larger than L_T. So, R_C can be approximately expressed as

$$R_C \approx \frac{\rho_C}{WL_T}. \tag{13}$$

The contact resistivity ρ_C can be extracted from Eq. (13). As plotted in Fig. 5(b), ρ_C sharply decreases with increasing gate voltage. This means that the contact resistivity of the S/D contacts in a MoS_2 transistor is strongly dependent on gate voltage. So, the contacts also contribute to the switching of these MoS_2 transistors. It may indicate that, in addition to minimizing contact resistance, the gate voltage can also be used to modulate the barrier so that the device performance can be optimized where a barrier at the metal contact is preferred, such as in solar cells and photovoltaic devices. Unlike bulk devices, the band bending in 2D MoS_2 transistors takes place along the current transport direction instead of the vertical direction.[22] Even though the top-gate would not affect the charge density under the contact,[30] it affects the barrier height and width along the edge of the contacts. As the gate bias gets higher, the band in the channel bends downward. However, the energy band of MoS_2 under the contact would not change because it is shielded from the top gate by the metal contact. The barrier between the MoS_2 under contact and in the channel gets lower and narrower. As a result, the contact resistivity gets lower. Meanwhile, the current transfer length increases a little from 114.3 nm to 128.5 nm. It may be a result of the limited density of state in 2D MoS_2. At higher gate bias, the current density is higher. The limited density of state in 2D MoS_2 requires a larger area for the carrier injection. Correspondingly, the transfer length increases. In total, the lower contact resistivity and larger transfer length result in a lower contact resistance at higher gate bias.

In summary, n-type MoS_2 FETs were fabricated with a conventional lithography process. All MoS_2 transistors exhibited good n-type I-V characteristics. The contacts of the MoS_2 transistors were analyzed with gate assisted contact measurement structures including Kelvin test structure and four-probe test structure. Contact resistance is smaller than the channel resistance, indicating that these MoS_2 transistors are channel-dominant devices. The values of contact resistance extracted from Kelvin test structure and four-probe test structure are significantly different. According to TLM, this difference is due to the current crowding and the different

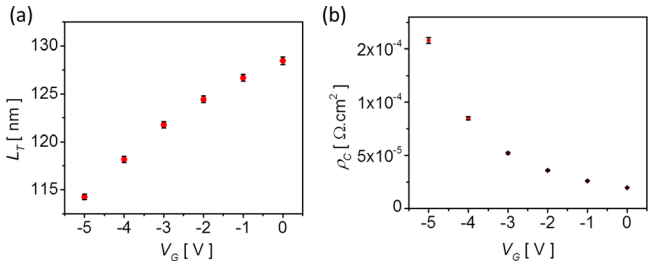

FIG. 5. (a) Transfer length and contact resistivity of MoS_2 transistors: (a) current transfer length and (b) contact resistivity at different V_G.

voltage sampling positions in each method. The current transfer length, which is extracted based on the ratio of the contact-front and contact-end resistance obtained by these two methods, increases with increasing the gate voltage. Our result clearly shows that the gate effectively modifies the contact resistivity through the current crowding, which should be taken into consideration during the design and fabrication of 2D semiconductor devices and circuits.

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[1]S. Z. Butler, S. M. Hollen, L. Cao, Yi. Cui, J. A. Gupta, H. R. Gutiérrez, T. F. Heinz, S. S. Hong, J. Huang, A. F. Ismach, E. Johnston-Halperin, M. Kuno, V. V. Plashnitsa, R. D. Robinson, R. S. Ruoff, S. Salahuddin, J. Shan, Li. Shi, M. G. Spencer, M. Terrones, W. Windl, and J. E. Goldberger, ACS Nano **7**(4), 2898 (2013).
[2]D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, and M. C. Hersam, ACS Nano **8**(2), 1102 (2014).
[3]S. Lebègue and O. Eriksson, Phys. Rev. B **79**(11), 115409 (2009).
[4]A. Kuc, N. Zibouche, and T. Heine, Phys. Rev. B **83**(24), 245213 (2011).
[5]A. Splendiani, L. Sun, Y. Zhang, T. Li, J. Kim, C.-Y. Chim, G. Galli, and F. Wang, Nano Lett. **10**(4), 1271 (2010).
[6]R. S. Sundaram, M. Engel, A. Lombardo, R. Krupke, A. C. Ferrari, Ph. Avouris, and M. Steiner, Nano Lett. **13**, 1416 (2013).
[7]Z. Y. Yin, H. Li, L. Jiang, Y. M. Shi, Y. H. Sun, G. Lu, Q. Zhang, X. D. Chen, and H. Zhang, ACS Nano **6**(1), 74 (2012).
[8]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. **6**(3), 147 (2011).
[9]T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, and A. Javey, ACS Nano **8**(6), 6259 (2014).
[10]H. Li, Z. Yin, Q. He, H. Li, X. Huang, G. Lu, D. W. H. Fam, A. Iing, Y. Tok, Q. Zhang, and H. Zhang, Small **8**(1), 63 (2012).
[11]Lu. Wang, Ye. Wang, J. It. Wong, T. Palacios, J. Kong, and H. Y. Yang, Small **10**(6), 1101 (2014).
[12]Tu. Hong, B. Chamlagain, S. Hu, S. M. Weiss, Z. Zhou, and Ya.-Q. Xu, ACS Nano **9**(5), 5357 (2015).
[13]W.-Y. Lu and Y. Taur, IEEE Trans. Electron Devices **53**(5), 1137 (2006).
[14]G.-H. Lee, Y.-J. Yu, Xu. Cui, N. Petrone, C.-Ho. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, ACS Nano **7**(9), 7931 (2013).
[15]H.-Yu. Chang, S. Yang, J. Lee, Li. Tao, W.-S. Hwang, D. Jena, N. Lu, and D. Akinwande, ACS Nano **7**(6), 5446 (2013).
[16]J. Yoon, W. Park, G.-Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W.-K. Hong, B. H. Lee, and H. C. Ko, Small **9**(19), 3295 (2013).
[17]S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, Nano Lett. **13**(1), 100 (2013).
[18]C. Gong, L. Colombo, R. M. Wallace, and K. Cho, Nano Lett. **14**(4), 1714 (2014).
[19]S. McDonnell, R. Addou, C. Buie, R. M. Wallace, and C. L. Hinkle, ACS Nano **8**(3), 2880 (2014).
[20]S. Chuang, C. Battaglia, A. Azcatl, S. McDonnell, J. S. Kang, X. Yin, M. Tosun, R. Kapadia, H. Fang, R. M. Wallace, and A. Javey, Nano Lett. **14**(3), 1337 (2014).
[21]Y. Du, L. Yang, J. Zhang, H. Liu, K. Majumdar, P. D. Kirsch, and P. D. Ye, IEEE Electron Device Lett. **35**(5), 599 (2014).
[22]J. Kang, W. Liu, and K. Banerjee, Appl. Phys. Lett. **104**(9), 093106 (2014).
[23]J. Kang, W. Liu, D. Sarkar, D. Jena, and K. Banerjee, Phys. Rev. X **4**(3), 031005 (2014).
[24]M. M. Perera, M.-W. Lin, H.-J. Chuang, B. P. Chamlagain, C. Wang, X. Tan, M. M.-C. Cheng, D. Tománek, and Z. Zhou, ACS Nano **7**(5), 4449 (2013).
[25]R. Kappera, D. Voiry, S. E. Yalcin, B. Branch, G. Gupta, A. D. Mohite, and M. Chhowalla, Nat. Mater. **13**(12), 1128 (2014).
[26]Xu. Cui, G.-H. Lee, Y. D. Kim, G. Arefe, P. Y. Huang, C.-Ho. Lee, D. A. Chenet, X. Zhang, L. Wang, F. Ye, F. Pizzocchero, B. S. Jessen, K. Watanabe, T. Taniguchi, D. A. Muller, T. Low, P. Kim, and J. Hone, Nat. Nano **10**(6), 534 (2015).
[27]Y. Liu, H. Wu, H.-C. Cheng, S. Yang, E. Zhu, Q. He, M. Ding, D. Li, J. Guo, N. O. Weiss, Yu. Huang, and X. Duan, Nano Lett. **15**(5), 3030 (2015).
[28]Y. Guo, Y. Han, J. Li, An. Xiang, X. Wei, S. Gao, and Q. Chen, ACS Nano **8**(8), 7771 (2014).
[29]H. Liu, M. Si, Y. Deng, A. T. Neal, Y. Du, S. Najmaei, P. M. Ajayan, J. Lou, and P. D. Ye, ACS Nano **8**(1), 1031 (2014).
[30]H. Liu, M. Si, S. Najmaei, A. T. Neal, Y. Du, P. M. Ajayan, J. Lou, and P. D. Ye, Nano Lett. **13**(6), 2640 (2013).
[31]H. Yuan, A. Badwan, C. A. Richter, H. Zhu, O. Kirillov, D. E. Ioannou, and Q. Li, Appl. Phys. Lett. **105**(13), 133513 (2014).
[32]H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, and D. Baillargeat, Adv. Funct. Mater. **22**(7), 1385 (2012).
[33]W. Liu, J. Kang, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, Nano Lett. **13**(5), 1983 (2013).
[34]H. Yuan, G. Cheng, L. You, H. Li, H. Zhu, W. Li, J. J. Kopanski, Y. S. Obeng, A. R. H. Walker, D. J. Gundlach, C. A. Richter, D. E. Ioannou, and Q. Li, ACS Appl. Mater. Interfaces **7**(2), 1180 (2015).
[35]H. Liu, K. Xu, X. Zhang, and P. D. Ye, Appl. Phys. Lett. **100**(15), 152115 (2012).
[36]S.-W. Min, H. S. Lee, H. J. Choi, M. K. Park, T. Nam, H. Kim, S. Ryu, and S. Im, Nanoscale **5**(2), 548 (2013).
[37]W. Zhu, T. Low, Yi.-H. Lee, H. Wang, D. B. Farmer, J. Kong, F. Xia, and P. Avouris, Nat. Commun. **5**, 3087 (2014).
[38]A. Tarasov, P. M. Campbell, M.-Y. Tsai, Z. R. Hesabi, J. Feirer, S. Graham, W. Jud Ready, and E. M. Vogel, Adv. Funct. Mater. **24**(40), 6389 (2014).
[39]L. K. Mak, C. M. Rogers, and D. C. Northrop, J. Phys. E **22**(5), 317 (1989).
[40]H. Murrmann and D. Widmann, IEEE Trans. Electron Devices **16**(12), 1022 (1969).
[41]H. H. Berger, Solid-State Electron. **15**(2), 145 (1972).
[42]W. T. Lynch and K. K. Ng, IEEE Int. Electron Device Meet. Dig. **1988**, 352.
[43]S. E. Mohney, Y. Wang, M. A. Cabassi, K. K. Lew, S. Dey, J. M. Redwing, and T. S. Mayer, Solid-State Electron. **49**(2), 227 (2005).