Impact of BTI on Random Logic Circuit Critical Timing

K.P. Cheung, J.W. Lu, G.F. Jiao, C. Vaz, J.P. Campbell, J.T. Ryan
Semiconductor and Dimensional Metrology Division, NIST, Gaithersburg, MD, 20899, USA, kpckpc@ieee.org

Introduction: Bias temperature instability (BTI) is known to be a serious reliability issue for state-of-the-art Silicon MOSFET technology [1-6]. It is well-known that in addition to a "permanent" degradation, there is a large recoverable degradation component [7] that gets larger as the delay between stress and measure is shorter. This recoverable component, when it is taken into account, is often treated as a source for lifetime extension [1-6, 8-12]. In other words, the recovery buys margin in measured lifetime. BTI degradations mostly manifest as threshold voltage (V_{TH}) increase, leading to frequency degradation in ring-oscillator (RO) "test" circuits [8-12]. This RO degradation is the most "circuit relevant" BTI guidance for circuit designers even though RO patterns are poor representations of random digital logic. The fact that recovery is time sensitive leads one to ask, naturally, what will happen to the random pattern in a real logic circuit? To answer this question, existing experimental techniques are not adequate. We recently developed a single transistor eye-diagram technique to address this question and found a previously overlooked but serious BTI impact on critical timing of random logic circuits [13, 14].

Advanced MOSFETs have defects in the gate dielectric even when fresh (as fabricated). Bias-Temperature stress (negative bias for pFET and positive bias for nFET) increases the defect density over time, leading to V_{TH} increase (instability). The "permanent" component of the V_{TH} shift is generally attributed to defects at the gate dielectric-substrate interface (interface states). The recoverable component is generally attributed to bulk defects. For a given bulk defect density, certain percentage of them capture charge during transistor ON time, leading to a finite V_{TH} increase. A certain percentage of these captured charges flows back out to the substrate during transistor OFF time, leading to partial V_{TH} recovery. Statistically, higher percentage of the defects are filled with charges with longer ON time, and higher percentage of the capture charges will flow out with longer OFF time. If the ON/OFF time is fixed, a steady state will reach with a tight distribution of V_{TH} at the end of ON time and the end of OFF time, leading to a unique frequency for the RO. As defect density increases, the steady state shifts to produce a lower RO frequency.

When ON/OFF times are random, as in random logic, the V_{TH} shifts at the end of ON time as well as at the end of OFF time are random. This leads to a random timing sift of the rising edge and falling edge of the logic state of each transistor. Since a critical path typically involves a few logic gates (logic depth), the number of transistors involved can easily more than 10 and their shifts are synchronized and therefore add linearly. The result is significant random skew in addition to the systematic skew increases predicted by RO degradation and this random skew has not been recognized or accounted for in any design solution to BTI degradation. In other words, timing failure due to BTI is a more severe problem than has been known.

Experimental: The challenge in measuring random rising/falling edge shift at full circuit speed is substantial and new approach is needed. We borrowed the eye-diagram technique commonly used in communication network and apply it to a single transistor. This unusual application of eye-diagram method requires careful modification to take care of signal integrity issues such as impedance matching and return current control.

In a nut shell, we apply a pseudo-random binary sequence (PRBS) waveform mimicking random logic to the transistor gate and monitor the drain current. The key is in the method of analyzing the drain current waveform. The eye-diagram method cut the long waveform into 2-bits segments and lay them on top of each other. In the absence of timing jitter, all the rising/falling edges line up precisely. When there is random timing shift, these edges spread out and the statistic of the timing distribution can be extracted.

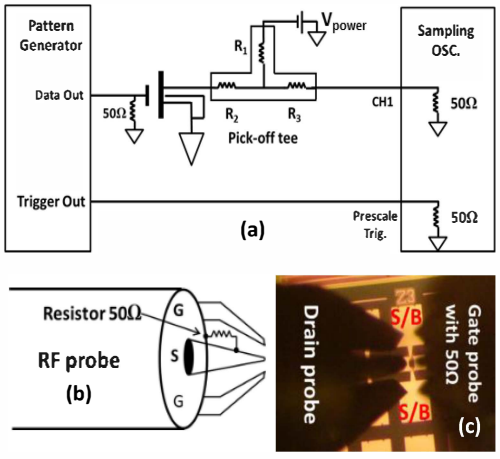

Fig. 1 (a) Experiment setup of the measurement. Transition time (t_r and t_f) of the input signal is 25 ps. (b) Schematic drawing of gate RF probe with 50 Ω termination. (c) Photo of GSG RF probes and RF electrode patterned pMOSFET.

Experimentally, the measurement set up is shown is fig. 1. A pattern generator produces the very high bit rate waveform. This waveform is applied to the gate of the RF transistor (source and body are grounded) with a 50Ω terminated RF probe (ground-signal-ground). The drain current is monitored through another RF probe (not

terminated). The output is connected to a pickoff TEE and then the high-speed oscilloscope with eye-diagram capability. The pickoff TEE allows drain bias to be applied while keeping every well matched to 50Ω to ensure signal integrity. Drain bias is kept at saturation. As the transistor turns ON and OFF, the drain bias varies but always well in the saturation region. The drain current waveform can be calculated from the measured waveform and the known resistance values inside the pickoff TEE. However, for jitter measurement, this conversion is not necessary.

The bit-rate used in our experiment is 2 Gbit/s, limited by the pad capacitance of the RF transistor. The rise and fall time of the pattern coming out of the pattern generator is 25 ps. However, the rise and fall times are much longer is the measured waveform due to the pad capacitance.

The devices used for this study are 10 x 0.18 μm^2 (2 nm/1 nm) HfO_2/SiO_2 pFETs for NBTI and nFETs for PBTI with ground-signal-ground RF layouts. Timing jitter is quantified by recording the transition of ≈32,000 bits repetitively superimposed (such that clock edges are aligned) to construct an eye-diagram (Fig. 2).

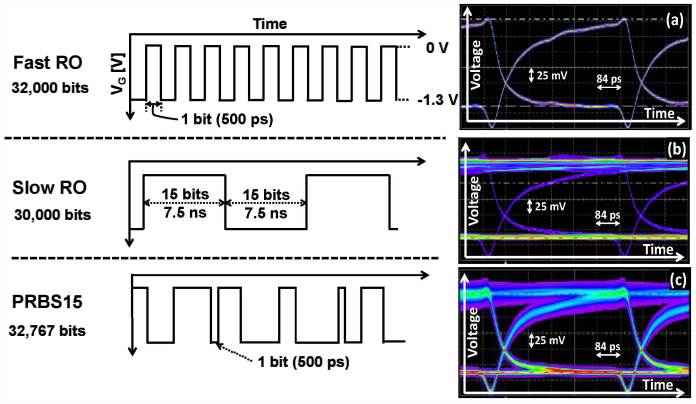

Fig. 2 Three types of bit patterns: fast ring oscillator; slow ring oscillator; and 2^{15} bit pseudo random. Each pattern is over 32,000 bits long. The typical corresponding eye-diagrams are on the right.

Three types of patterns are used for measuring the eye-diagram in this work (fig. 2). Two are regular 50% duty cycle ON/OFF patterns imitating ring oscillators with different frequency. The third one is a pseudo random pattern 2^{15} bit long to simulate random logic. Typical eye-diagrams obtain from these patterns are also shown is fig. 2. Notice how clean the eye-diagrams are for the regular pattern comparing to the random pattern. The under-shoot before transistor turn on is due to displacement current of the pad capacitance (limiting our maximum bit rate).

Devices are each subject to a measure-stress-recovery-measure sequence at 100 °C (18/9 devices for NBTI/PBTI stress). The DC stresses (V_D=V_S= V_B=0 V) are +2V for PBTI and -2V for NBTI. Devices were allowed to recover (V_G=V_D=V_S=V_B=0 V) for 600 s after each stress. After each recovery step, a series of DC (I_D-V_G with V_D = 50 mV) and eye-diagram measurements were performed to assess ΔV_{th} and timing jitter increase (Fig. 5). Eye-diagram measurements were carried out at operation plus 10% voltage. In all cases, ΔV_{th} was determined using a constant-current criterion (500 nA x (W/L)). For each transistor, all measure-stress-recovery-measure-repeat operations are done with one probe landing to ensure consistent contact. This is a subtle but critical detail of the experiment. The use of a pickoff TEE for drain bias as well as drain current measurement is a key enabling choice.

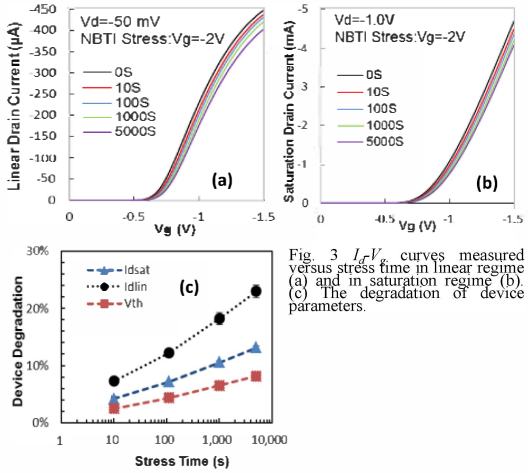

Fig. 3 I_d-V_g curves measured versus stress time in linear regime (a) and in saturation regime (b). (c) The degradation of device parameters.

Results and Discussion: Fig. 3 shows the transistor degradation under NBTI stress in the normal parameters such as V_{TH} shift, I_D degradation, etc… After 5000 seconds stress, V_{TH} degradation is about 8%. This is not yet at a failure level (for V_{TH}).

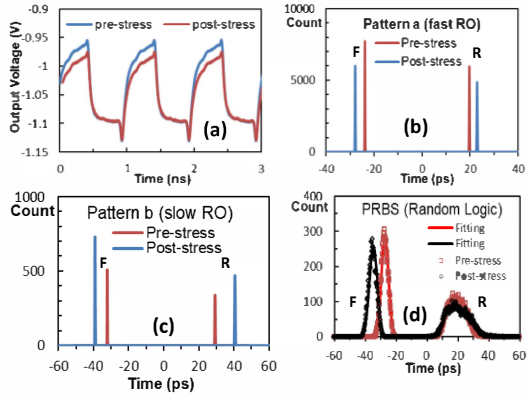

Fig.4 (a) Pre- and post-stress output waveforms of fast RO pattern and (b) the Pre- and post-stress jitter histograms extracted from the eye diagrams of fast RO pattern. (c) is the case for slow RO and (d) for PRBS15. F (R) is falling (rising) edge.

Fig. 4 shows some typical results with high-speed bit patterns. Fig. 4a shows how the drain current waveform degrades after stress. Remember that this is not the actual drain current but the directly related to it through the pickoff TEE. The ON current is clearly degraded after stress. Figures 4b & 4c are timing distribution of the rising and falling edges before and after stress for the fast RO

(4b) and slow RO (4c) cases. Timing of the rising/falling edge are measure at mid-point of the waveform. An obvious characteristic for all edges are very tight distribution, meaning very small jitter. This is consistent with the discussion earlier about RO. A steady state is reached. While that steady state depends on the frequency, the regular ON/OFF leads to a sharp distribution of rising/falling edges. Another characteristic is that after stress the rising edge shifted to earlier in time while the falling edge shifted to later in time. This stretch in time between rising and falling is a reflection of the frequency degradation in RO circuit after stress. Such time shifts are well-captured in the conventional RO-type measurements and circuit design solutions have been well publicized [2, 9-12]. In this work, we focus on the case in figure 4d and examine the changes in stress-induced *random* timing jitter. Random timing jitter is manifested as a broadening of the jitter distribution and is a substantially more formidable circuit reliability obstacle. As seen in figure 4d, the systematic shift of the rising and falling edges, similar to the RO cases, is still there. What we want to examine is the change in the width of the distribution as we stress the device. Some of that increase is already visible in figure 4d.

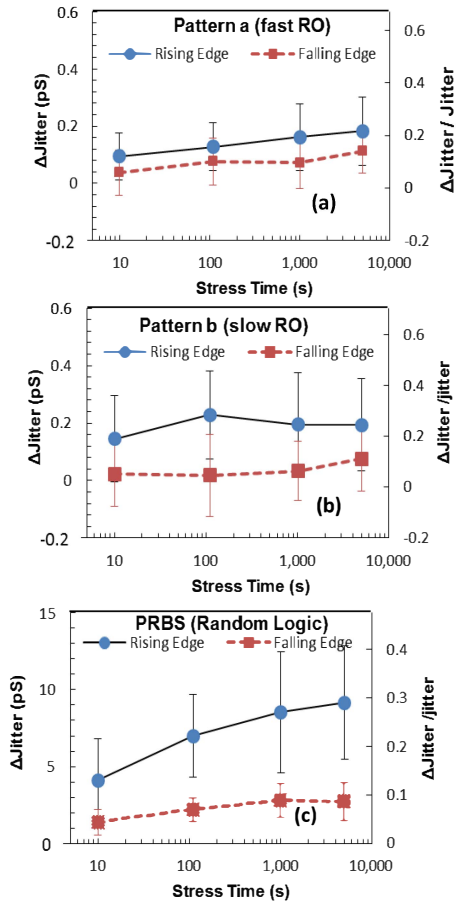

Fig. 5 Jitter degradation versus stress time with standard deviation from 18 devices for (a) fast RO (b) slow RO; (c) random logic of PRBS15.

Figure 5 plots the *change* of the timing distribution width, which we call *ΔJitter*, for the three patterns as a function of stress time. For RO patterns the data are within the noise, consistent with our expectation. For the pseudo random pattern, the *ΔJitter* of the rising edge increases with stress time significantly. Please note the difference in scale. The falling edge, on the other hand, is hardly changed. This asymmetry has to do with the measurement point. Referring to the eye-diagram for pseudo random pattern in figure 2, one can see that the mid-point is indeed very tight for the falling edge. In logic circuit, mid-point is not where timing is determined. If we use 70% for turn on and 30% for turn off, the problem is larger for both edges. Even using mid-point, the jitter increase on the rising edge alone is very significant when one remember that *ΔJitter* for transistors in the logic path add linearly.

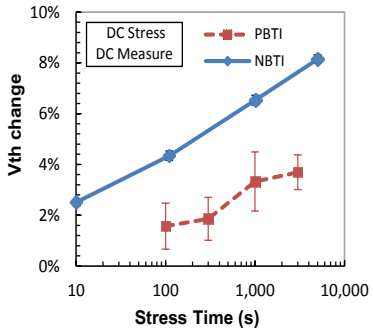

Fig. 6 Comparing V_{TH} shifts due to NBTI and PBTI as a function of stress time.

Figure 6 compares the V_{TH} shifts between NBTI and PBTI as a function of stress time. As is well known, PBTI has a smaller effect than NBTI. For the same stress amount (time and gate overdrive), the degradation for PBTI is about half of that from NBTI. When compare *ΔJitter* however, the difference is more pronounced. Figure 7 shows the rising edge *ΔJitter* as a function of stress time for both NBTI and PBTI. As can be seen, the jitter increase for PBTI is roughly 10 times smaller than that for NBTI.

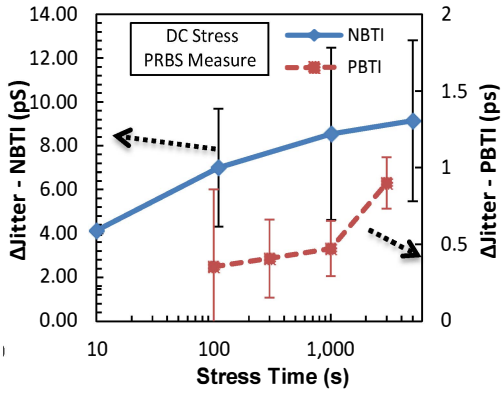

Fig. 7 Comparing *ΔJitter* from pseudo random pattern due to NBTI and PBTI as a function of stress time.

The difference in *Δlitter* respond between NBTI and PBTI may be explained by where the charges are trapped. For NBTI, the trapped charges responsible for fast transients are believed to be holes. The fast respond suggests that holes are mostly trapped in the buffer oxide layer near the interface. This make sense because hole mobility in SiO_2 is very low, making them ready to be captured by defect sites. For PBTI, electrons are the trapped charges. They have high mobility in the buffer layer and believed to be mostly trapped in the high-k layer which is known to have much higher defect density than the oxide buffer layer. The distance from the interface greatly affects the frequency respond. In our experiment, the ON/OFF time ranges from 500ps to a few μs. Traps beyond the 1 nm buffer layer cannot exchange charge with the inversion layer. Thus we see a much smaller *Δlitter* effect for the same amount of V_{TH} shift for PBTI.

Conclusions: Using a newly developed single transistor eye-diagram method, we examined the effect of BTI stress on logic circuit critical timing under a realistic bit pattern (pseudo random). We demonstrated that the recoverable part of the BTI degradation produce significant timing skew that is random in nature. This random timing skew is in addition to the systematic timing degradation captured in measurements using ring oscillator circuits. The size of this random skew is very large and can be a serious problem for logic circuit under tight timing budget. This effect has not been known before and therefore not accounted for in any of the proposed circuit methodology to mitigate BTI effects.

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