Evaluation of Uncertainty in Temporal Waveforms of Microwave Transistors

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***Abstract*—We evaluate the uncertainty in on-wafer vector-calibrated nonlinear measurements with the National Institute of Standards and Technology (NIST) Microwave Uncertainty Framework. We include in our analysis uncertainties in the passive calibration standards, power meter, NIST-traceable phase calibration reference, cable bending, and probe alignment. These uncertainties are propagated first to the electrical quantities across the terminals of the device-under-test, which was an on-wafer microwave transistor. Next, we propagate uncertainties to the transistor current-generator plane, whose temporal voltage/current waveforms and impedances are of interest for the design of power amplifiers.**

***Index Terms*—Microwave measurements uncertainty, microwave transistors, nonlinear de-embedding, vector-calibrated nonlinear measurements.**

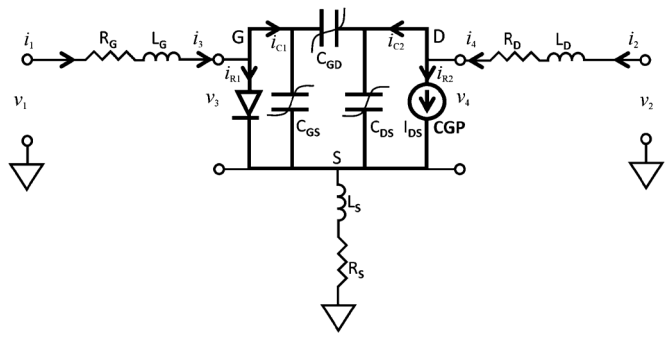

Fig. 1. Simplified nonlinear model for a field-effect transistor. "CGP" indicates the current-generator plane. v_1, i_1, v_2, and i_2 are the voltages and currents at the transistor terminals.

I. Introduction

MUCH PROGRESS has been made in large-signal network analysis over the last two decades [1]–[6]. Systems like the large-signal network analyzer (LSNA) enable the acquisition of the vector calibrated time-domain waveforms at the terminals of a transistor at microwave frequencies. These systems can be used for characterization, modeling, and waveform engineering.

One crucial step when dealing with microwave measurement systems is the calibration, which removes most of the systematic errors introduced by the measurement system itself. Nevertheless, residual uncertainties in the calibration procedure still exist and become significant as the measurement frequency increases. These uncertainties originate, for instance, from imperfections in the calibration standards.

Much work has been devoted to the uncertainty evaluation in measurements at microwave and millimeter-wave frequencies, including [7]–[13]. In [7]–[11], uncertainty is evaluated in microwave small-signal measurements. In [12] and [13], the study of uncertainty is carried out for load–pull measurements. Nevertheless, [12] and [13] focus on scalar quantities such as gain and output power.

Here we evaluate residual calibration uncertainties in on-wafer vector-calibrated large-signal measurements performed with a mixer-based LSNA. We account in this work for uncertainties in the relative calibration, absolute calibration, cable bending, and probe alignment. We propagated these uncertainties first to the waves across the transistor terminals. Furthermore, we shifted the uncertainties to the transistor current-generator plane, whose electrical quantities are of great interest for the design of power amplifiers.

II. Motivation

Knowledge of the temporal current and voltage at the transistor current-generator plane (see Fig. 1) is crucial in order to perform waveform engineering, which is a useful tool for the design of power amplifiers [14]. The various classes of operation of power amplifiers are defined by the shape of these waveforms across the transistor's current-generator plane [15], [16].

Waveform engineering can be performed in different ways. One approach consists of starting from a model of the transistor current source and using this model to generate the desired time-domain waveforms in a simulation environment [17]. Alternatively, one can directly measure the voltages and currents at the desired operating frequency [14]. The latter approach is preferred in many situations, as the extraction of an accurate nonlinear model for the transistor current source, including trapping and thermal effects [18], may not be a straightforward task.

Starting from measurements, one can search for the operating condition that yields the desired performance, and based on the

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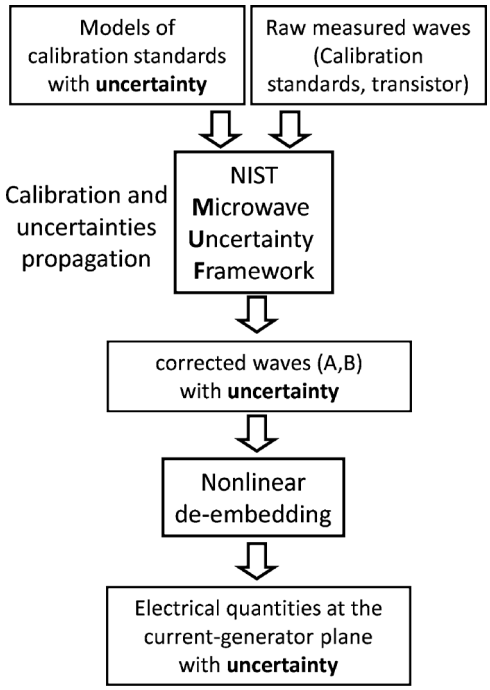


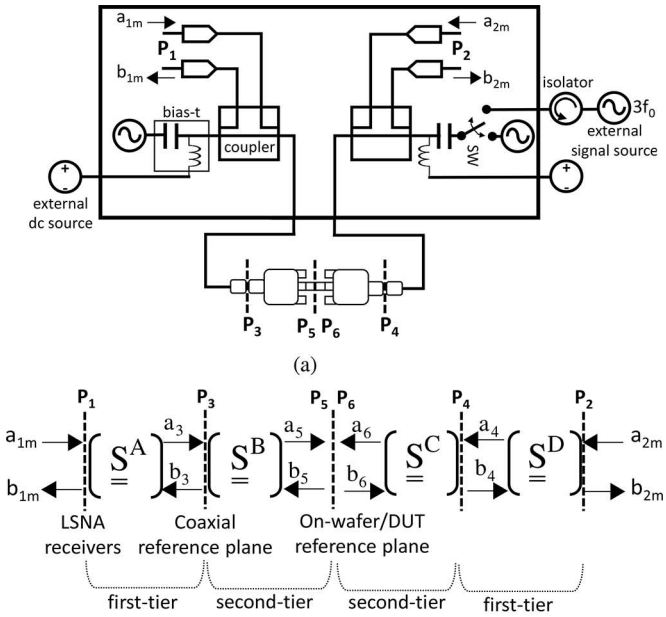
Fig. 2. Calibration and nonlinear de-embedding procedure.

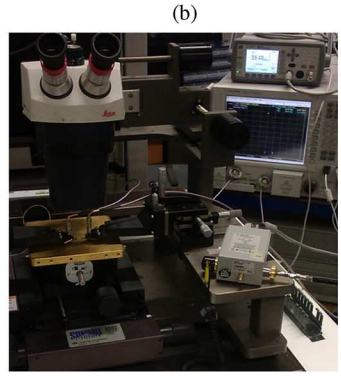
experimental voltage and current waveforms, determine the impedances needed at the transistor terminals. As long as the design frequency is low enough to neglect the transistor's parasitic elements and the transistor's nonlinear capacitances, the measured time-domain waveforms are very close to those appearing at the current-generator plane. Therefore, the selected impedances, obtained directly from measurements, guarantee the desired class of operation.

However, this assumption may not be valid at microwave frequencies. The measured current and voltage waveforms, along with the corresponding impedances, may differ from those at the current-generator plane as they are distorted by both the parasitics and the transistor's nonlinear capacitances. In this situation, one needs to determine the electrical quantities at the current-generator plane starting from time-domain waveforms measured at microwave frequencies. Thus, a nonlinear de-embedding procedure is needed in order to determine the impedances at the current-generator plane [19]–[21] based on microwave nonlinear measurements.

Nonlinear de-embedding relies on direct characterization of the linear parasitic network associated with transistor layout and access structures, and of the transistor's intrinsic nonlinear capacitances. Once these are determined, one can obtain the actual voltages and currents at the current-generator plane corresponding to those measured at microwave frequencies. However, no study has been performed yet to estimate the uncertainty in the current and voltage time-domain waveforms and impedances obtained after nonlinear de-embedding.

In this work, we propagate residual uncertainties to the electrical quantities at the transistor current-generator plane, as illustrated in Fig. 2. Starting from on-wafer raw LSNA measurements, we propagate uncertainties first through the calibration algorithm. Next, we propagate uncertainties through the nonlinear de-embedding algorithm.





(c)

Fig. 3. (a) Simplified measurement set-up and (b) calibration model in terms of error boxes. In (a), the switch SW is connected to the internal source during the calibration. During the measurements with the transistor it is connected to an external signal source to perform active load–pull. In (c), a mixer-based LSNA set-up. (Trade names are used here only to fully specify the experimental configuration and do not constitute an endorsement by NIST. Other instruments made by the same or different manufacturer may function as well or better for this application.)

III. Calibration

A. Nominal Calibration

We performed the calibration with the NIST Microwave Uncertainty Framework.[1] The Microwave Uncertainty Framework supports several calibration algorithms [22] and allows one to propagate residual uncertainties to the calibrated device-under-test (DUT) S-parameters and traveling waves, and to quantities derived from them [7], [23].

We calibrated raw waves acquired with a 50-GHz LSNA, as illustrated in Fig. 3. The calibration grid was defined with the fundamental frequency f_0 equal to 5 GHz and eight harmonics. The resolution bandwidth (IF bandwidth) was set to 1 Hz. The error boxes in Fig. 3(b) are described in terms of S-parameters, but other description could be adopted [4]. In Fig. 3, the raw

[1][Online]. Available at http://www.nist.gov/ctl/rf-technology/related-software.cfm

waves, as measured by the LSNA receivers, are a_{1m}, b_{1m}, a_{2m}, and b_{2m}. The corrected waves at the transistor terminals are a_5, b_5, a_6, and b_6 and are used to derive i_1, v_1, i_2, and v_2 in Fig. 1. As shown in Fig. 3(a), we performed a two-tier calibration.

The first tier is split into two parts, as typically done for LSNA measurements [4]. A relative calibration determines the reflection terms of the error boxes and the product of the transmission terms [22].

The actual value of the transmission terms is determined by the absolute calibration, which consists of connecting a power and phase reference at P_3 in Fig. 3(b) [2], [4], [24].

The second-tier calibration was performed directly on wafer and we used a multiline thru-reflect-line (TRL) algorithm [25]–[27].

Here we summarize the measurements steps.

Step 1) Raw waves were acquired while connecting one-port standards (i.e., short, open, and load) and a transmission standard (thru) at P_3 and P_4.

Step 2) Raw waves were acquired while connecting a power sensor and a phase reference at P_3.

Step 3) Raw waves were acquired while probing on-wafer calibration standards.

Step 4) Raw waves were acquired while probing the transistor.

Step 5) Raw waves were calibrated with the NIST Microwave Uncertainty Framework.

B. Calibration With Uncertainty Evaluation

The NIST Microwave Uncertainty Framework propagates uncertainty through each calibration step. We included in our analysis uncertainties in the passive calibration standards, power meter, NIST-traceable phase calibration reference, cable bending, and probe alignment. We neglected the uncertainties in the measured raw waves due to noise of the high-dynamic range receivers of the mixer-based LSNA [28].

Also, in order to account for any drift occurring during the measurement period, we acquired the measurements of the calibration standards before and after the transistor measurements. We performed the calibration with the Microwave Uncertainty Framework twice and averaged the two calibrations.

We developed physical models of the passive calibration standards and estimated the uncertainties in the models' elements from mechanical tolerances from the manufacturer [29].

In Tables I and II, we report the error mechanisms included within the calibration and their uncertainties.

The values of the physical dimensions of the on-wafer transmission lines and their uncertainties are estimated from the foundry process datasheet.

We accounted for probe-alignment errors with a model available in the NIST Microwave Uncertainty Framework.

To characterize the impact of cable bending, we measured a thru line in its relaxed state, and then remeasured it as we bent the cable in a similar way to what we do in practice. In this way we were able to include uncertainties in cable bending in our experiments based on direct measurements.

The comb generator was characterized at NIST with a sampling oscilloscope [30], [31] and uncertainty propagated in its phase spectrum. The uncertainty in the comb-generator phase at the frequencies of our calibration grid is reported in Table III.

For the amplitude calibration we included errors in the power-meter measurements. We included the following errors, as defined in [32]: the reference oscillator mismatch, the reference oscillator power uncertainty, the zero-set error, the zero carry-over error, and the instrumentation error, and error in the power

TABLE I
STANDARDS USED FOR THE SOLT CALIBRATION WITH ASSOCIATED UNCERTAINTIES

Offset Short	
Inner conductor diameter (mm)	1.042±0.004
Outer conductor diameter (mm)	2.400±0.005
Outer conductor length (mm)	6.750±0.005
Pin diameter (mm)	0.511±0.005
Offset Load	
Inner conductor diameter (mm)	1.042±0.004
Outer conductor diameter (mm)	2.400±0.005
Line length (mm)	7.700±0.005
Load resistance (Ω)	50±0.7
Load inductance (nH)	0.02±0.02
Pin diameter (mm)	0.511±0.005
Offset Open	
Inner conductor diameter (mm)	1.042±0.004
Outer conductor diameter (mm)	2.400±0.005
Line length (mm)	6.750±0.005
Pin diameter (mm)	0.511±0.005
Thru	
Inner conductor diameter (mm)	1.042±0.004
Pin diameter (mm)	0.511±0.005

TABLE II
STANDARDS USED FOR THE TRL CALIBRATION WITH ASSOCIATED UNCERTAINTY: W IS THE WIDTH OF THE LINES, H IS THE THICKNESS OF THE SUBSTRATE, AND L IS THE LENGTH OF THE LINES. C IS THE LOW-FREQUENCY CAPACITANCE OF THE LINES [27]

	W (μm)	H (μm)	L (μm)
Line (L_1)	48.7±2	70±7	3850±2
Line (L_2)	48.7±2	70±7	1200±2
Line (L_3)	48.7±2	70±7	400±2
THRU	48.7±2	70±7	0
Reflect	48.7±2	70±7	0
Probe-alignment error	±5 μm		
C = 1.953 pF/cm			

TABLE III
NOMINAL VALUE AND POINT-BY-POINT STANDARD UNCERTAINTY OF THE COMB-GENERATOR PHASE SPECTRUM CHARACTERIZED WITH A SAMPLING OSCILLOSCOPE [30], [31]. WE ALSO INCLUDED FULL CORRELATIONS OF ALL UNCERTAINTIES CONSIDERED IN THE CHARACTERIZATION OF THE COMB GENERATOR

Frequency (GHz)	Phase (degree)
5	173.7±0.3
10	167.8±0.5
15	162.6±0.5
20	156.6±0.7
25	151.8±0.7
30	149.2±0.5
35	149.4±0.7
40	138.2±0.6

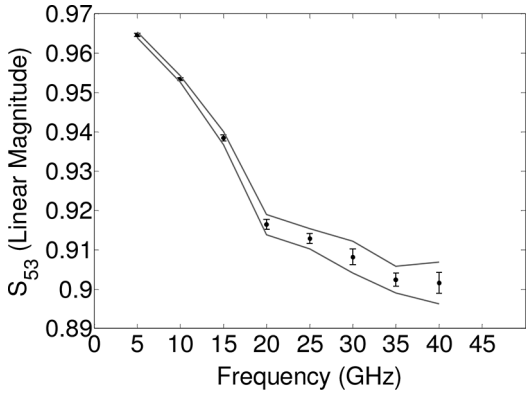


Fig. 4. Standard uncertainty and 95% confidence interval of the magnitude of the transmission term of error box between P_3 and P_5.

sensor calibration factor. Typical values for these errors can be found in manufacturer's documentation [32]. We also measured the input match of the power sensor with a calibrated vector network analyzer (VNA) and used it in the amplitude calibration procedure.

The uncertainties in Tables I–III propagate to the corrected waves through the equations of the chosen calibration algorithm and are mapped as uncertainties in the error box coefficients. For example, in Fig. 4, we report the nominal value, along with the uncertainty and 95% confidence interval, of error coefficient S_{53}, which is the transmission term of the error box S^B in Fig. 3(b).

The next step consists of propagating the uncertainties in the corrected waves incident on the transistor to the transistor current source. The nonlinear de-embedding algorithm [33] used to perform this step is described in Section IV.

IV. Nonlinear De-Embedding

With reference to Fig. 1, we define the following vectors:

$$\underline{V_m}_h = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}_h \tag{1}$$

$$\underline{I_m}_h = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}_h \tag{2}$$

$$\underline{V_{\rm int}}_h = \begin{bmatrix} V_3 \\ V_4 \end{bmatrix}_h \tag{3}$$

$$\underline{I_{\rm int}}_h = \begin{bmatrix} I_3 \\ I_4 \end{bmatrix}_h \tag{4}$$

where h is the frequency index. $\underline{V_m}$ and $\underline{I_m}$ are the voltages and currents at transistor terminals as measured at microwave frequencies and obtained after calibration. The first step of the de-embedding procedure consists of removing the contribution of the linear parasitic network (see Fig. 1) and obtaining the voltages and currents $\underline{V_{\rm int}}$ and $\underline{I_{\rm int}}$. The linear parasitic network, whose elements are extracted as in [34] and [35] and reported in Table IV can be described by a 4×4 frequency dependent Y-parameter matrix, which links $\underline{V_{\rm int}}$ and $\underline{I_{\rm int}}$ to $\underline{V_m}$ and $\underline{I_m}$ by means of (5),

$$\begin{bmatrix} \underline{I_m}_h \\ \underline{I_{\rm int}}_h \end{bmatrix} = \underline{\underline{Y}}_h \begin{bmatrix} \underline{V_m}_h \\ \underline{V_{\rm int}}_h \end{bmatrix}. \tag{5}$$

TABLE IV
Values of the Parasitic Elements

R_G (Ω)	R_D (Ω)	R_S (Ω)
1.1	0.9	0.3
L_G (pH)	L_D (pH)	L_S (pH)
26.2	25.6	13.8

The intrinsic voltages obtained from (5) are those that control the conductive phenomena and the charge storage within the semiconductor area. The former generate the resistive part of the transistor currents ($\underline{i_R}$), the latter the displacement currents ($\underline{i_C}$). Therefore,

$$\underline{i_{\rm int}} = \underline{i_R} + \underline{i_C} \tag{6}$$

with

$$\underline{i_R} = \begin{bmatrix} i_{R1} \\ i_{R2} \end{bmatrix} \tag{7}$$

$$\underline{i_C} = \begin{bmatrix} i_{C1} \\ i_{C2} \end{bmatrix}. \tag{8}$$

The second step of the nonlinear de-embedding process consists of computing the vector of displacement currents as a function of the intrinsic voltages (9)

$$\underline{i_C} = f(\underline{v_{\rm int}}). \tag{9}$$

The function f describes the transistor intrinsic capacitances, which are bias dependent. Therefore, f is typically nonlinear and can be expressed either in the form of a look-up table [34] or by analytical expressions [36]. In this work, the value of the capacitances are obtained from the bias-dependent imaginary parts of the Y-parameters derived from measured multibias S-parameters. The displacement currents can be computed by means of harmonic-balance simulations.

Once the vector i_c is known, the resistive currents can be computed at each frequency from large-signal measurements with

$$\underline{I_R}_h = \underline{I_{\rm int}}_h - \underline{I_C}_h. \tag{10}$$

Using this procedure, we obtain the time-domain waveforms of the transistor resistive currents along with the impedances as seen at the current-generator plane, which are computed from

$$Z_h^{\rm CGP} = -\left.\frac{V_4}{I_{R2}}\right|_h. \tag{11}$$

In this work, we kept fixed the elements of the parasitic network. Therefore, the results of (10) and (11) strongly depend on the selection of the function f (9), which is directly linked to the transistor capacitance model. The wrong selection of f has a direct impact on the electrical quantities at the current-generator plane and on their uncertainty, as discussed in Section V.

V. Uncertainty Analysis

This section is split into three parts. Section V-A focuses on the selection of the capacitance model. Section V-B deals with the uncertainty propagation to the electrical quantities at the current-generator plane. In Section V-C, the results are discussed.

TABLE V
NOMINAL VALUE OF THE IMPEDANCES AT THE EXTRINSIC PLANE AND AT THE CURRENT-GENERATOR PLANE AFTER NONLINEAR DE-EMBEDDING

	f_0 (Ω)	$2f_0$ (Ω)	$3f_0$ (Ω)
Z_{EXT}	52.2-j2.6	53.1-j5.9	36.7+j373.8
Z_{INT}	53.3-j1.3	54.2-j3.3	40.1+j373.5
$Z_{CGP,1}$	49.4-j18.7	42.0-j11.9	29.1-j34.7
$Z_{CGP,2}$	51.4-j1.1	50.4-j10.2	78.6-j40.9
$Z_{CGP,3}$	49.3-j16.6	40.4-j22.4	94.2-j117.1

A. Selection of the Intrinsic Capacitance Model

We studied a 0.25×300 μm^2 gallium–arsenide (GaAs) transistor. The transistor was biased at $V_{GS0} = -0.6$ V and $V_{DS0} = 6$ V. The experimental conditions that we considered are such that the gate Schottky junction, represented with the diode in Fig. 1, is never brought to forward or reverse conduction. Therefore, we neglected resistive current i_{R1} (Fig. 1). The only resistive current we refer to is that associated with the current source I_{DS} in Fig. 1.

The intrinsic transistor capacitances are extracted from Y-parameters derived from multi-bias S-parameter measurements. The bias-dependent values of the capacitances are then stored in a look-up table. The look-up table description, as compared to analytical formulations, is very accurate, as nonlinear capacitances are extracted directly from measurements over a dense grid of bias points. However, the look-up-table-based description has limited extrapolation capability outside the range of the measurements used for the extraction. In order to prevent extrapolation errors, the experimental temporal waveforms considered in this work are such to fall within the measurement grid of the multi-bias S-parameters. We applied nonlinear de-embedding to the following cases.

1) *Linear capacitance model*. The values of the intrinsic capacitances are assumed to be constant and equal to the value stored in the table corresponding to the selected bias point. For the device considered in this work, these values are: $C_{GS} = 534$ fF, $C_{GD} = 36$ fF, $C_{DS} = 59$ fF, and $C_m = 313$ fF. C_m is the transcapacitance [37].
2) *Partial nonlinear capacitance model*. Full look-up table, except that the feedback capacitance C_{GD} is neglected.
3) *Fully nonlinear capacitance model*. No approximations are made and the full look-up table is used.

We performed LSNA measurements with the load impedance at f_0 and $2f_0$ close to 50 Ω. The load impedance at $3f_0 = 15$ GHz was tuned by active signal injection and we searched for a value close to the edge of the Smith chart. In this way we could mimic for the third harmonic the situation encountered in the designing high-efficiency amplifiers, where harmonics are terminated with an open or short circuit [15], [16]. The value of the measured output impedance (Z_{EXT}) at f_0, $2f_0$, and $3f_0$ is reported in Table V. In Table V, we report the impedances at the intrinsic plane (Z_{INT}) and the impedances at the current-generator plane (Z_{CGP}) obtained after performing nonlinear de-embedding with the three transistor capacitance models.

As expected, the impedances at the current-generator plane strongly depend on the values of the de-embedded transistor capacitances and the nonlinear capacitance model we used. Moreover, each set of de-embedded impedances results in different current and voltage time-domain waveforms at the current-generator plane, as shown in Fig. 5.

In Fig. 5, we report the dynamic voltage–current relationships (i_4 versus v_3) and loadline (i_4 versus v_4) corresponding to the impedance Z_{INT} in Table V obtained after de-embedding only the effect of the linear parasitic network. In the same figure, we show the dynamic voltage–current relationships (i_{R2} versus v_3) and loadline (i_{R2} versus v_4) at the current-generator plane after de-embedding the transistor nonlinear capacitances, corresponding to $Z_{CGP,1}$, $Z_{CGP,2}$, and $Z_{CGP,3}$ in Table V. $Z_{CGP,1}$, $Z_{CGP,2}$, and $Z_{CGP,3}$ are also shown on the Smith chart along with the measured impedance Z_{EXT}.

If the nonlinear de-embedding is properly performed, the de-embedded resistive current waveform i_{R2} must satisfy constraints directly linked to the transistor's physical behavior. First, the current must show clipping at zero amperes when the instantaneous gate–source voltage (v_3 in Fig. 1) is smaller than the threshold voltage. Moreover, if the transistor in saturation region behaved as an ideal voltage controlled current–source, voltage–current relationships shown in Fig. 5—i_{R2} versus v_3 (a)–(c)—should show almost no hysteresis. This behavior should manifest even if the loadline at the current–source terminals—i_{R2} versus v_4 [see Fig. 5(d)–(f)]—was not a closed line. Clearly the actual behavior of the transistor may deviate from that ideal if channel-length modulation and thermal effects are not negligible and may introduce a slight hysteresis in the voltage–current relationships in Fig. 5(a)–(c).

The only dynamic voltage–current relationship (i_{R2} versus v_3), which reproduces the behavior close to that of a voltage-controlled current source, is that in Fig. 5(c), which corresponds to $Z_{CGP,3}$ [see Fig. 5(i)] and which is obtained by using the fully nonlinear capacitance model. The linear model yields a resistive current waveform, which poorly clips to zero amperes in the pinch-off region [see Fig. 5(a)], where the actual capacitance to be de-embedded is smaller than that at the bias point. When neglecting the feedback capacitance ($C_{GD} = 0$ F), significant hysteresis remains in the de-embedded voltage-current relationship [see Fig. 5(b)].

Similarly, the wrong selection of the transistor capacitance model affects the time-domain waveform of the gate current, which is purely capacitive in our case and related to C_{GS} and C_{GD} in Fig. 1. The measured temporal gate-current waveform is compared in Fig. 6 with the simulations obtained by the three capacitance models. As before, the best agreement is obtained with the fully nonlinear capacitance model.

This analysis, which can be extended to other devices and different technologies, suggests that waveform engineering can be performed, as proposed in [14], if one accurately knows the transistor's nonlinear capacitances and the parasitic elements. In this way, one can obtain the time-domain waveforms appearing at the current-generator plane [33]. Taking this into consideration, in Section V-B we report the results obtained by propagating the uncertainty in the calibrated waves at the transistor terminals to the electrical quantities at the current-generator plane.

B. Uncertainty Results

The NIST Microwave Uncertainty Framework performs error analysis based on a sensitivity approach and Monte Carlo

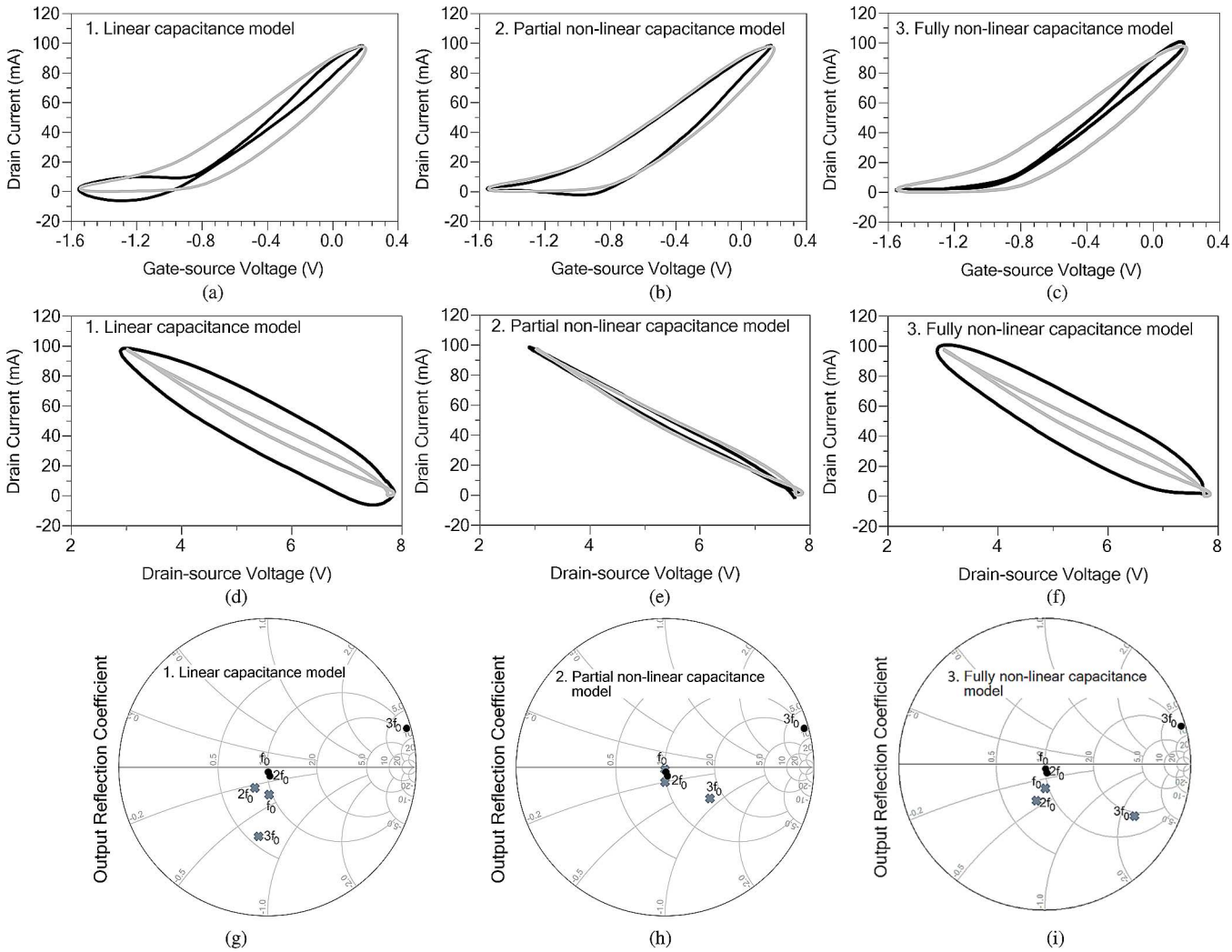


Fig. 5. Dynamic transcharacteristic and loadline of the GaAs pHEMT at: $V_{\mathrm{GS0}} = -0.6$ V, $V_{\mathrm{DS0}} = 6$ V, and $f_0 = 5$ GHz. Transcharacteristic at the intrinsic plane (grey line) and the current generator plane (black line) after applying nonlinear de-embedding to the measurement assuming (a) linear capacitances, (b) $C_{\mathrm{GD}} = 0$ F, and (c) nonlinear capacitances. Corresponding loadlines are shown in (d), (e), and (f). In (g), (h), and (i), the measured output impedance (Z_{EXT}) (dot) and the impedance at the current-generator plane obtained after de-embedding (crosses) at f_0, $2f_0$, and $3f_0$.

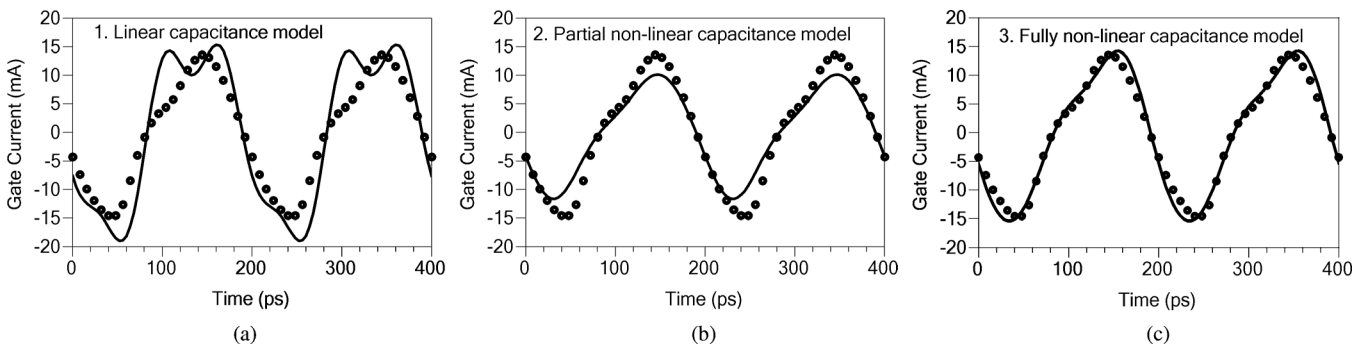


Fig. 6. Measured (symbols) gate-current time-domain waveform of the GaAs pHEMT at: $V_{\mathrm{GS0}} = -0.6$ V, $V_{\mathrm{DS0}} = 6$ V, and $f_0 = 5$ GHz. The simulated gate-current waveform (continuous line) is obtained assuming: (a) linear capacitances, (b) $C_{\mathrm{GD}} = 0$ F, and (c) nonlinear capacitances.

method that preserve correlations in the uncertainties [7], [23]. As schematically illustrated in Fig. 7, the uncertainties in the calibration standards are first mapped through the calibration coefficients into the corrected waves at the transistor terminals both in the frequency and time domain. Subsequently, the uncertainties in the corrected waves at the transistor terminals are propagated to the electrical quantities at the transistor current-generator plane. This is accomplished via a post-processor module, which is embedded in the Microwave Uncertainty Framework.

The post-processor module in the Microwave Uncertainty Framework controls a commercial circuit simulator where the

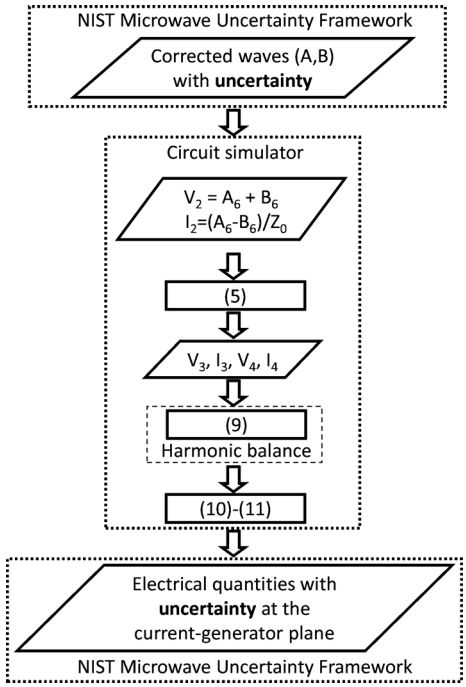


Fig. 7. Microwave Uncertainty Framework and post-processor. The equations of the nonlinear de-embedding and the harmonic-balance analysis are performed with a commercial circuit simulator.

TABLE VI
NOMINAL VALUE, STANDARD UNCERTAINTY, AND 95% CONFIDENCE INTERVAL OF THE IMPEDANCE AT THE EXTRINSIC PLANE, AT THE INTRINSIC PLANE, AND AT THE CURRENT-GENERATOR PLANE

	nominal(Ω)	std. unc.(Ω)	95% interval
$\mathrm{Re}\{Z^{EXT}(f_0)\}$	52.2	±1.3	±2.6
$\mathrm{Im}\{Z^{EXT}(f_0)\}$	-2.6	±0.2	±0.4
$\mathrm{Re}\{Z^{EXT}(2f_0)\}$	53.1	±1.0	±2.0
$\mathrm{Im}\{Z^{EXT}(2f_0)\}$	-5.9	±0.5	±1.0
$\mathrm{Re}\{Z^{EXT}(3f_0)\}$	36.7	±6.6	±13.2
$\mathrm{Im}\{Z^{EXT}(3f_0)\}$	373.8	±26.2	±52.4
$\mathrm{Re}\{Z^{INT}(f_0)\}$	53.3	±1.3	±2.6
$\mathrm{Im}\{Z^{INT}(f_0)\}$	-1.3	±0.2	±0.4
$\mathrm{Re}\{Z^{INT}(2f_0)\}$	54.2	±1.0	±2.0
$\mathrm{Im}\{Z^{INT}(2f_0)\}$	-3.3	±0.5	±1.0
$\mathrm{Re}\{Z^{INT}(3f_0)\}$	40.1	±6.9	±13.7
$\mathrm{Im}\{Z^{INT}(3f_0)\}$	373.5	±25.9	±51.8
$\mathrm{Re}\{Z^{CGP}(f_0)\}$	49.3	±0.9	±2.0
$\mathrm{Im}\{Z^{CGP}(f_0)\}$	-16.6	±0.6	±1.3
$\mathrm{Re}\{Z^{CGP}(2f_0)\}$	40.4	±0.4	±0.8
$\mathrm{Im}\{Z^{CGP}(2f_0)\}$	-22.4	±0.8	±1.5
$\mathrm{Re}\{Z^{CGP}(3f_0)\}$	94.2	±6.1	±15.4
$\mathrm{Im}\{Z^{CGP}(3f_0)\}$	-117.1	±7.7	±12.3

equations of the nonlinear de-embedding (5), (9)–(11) were implemented and propagates the sensitivity and Monte Carlo analyses through the circuit simulations. The circuit simulator enabled harmonic-balance analysis, which was needed to evaluate the displacement current generated by the nonlinear capacitances (9).

Along with the sensitivity analysis, which included 394 sources of uncertainty, we performed 100 Monte Carlo simulations. As previously mentioned, the measurands we focused on are the electrical quantities at the current-generator plane.

In Table VI, we report the nominal value, standard uncertainty, and confidence interval of the impedances at f_0, $2f_0$, and $3f_0$. The impedances in Table VI are those at the extrinsic plane (i.e., transistor terminals), at the intrinsic plane (only parasitic network is de-embedded), and the current generator plane. In Fig. 8, we also show the histograms, including Monte Carlo simulations results, of the impedances at the current-generator plane. Monte Carlo results confirm the validity of the sensitivity analysis as no significant statistical bias is observed in the expected value.

The individual contributions to the total uncertainty in the impedances at the current-generator plane are reported in Table VII.

Each of the contributions listed in Table VII can be further linked to fundamental error mechanisms, as reported in Table VIII for the TRL calibration.

Imperfections in the physical dimensions of the lines affect the characteristic impedance [26] whose uncertainty propagates to the calibrated voltage and current waveforms and then to the impedances derived from them.

From Table VII, it also emerges that the uncertainty in the impedances at the current-generator plane is also affected by errors in the absolute calibration. On the other hand, the impact of errors in the absolute calibration is zero when looking at the impedance at the extrinsic and intrinsic planes. This can explained as follows. The impedance at the extrinsic and intrinsic plane are calculated either directly from measurements at the same reference plane, i.e., the extrinsic plane, or at the intrinsic plane as a result of a linear transformation (5). In these cases, the ratio of voltage and current is obviously not affected by errors in the absolute calibration. Differently, the impedances at the current-generator plane are derived from (9)– (11), which also include a nonlinear transformation applied to the intrinsic voltages due the capacitance nonlinearity (9). This transformation makes the impedances at the current-generator plane also sensitive to errors in the absolute calibration.

In Fig. 9, we show the temporal waveforms of the voltage and current at the current-generator plane. As the NIST Microwave Uncertainty Framework keeps track of correlations, we can also look at the uncertainty in time domain.

C. Additional Discussion

In Section IV, we highlighted the importance of the choice of a proper capacitance model in order to get correctly uncertainties after applying a nonlinear de-embedding procedure. Based on the obtained results, some considerations can be made.

We firstly observe that the uncertainty at the extrinsic plane in the impedance at $3f_0$ is much larger than the uncertainty at f_0 and $2f_0$. This can be intuitively explained considering that at $3f_0 = 15$ GHz, the magnitudes of the measured waves a_6 and b_6 are almost equal resulting in the impedance at the edge of the Smith chart, as shown in Fig. 6. Therefore the sensitivity of the impedance to variations of the reflection coefficient $\Gamma = a_6/b_6$ is larger at 15 GHz than at 5 and 10 GHz, where the measured impedance is close to 50 Ω. In order to show that the measured incident and scattered waves at $3f_0$ fall well within the dynamic

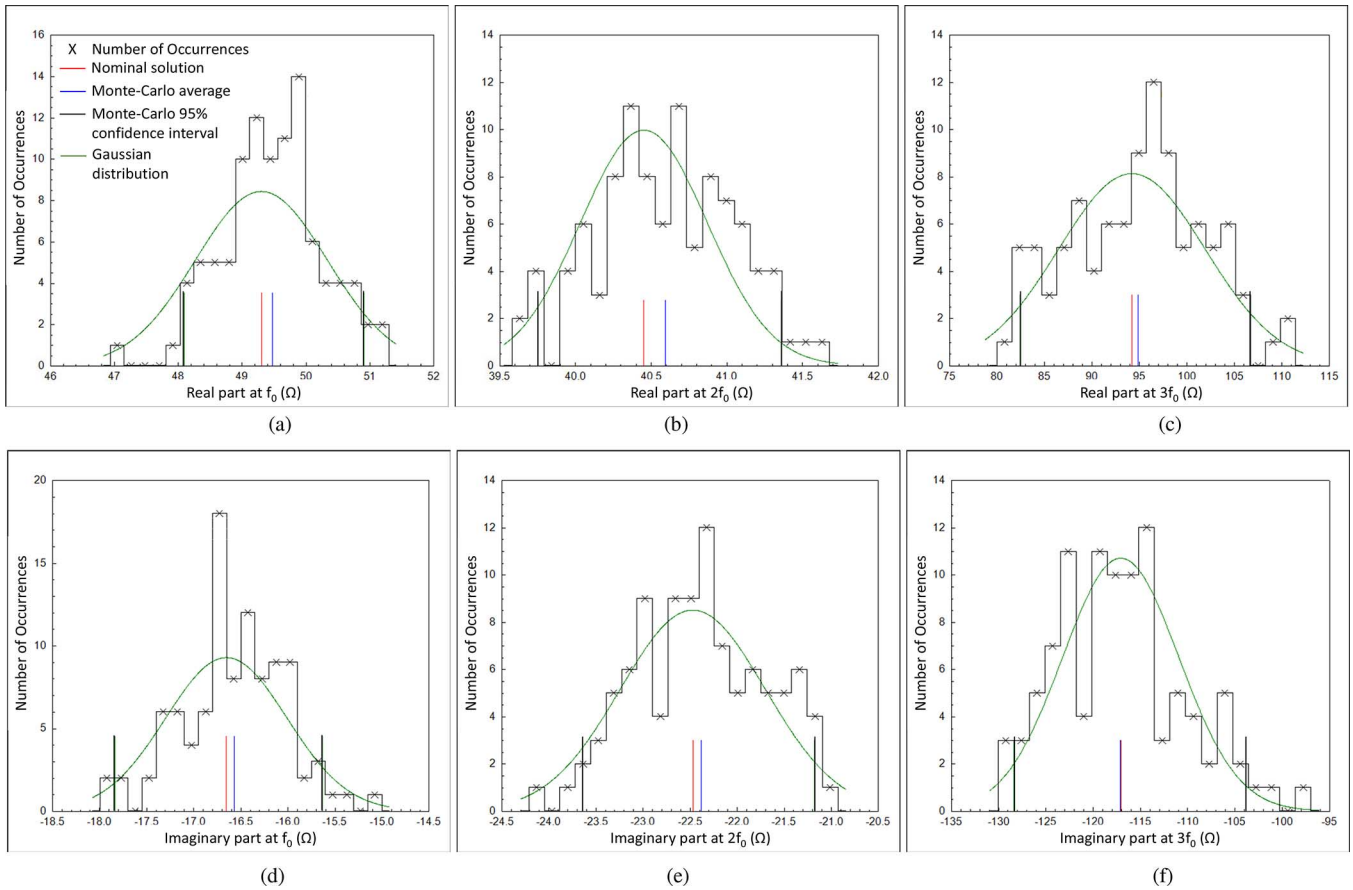


Fig. 8. Histogram of Monte Carlo simulations and distribution from sensitivity analysis of the: (a)–(c) real and (d)–(f) imaginary part of the load impedance at the current-generator plane at f_0, $2f_0$, and $3f_0$. The blue and the red line (in the online version) are the nominal value and the average from 100 Monte Carlo simulations, respectively.

TABLE VII
COMBINED AND INDIVIDUAL UNCERTAINTY CONTRIBUTIONS IN THE REAL AND IMAGINARY PART OF THE IMPEDANCES AT THE TRANSISTOR CURRENT-GENERATOR PLANE

	$Re\{Z^{CGP}(f_0)\}$ (Ω)	$Im\{Z^{CGP}(f_0)\}$ (Ω)	$Re\{Z^{CGP}(2f_0)\}$ (Ω)	$Im\{Z^{CGP}(2f_0)\}$ (Ω)	$Re\{Z^{CGP}(3f_0)\}$ (Ω)	$Im\{Z^{CGP}(3f_0)\}$ (Ω)
TOTAL	1.032	0.643	0.419	0.770	7.718	6.167
TRL	1.012	0.640	0.339	0.763	7.17	5.390
SOLT	0.001	0.001	0.010	0.006	0.563	0.480
POWER METER	0.014	0.002	0.084	0.081	1.328	2.394
COMB-GENERATOR REPEATABILITY	0.002	0.001	0.012	0.004	0.698	0.697
COMB-GENERATOR CHARACTERIZATION	0.002	0.001	0.024	0.015	1.559	1.342
PROBE ALIGNMENT	0.203	0.060	0.212	0.046	0.805	0.505
CABLE BENDING	0.001	0.001	0.002	0.232	0.114	0.232

TABLE VIII
COMBINED AND INDIVIDUAL UNCERTAINTY CONTRIBUTIONS IN THE REAL AND IMAGINARY PART OF THE IMPEDANCES AT $3f_0$ AT THE TRANSISTOR CURRENT-GENERATOR PLANE

	$W(L_1)$	$H(L_1)$	$W(L_2)$	$H(L_2)$	W(Reflect)	H(Reflect)	TOTAL
$Re\{Z^{CGP}(3f_0)\}$ (Ω)	2.026	5.321	0.855	2.201	2.559	2.559	7.718
$Im\{Z^{CGP}(3f_0)\}$ (Ω)	2.150	4.542	0.703	1.703	0.364	0.524	6.167

range of the instrument, their measured amplitudes are reported in Fig. 10.

Furthermore, we observe that the uncertainties in the impedances at the extrinsic and intrinsic planes are very similar. The largest difference occurs when propagating the uncertainties to the current-generator plane and when the impedance at the measurement plane significantly differs from 50 Ω. For the experimental conditions we considered, the impedance at f_0 and $2f_0$ is very close to 50 Ω at the extrinsic plane and its uncertainty does not change much when shifting it up to the current-gen-

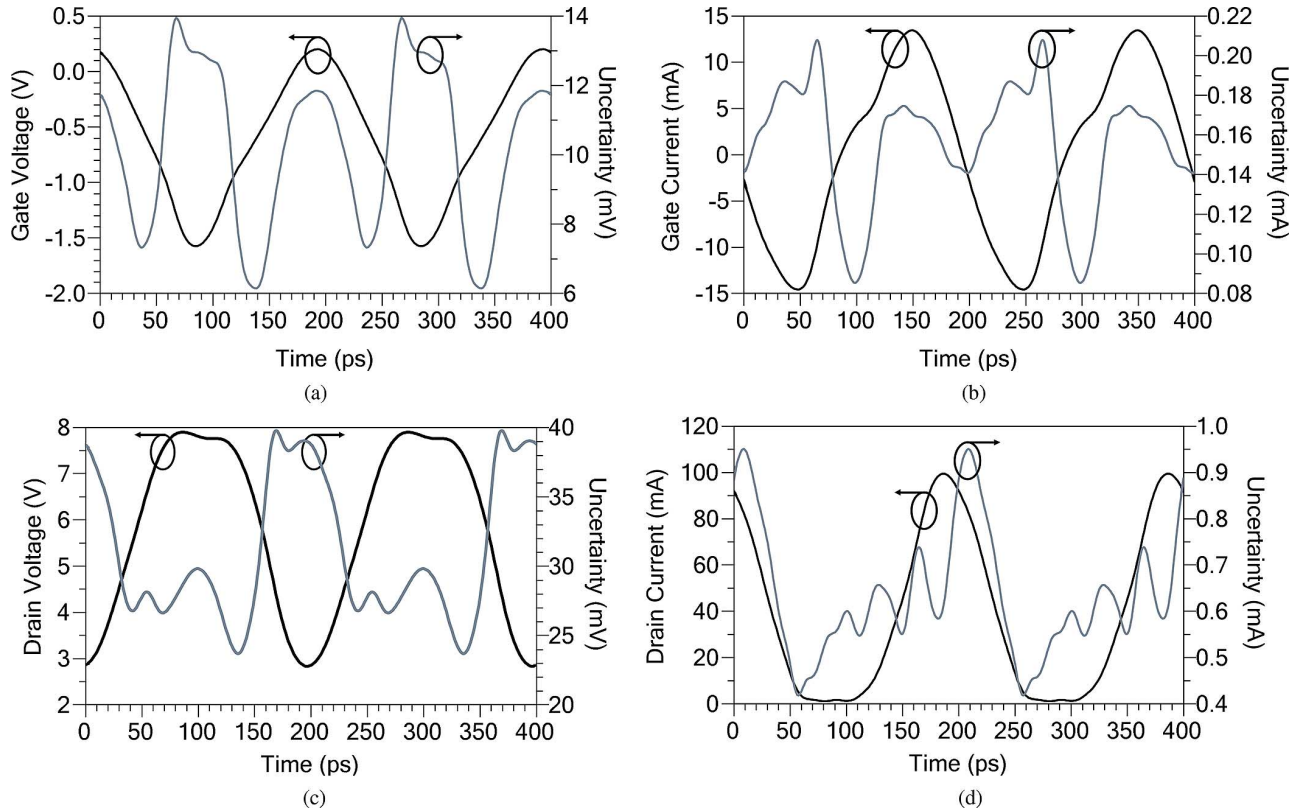


Fig. 9. (a) Gate voltage, (b) gate-current, (c) drain-voltage, and (d) drain-current time-domain waveforms at the current-generator plane at $V_{\mathrm{GS0}} = -0.6$ V, $V_{\mathrm{DS0}} = 6$ V, $f_0 = 5$ GHz, input power equal to 6 dBm, $Z_{\mathrm{CGP}}(f_0) = 49.3 - j16.6\ \Omega$, $Z_{\mathrm{CGP}}(2f_0) = 40.4 - \mathrm{j}22.4\ \Omega$, $Z_{\mathrm{CGP}}(3f_0) = 94.2 - \mathrm{j}117.1\ \Omega$. Nominal solution (black line) and standard uncertainty (grey line).

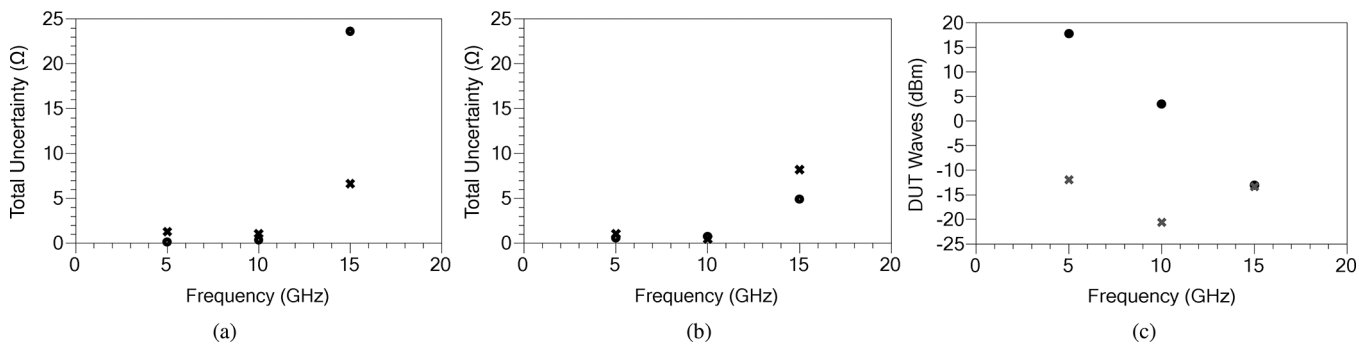


Fig. 10. Total uncertainty in the impedance at: (a) the extrinsic plane and (b) current generator plane at f_0, $2f_0$, and $3f_0$. Real part (crosses) and imaginary part (circles). In (c), the nominal value of the amplitude of the corrected waves a_6 (crosses) and b_6 (circles) at the transistor terminals.

erator plane. The largest change is observed when shifting the impedance at $3f_0$ from the extrinsic plane to the current-generator plane.

Therefore, evaluating the uncertainties in the measured extrinsic impedances may not be sufficient to correctly estimate uncertainties in the corresponding impedances at the current-generator plane.

This is important since the design approaches based on waveform engineering search for the desired operating condition at the current-generator plane by experimentally tuning the impedances at microwave frequencies at the transistor terminals, i.e., the extrinsic plane. In many situations, the impedances needed to obtain the desired performance are very different from the reference impedance. Therefore, nonlinear de-embedding is essential not only to correctly determine the impedances at the current-generator plane, but also to correctly know the uncertainty at the current-generator plane.

VI. Conclusion

We evaluated the uncertainties in on-wafer vector-calibrated nonlinear measurements with the NIST Microwave Uncertainty Framework. The residual uncertainties in the calibration procedure were first propagated to the temporal voltage and current waveforms at the transistor terminals. Next we propagated the uncertainties in the calibrated waves at the transistor terminals to the temporal current and voltage waveforms and the impedances at the transistor current-generator plane. These electrical quantities, which represent the measurands of our anal-

ysis, cannot be measured directly at microwave frequencies as they are masked by the transistor's parasitic network and intrinsic nonlinear capacitances. A nonlinear de-embedding procedure is therefore needed if one wants to correctly retrieve the current-generator plane electrical quantities with their uncertainty.

We included in our analysis uncertainties in the passive calibration standards, power meter, NIST traceable phase calibration reference, cable bending, and probe alignment.

Other sources of uncertainties can be added in a straightforward manner.

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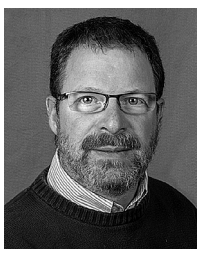

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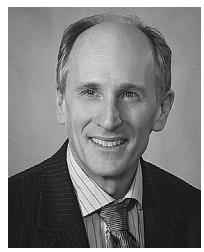

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