Physics-based Electro-thermal Saber Model and Parameter Extraction for High-Voltage SiC Buffer-Layer IGBTs†

T. H. Duong[1], A. R. Hefner[1], J. M. Ortiz-Rodríguez[1]
[1]Semiconductor and Dimensional Metrology Division
National Institute of Standards and Technology
Gaithersburg, MD 20899, USA
tam.duong@nist.gov

S.-H. Ryu[2], Edward Van Brunt[2], Lin Cheng[2],
Scott Allen[2], John W. Palmour[2]
[2]Cree, Inc.
Durham, NC 27703, USA

***Abstract*— The purpose of this paper is to present a physics-based electro-thermal Saber®* model and parameter extraction sequence for high-voltage SiC buffer layer n-channel insulated gate bipolar transistors (IGBTs). This model was developed by modifying and extending the previously developed physics-based silicon buffer layer IGBT electro-thermal model and IGBT Model Parameter extrACtion Tools (IMPACT) to include SiC specific device and material properties. The validated simulation results in this paper demonstrate that the new electro-thermal Saber® model for high-voltage SiC buffer layer n-channel IGBTs can be used to describe the static and dynamic behaviors for a wide range of device designs and circuit conditions for IGBTs with blocking voltages from 12 kV to 20 kV. The new physics-based model provides both device and circuit predictive capability.**

I. INTRODUCTION

Silicon carbide (SiC) has emerged as a material of choice for the next generation of high-voltage power semiconductor devices. The primary advantage of the SiC material for power devices is that it has an order of magnitude higher breakdown electric field (2×10^6 V/cm to 4×10^6 V/cm) and a higher temperature capability than conventional silicon materials [1]. The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of silicon devices) and more highly doped (more than 10 times higher) voltage-blocking layers. For minority carrier conductivity modulated devices such as PiN diodes or IGBTs, the voltage blocking layer of 0.1 times the thickness of a silicon device can result in a factor of 100 times faster switching speed. This is possible because the diffusion length, L, required to modulate the conductivity of the blocking layer can also be reduced to 1/10th the value required for a Si device with the same blocking voltage, thus permitting the reduction of the lifetime, τ, by a factor of 100 according to $L = \sqrt{D\,\tau}$, where D is the diffusion coefficient.

Recently, ultra high-voltage (from 12 kV to 22 kV) 4H-SiC buffer layer n-channel IGBTs (N-IGBT) with an active area of 0.16 cm^2 for the 12 kV device and 0.37 cm^2 for the 20 kV device have shown superior characteristics such as a differential on-state resistance (Ron,sp,diff) of 5.3 mΩ-cm^2 for the 12 kV device at a gate bias of 20 V [2]. The purpose of this work is to present an electro-thermal Saber® model and parameter extraction sequence for this new class of high-voltage SiC buffer layer N-IGBTs. The validated results shown in this work demonstrate that the developed electro-thermal Saber® model can be used to describe the static and dynamic behaviors of the 12 kV and 20 kV 4H-SiC buffer layer N-IGBT.

II. HIGH VOLTAGE 4H-SIC BUFFER LAYER N-IGBT STRUCTURE

Fig. 1 shows simplified cross-sections of the 4H-SiC buffer layer N-IGBT [2]. As an example, the 12 kV N-IGBTs studied in this work utilize a $2x10^{14}$ cm^{-3} doped, 140 μm thick N-type epilayer as the drift layer, and have N-type field-stop buffer layers with doping concentrations ranging from $1x10^{17}$ cm^{-3} to $5x10^{17}$ cm^{-3}. The P+ 4H-SiC substrate serves as the electron injector layer for the N-IGBTs. The field-stop buffer layers in the N-IGBTs have thicknesses ranging from 2 μm to 10 μm. The MOS channel length, defined by the distance between the edge of the P-well to the edge of the N+ source region for N-IGBTs, is approximately 1 μm. SiO_2 layers with an approximate thickness of 50 nm were thermally grown on N-IGBTs, for gate dielectric. Similarly, the 20 kV IGBTs utilize a $2x10^{14}$ cm^{-3} doped, 180 μm thick N-type epilayer as the drift layer, and have N-type field-stop buffer layers with doping concentrations in the range of ranging of 1 ~ $5x10^{16}$ cm^{-3} and thicknesses in the range 2 μm [3].

† Contribution of NIST, not subject to copyright. The devices discussed in this paper were produced by Cree Inc. and funded by U.S. Army Research Laboratory located at Adelphi, MD, USA.

* Saber® mixed-technology system simulation software is a registered trademark of Synopsys®, Inc. Certain commercial products or materials have been identified in order to specify or describe the subject matter of this paper adequately. This does not imply recommendation or endorsement by the NIST, nor does it imply that the products are the best for the purpose.

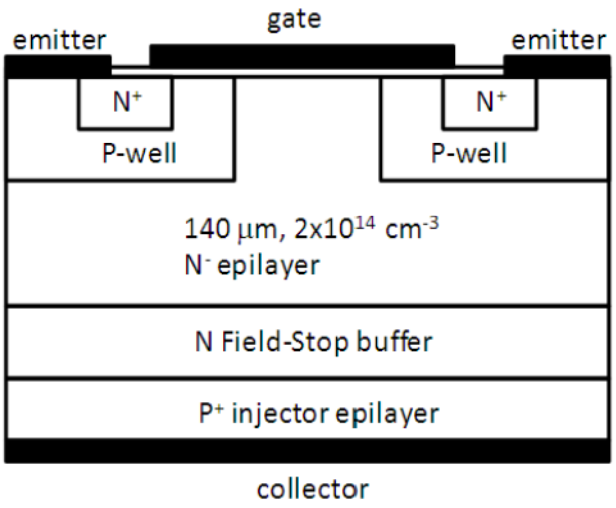

Fig. 1: Simplified cross-sections of the 12 kV 4H-SiC buffer layer N-IGBT.

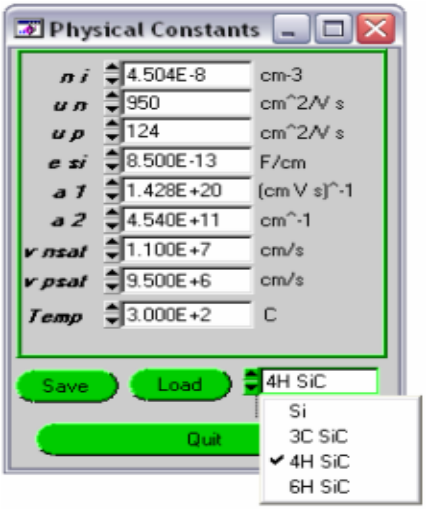

Fig. 2: Temperature dependent material parameters for 4H-, 6H-, and 3C-SiC was added to SiC--IMPACT extraction tools.

III. IMPLEMENTATION OF HIGH-VOLTAGE 4H-SIC BUFFER LAYER N-IGBT MODEL INTO THE SABER® CIRCUIT SIMULATOR

The previously developed silicon buffer layer IGBT model was implemented into the Saber® circuit simulator using the Saber® MAST modeling language [4, 5]. In this work, the model is extended to include the device and material properties of SiC by incorporating the material properties described in [6, 7] into the models described in [4, 5]. To implement the high voltage 4H-SiC buffer layer N-IGBT electro-thermal model into the Saber® circuit simulator, the nonlinear functions of the system variables listed in Table I as in [4] and the power MOSFET equations listed in Table II as in [7] are combined. The new extended model can be used to describe the static and dynamic behaviors for both Si and 4H-SiC buffer layer N-IGBT.

IV. HIGH-VOLTAGE 4H-SIC BUFFER LAYER N-IGBT PARAMETER EXTRACTION

Previously, a software package called IGBT Model Parameter extrACtion Tools (IMPACT) [6, 8] for extracting parameters of silicon IGBTs was extended to include SiC power MOSFETs in a software package called SiC—IMPACT [7]. In this work, the SiC-IMPACT software tools are extended to include features that are needed for SiC IGBTs, including an alternate Tau-Effective-Extraction Program (TAUEFFMSR) to extract the base lifetime (τHL) and buffer-layer lifetime (τbuf) model parameters. These tools are now capable of extracting the 20 physical and structural parameters of the physics-based Hefner IGBT and power MOSFET models for both Silicon and SiC.

To perform the parameter extraction, the material type is first selected as demonstrated in Fig.2, and then the extraction steps are performed in the order that they are listed in the subsections below.

A. τHL and τbuf Extraction (TAUEFFMSR)

The new TAUEFFMSR program is used to perform the extraction of τHL and τbuf by using the measured data directly from the inductive load turn-off switching measurements. Figs. 3-8 show the front panel and sub-panels of the TAUEFFMSR program.

Fig. 3 shows the front panel of the TAUEFFMSR program with measured current and voltage waveforms of inductive load turn-off switching at an IGBT anode current of 16 A, clamp voltages of 1 kV to 8 kV, and at an IGBT temperature of 25 °C. The program allows the user to load any complete set of measurements into memory, but it can also suppress the display of waveforms that the user may not be manually processing at the moment during the parameter extraction. This facilitates the analysis of each {temperature, voltage, current} set of measurements individually by displaying only the data of interest to the user.

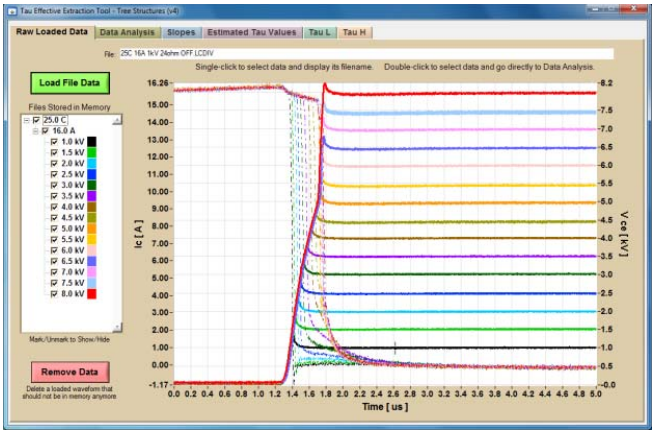

Fig. 3: Front panel of the TAUEFFMSR program showing measured current and voltage waveforms of inductive load turn-off switching at 16 A, and 1 kV to 8 kV at 25 °C.

After loading all the desired inductive load turn-off switching measured data into the program as demonstrated in Fig. 3, the user then selects a particular waveform to extract the effective lifetime (τeff) at that clamp voltage by double-click a voltage waveform. Figs. 4 to 6 show the pop-up panels of the TAUEFFMSR program used to extract the lifetime parameters form the effective lifetime versus clamp voltage.

To extract the effective lifetime from the current waveform at a given clamp voltage, the user selects the portion of the voltage waveform in the *Data Analysis* tab as shown in Fig. 4, where the behavior resembles an exponential decay. The program provides controls and smoothed data curves to refine the process of fitting the data when too much noise or oscillations are present. The lower graph in Fig. 5 aids in the visualization of this effective lifetime extraction by allowing the comparison of the natural log curves of data and exponential fit.

Fig. 6 shows the extracted τeff values versus clamp voltage at 16 A and 25 ^{o}C. To obtain this curve, the process shown in Fig. 4 is repeated for all the measured voltage levels at each temperature. Fig. 6 is then used to extract the values of the high-doped base (HDB) and low-doped base (LDB) lifetime versus temperature. Fig. 7 shows the comparison of measured values of τeff versus clamp voltage with extraction curve [4] used to obtain HDB and LDB lifetimes. Fig. 8 shows the extracted values of the HDB and LDB lifetimes versus temperature, compared with the temperature dependent model for these parameters that is used within the Hefner IGBT model.

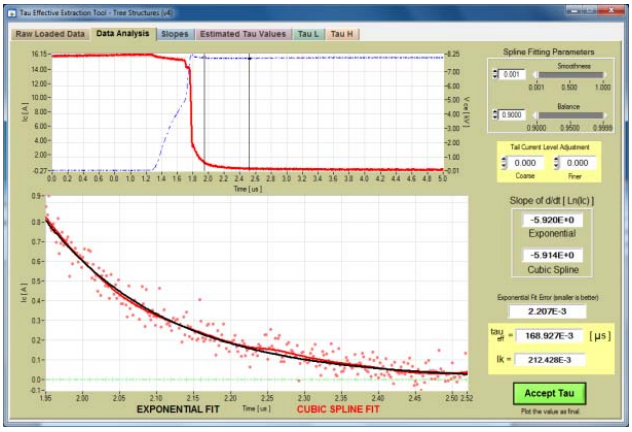

Fig. 4: A pop-up panel of the TAUEFFMSR program showing the tail current section used to extract effective lifetime (τeff) at a clamp voltage of 8 kV. The solid red and black curves are the cubic spline fit and exponential fit, respectively.

Fig. 5: A pop-up panel of the TAUEFFMSR program showing the natural log of the tail current that is used to extract τeff.

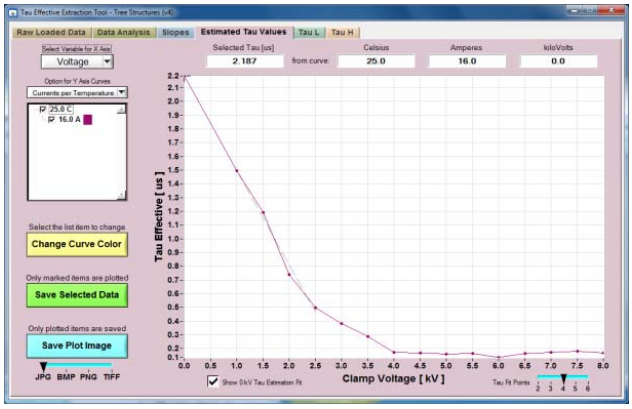

Fig. 6: A pop-up panel of the TAUEFFMSR program showing the τeff values versus clamp voltage at 16 A and 25 ^{o}C.

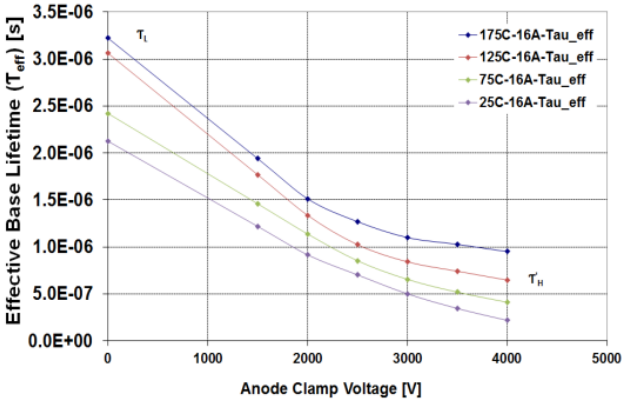

Fig. 7: Comparison of measured values of τeff versus clamp voltage with a model using parameters extracted from TAUEFFMSR.

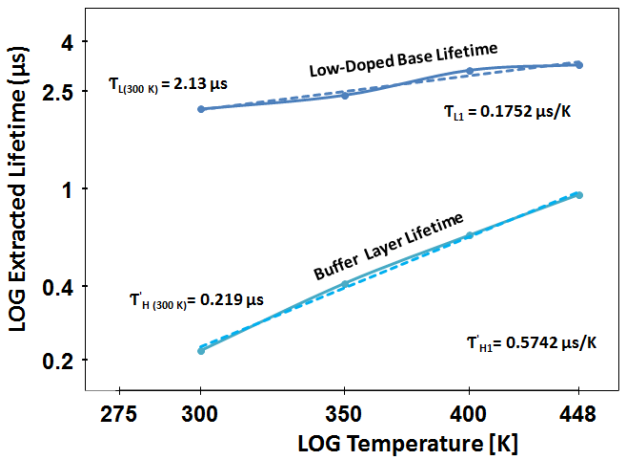

Fig. 8: Extracted values of the HDB and LDB lifetime versus temperature extracted using TAUEFFMSR.

B. Isne, Wb, Nb, Wbuf Extraction (BTAMSR & DIMPACT)

The value of the Nb parameter for SiC IGBTs is extracted using the Capacitance-Voltage (CV) program, included in the automated software package called Diode Model Parameter extrACtion Tools (DIMPACT) as described in [9] rather than using the BTAMSR program as described in [6]. The parameters Wb and Wbuf are extracted as described in [6].

C. VT, Kpsat, □, Kfl, dVTl Extraction (SATMSR)

Figs. 9 and 10 show the SATMSR front panel and the final fit window demonstrating extraction of low- and high-current saturation region parameters, respectively. In SATMSR, the saturation current versus VGS is used to extract VT, KP, low current transconductance factor (KFL), low current threshold voltage differential (dVTL), and the temperature coefficients of threshold voltage (VT1) and transconductance (KP1) [5].

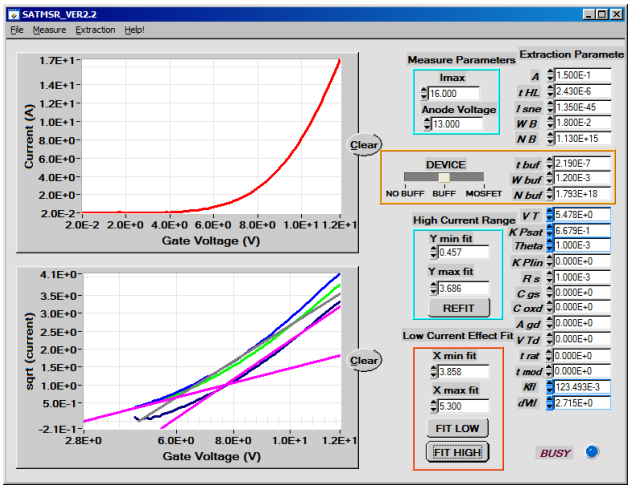

Fig. 9: SATMSR front panel demonstrating extraction of Kp, VT, □, Kfl, and dVTl.

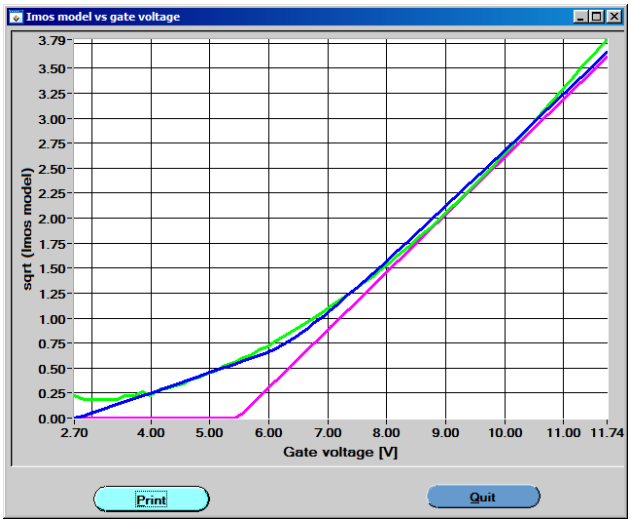

Fig. 10: SATMSR final fit window demonstrating low- and high-current fit.

D. Kplin, Rs, τrat, τmod Extraction (LINMSR)

Fig. 11 shows the front panel of the LINMSR extraction program. In this program, the on-state voltage versus VGS for a constant current is used to extract KPlin, KPlin1, RS, NB. The values of KPlin, KPlin1, RS, and NB parameters are calculated from the model equations [6-8] that are valid for the linear region. In this LINMSR program the values of the parameters extracted from the SATMSR program are used as known values in the equations.

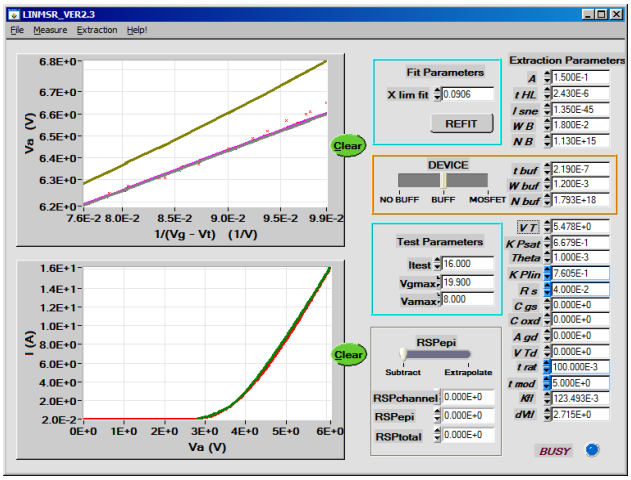

Fig. 11: LINMSR front panel demonstrating extraction of Kf, Rs, and Nb.

E. Cgs, Coxd, Agd, VTd, Nbuf Extraction (CAPMSR)

Fig. 12 shows the front panel for the CAPMSR program. The CAPMSR program measures gate and gate-drain charge characteristics for negative and positive gate voltages to extract CGS, COXD, AGD, and VTD.

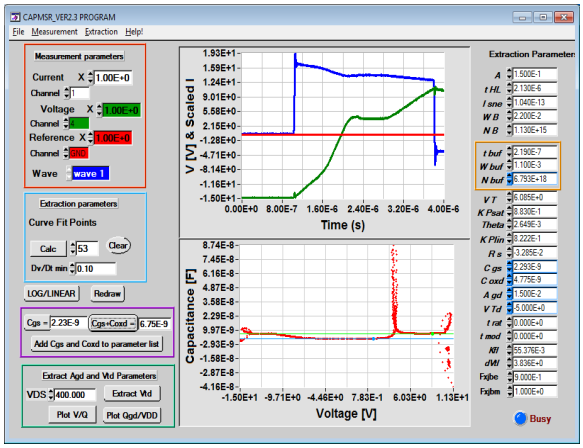

Fig. 12: CAPMSR front panel demonstrating the extraction of Cgs, Coxd, Agd, and VTd.

V. MEASURED AND SIMULATED RESULTS

A. 12 kV 10 A SiC buffer layer N-IGBT

Figs. 13 and 14 show the 12 kV, 10 A SiC buffer layer N-IGBT model (solid) compared with measured (dashed) output characteristics at 25 °C and 175 °C, respectively.

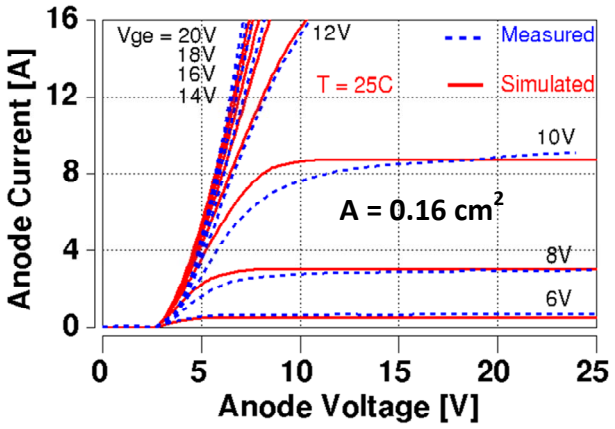

Fig. 13: Measured (dashed) and simulated output characteristics of a 12 kV, 10 A 4H-SiC buffer layer N-IGBT at 25 °C.

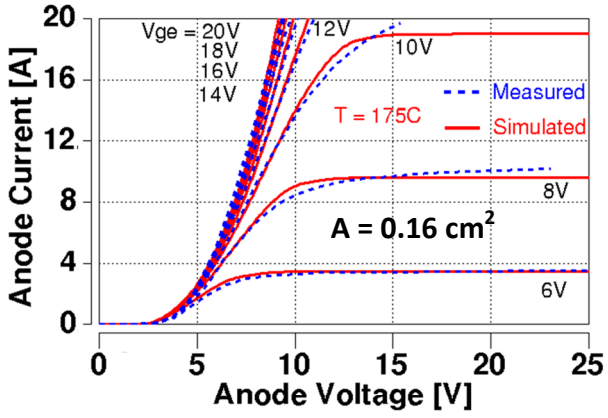

Fig. 14: Measured (dashed) and simulated output characteristics of a 12 kV, 10 A 4H-SiC buffer layer N-IGBT at 175 °C.

Figs. 15 and 16 compare the measured (dashed) and simulated (solid) anode current and anode voltage waveforms for clamped inductive load switching at different clamp voltages for the 12 kV, 10 A SiC buffer layer N-IGBT at a switching current of 16 A, gate resistor of 24 Ω, and IGBT temperatures of 25 °C and 175 °C, respectively.

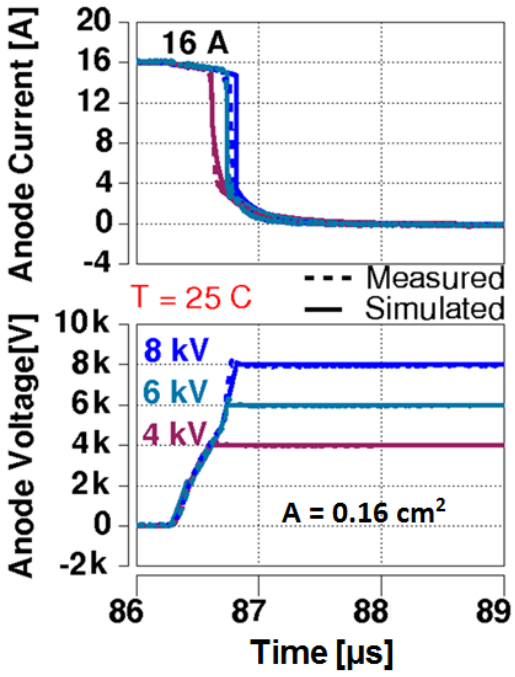

Fig. 15: Measured (dashed) and simulated (solid) anode current and anode voltage waveforms for different inductive load turn-off clamp voltages for a 12 kV, 10 A 4H-SiC buffer layer N-IGBT at 25 °C.

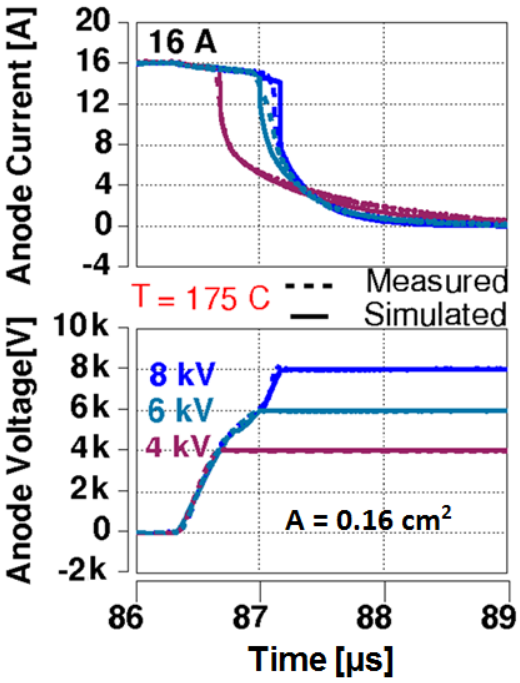

Fig. 16: Measured (dashed) and simulated (solid) anode current and anode voltage waveforms for different inductive load turn-off clamp voltages for a 12 kV, 10 A 4H-SiC buffer layer N-IGBT at 175 °C.

Figs. 17 and 18 compare the measured (dashed) and simulated (solid) anode current and anode voltage waveforms for clamped inductive load switching at three different switching currents (i.e., 8 A, 12 A, and 16 A) for the 12 kV, 10 A SiC buffer layer N-IGBT at the clamped voltage of 8 kV, gate resistor of 24 Ω, and IGBT temperatures of 25 °C and 175 °C, respectively.

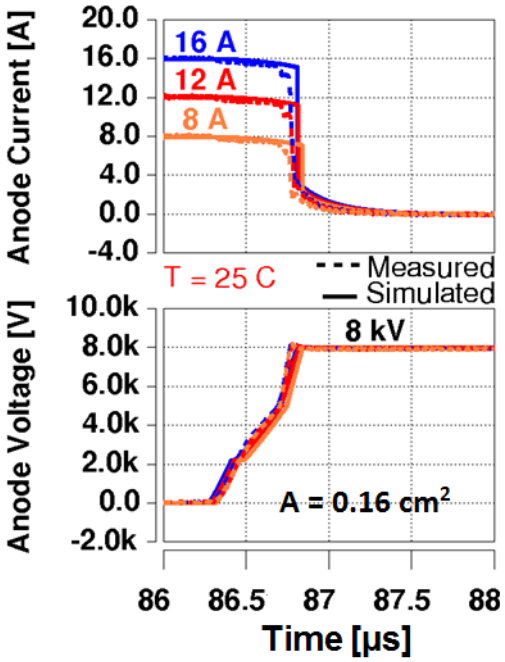

Fig. 17: Measured (dashed) and simulated (solid) anode current and anode voltage waveforms for different collector currents for a 12 kV, 10 A 4H-SiC buffer layer N-IGBT at 25 °C.

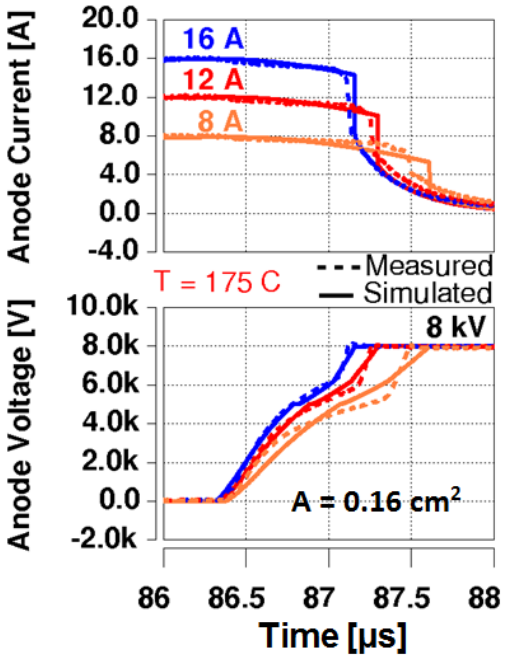

Fig. 18: Measured (dashed) and simulated (solid) anode current and anode voltage waveforms for different collector currents for a 12 kV, 10 A 4H-SiC buffer layer N-IGBT at 175 °C.

B. 20 kV 20 A SiC buffer layer N-IGBT

Figs. 19 and 20 show the 20 kV, 20 A SiC buffer layer N-IGBT model (solid) compared with measured (dashed) output characteristics at 25 °C and 175 °C, respectively.

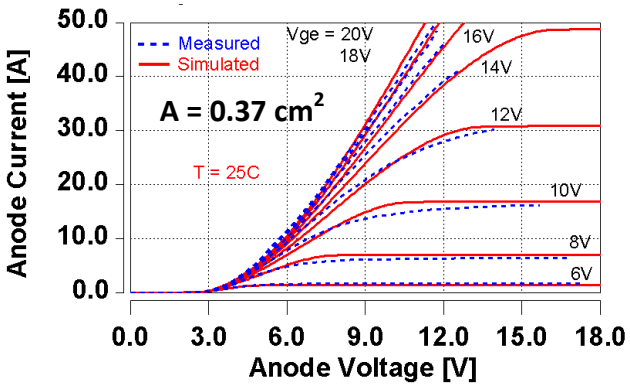

Fig. 19: Measured (dashed) and simulated output characteristics of a 20 kV, 20 A 4H-SiC buffer layer N-IGBT at 25 °C.

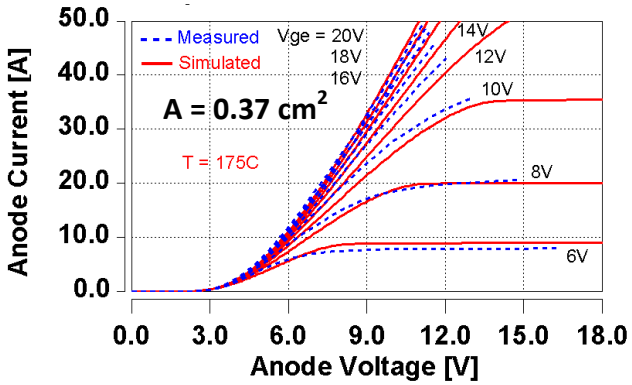

Fig. 20: Measured (dashed) and simulated output characteristics of a 20 kV, 20 A 4H-SiC buffer layer N-IGBT at 175 °C.

Figs. 21 and 22 compare the measured (dashed) and simulated (solid) anode current and anode voltage waveforms for clamped inductive load switching at different clamp voltages for the 20 kV, 20 A SiC buffer layer N-IGBT at a switching current of 50 A, gate resistor of 5.5 Ω, and IGBT temperatures of 25 °C and 175 °C, respectively.

Figs. 23 and 24 compare the measured (dashed) and simulated (solid) anode current and anode voltage waveforms for clamped inductive load switching at three different switching currents (i.e., 30 A, 40 A, and 50 A) for the 20 kV, 20 A SiC buffer layer N-IGBT at the clamped voltage of 8 kV, gate resistor of 5.5 Ω, and IGBT temperatures of 25 °C and 175 °C, respectively.

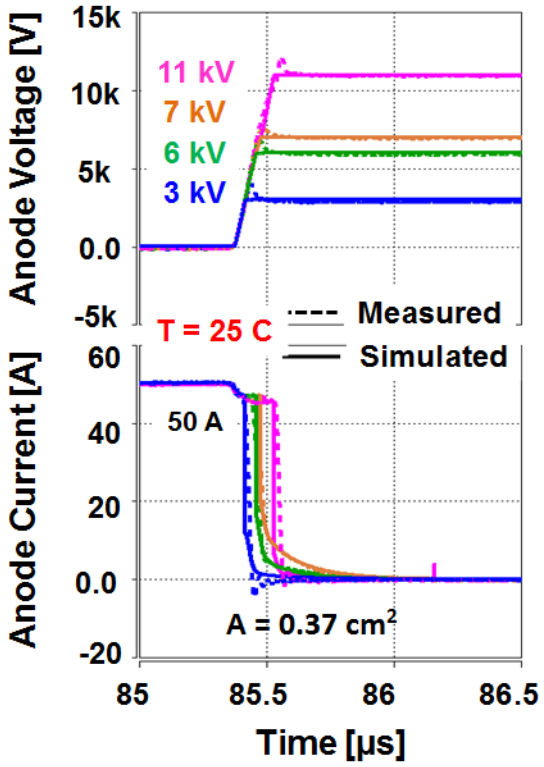

Fig. 21: Measured (dashed) and simulated (solid) anode current and anode voltage for different inductive load turn-off clamp voltages for a 20 kV, 20 A 4H-SiC buffer layer N-IGBT at 25 °C.

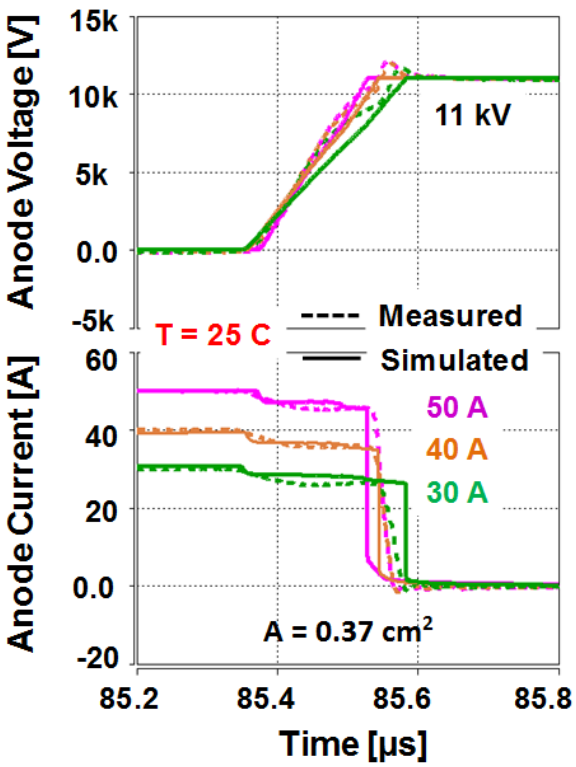

Fig. 23: Measured (dashed) and simulated (solid) anode current and anode voltage for different collector currents for a 20 kV, 20 A 4H-SiC buffer layer N-IGBT at 25 °C.

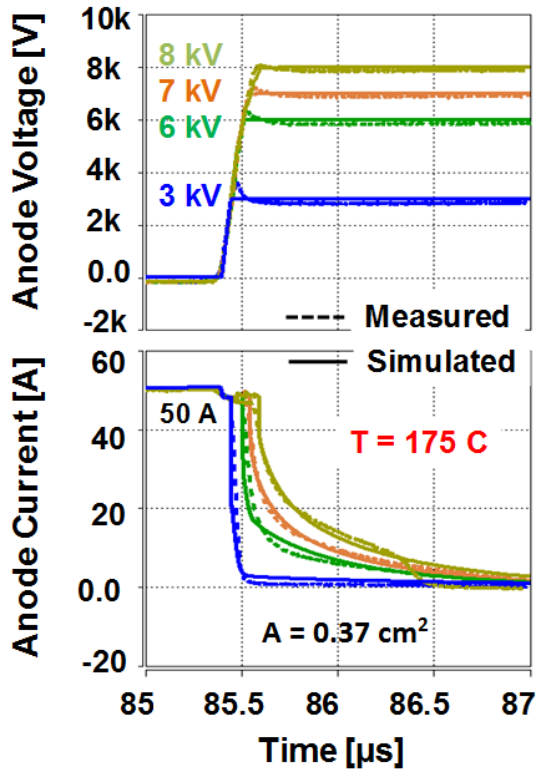

Fig. 22: Measured (dashed) and simulated (solid) anode current and anode voltage for different inductive load turn-off clamp voltages for a 20 kV, 20 A 4H-SiC buffer layer N-IGBT at 25 °C.

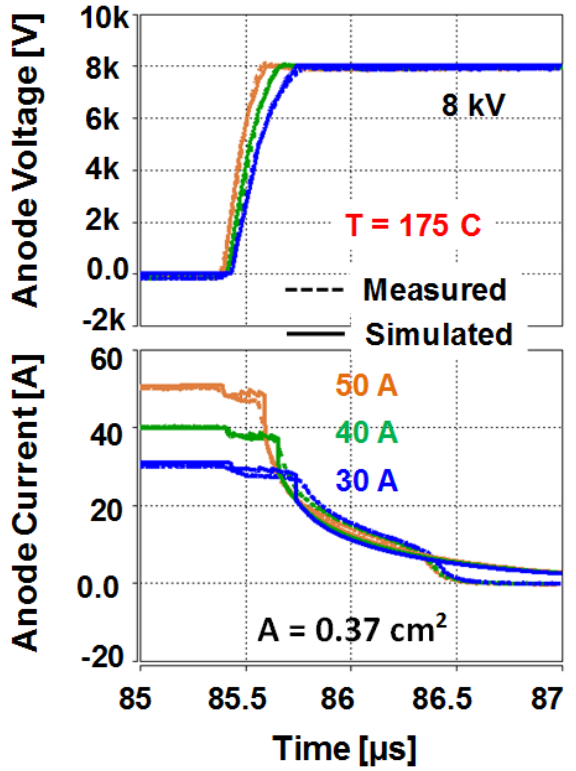

Fig. 24: Measured (dashed) and simulated (solid) anode current and anode voltage for different collector currents for a 20 kV, 20 A 4H-SiC buffer layer N-IGBT at 175 °C.

VI. CONCLUSIONS

This paper presents a new electro-thermal model implemented in the Saber® circuit simulator and an extraction sequence for high-voltage SiC buffer layer IGBT devices. The results for 12 kV, 10 A and 20 kV, 20 A devices indicated that the developed electro-thermal Saber® model can be used to accurately simulate the circuit performance of the new device types. Since the model is physics-based and parameterized in terms of structural and physical parameters, the model also provides a predictive device design capability for the new SiC IGBT devices.

REFERENCES

[1] Hefner Jr. A. R., Sei-Hyung, R., Brett H., Berning D. W., Hood C. E., Ortiz-Rodriguez J. M., Rivera-Lopez A., Duong T., Akuffo A., Hernandez M.,"Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Device," Proceedings of the 2006 IEEE Industry Applications Society (IAS) Annual Meeting, October 08-12, 2006, Tampa, FL, pp. 330-337.J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.

[2] Sei-Hyung Ryu, Lin Cheng , Sarit Dhar, Craig Capell, Charlotte Jonas, Allen Hefner, Michael O'Loughlin, Al Burk, Anant Agarwal, and John Palmour, Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs June 3-7 2012 - Bruges, Belgium, pp. 257-260.

[3] E. V. Brunt, L. Cheng, M. O'Loughlin, C. Capell, C. Jonas, , K. Lam, J. Richmond, V. Pala, S. Ryu, S. T. Allen, A. A. Burk, and J. W. Palmour, "22 kV, 1 cm2, 4H-SiC n-IGBTs with Improved Conductivity Modulation," Proceedings of the 2014 26th International Symposium on Power Semiconductor Devices, June 15-19, 2014 Waikoloa, Hawaii. Pp. 358-361.

[4] A. R. Hefner, "Modeling buffer layer IGBTs for circuit simulation," Power Electronics, IEEE Transactions on Volume 10, Issue 2, March 1995, pp. 111-123.

[5] A. Hefner, "A Dynamic Electro-Thermal Model for IGBT," in IEEE Transactions on Industry Applications, vol.30, no. 2, (1994).

[6] Ty R. McNutt, Allen R. Hefner, H. Alan Mantooth, David Berning, and Sei-Hyung Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence." IEEE Transactions On Power Electronics, Vol. 22, No. 2, March 2007, pp. 353-363.

[7] Duong T., Hefner Jr. A. R., and Berning D. W., "Automated Parameter Extraction Software For High-Voltage, High-Frequency SiC Power MOSFETs," Proceedings of the 2006 IEEE Workshop on Computers in Power Electronics (COMPEL), July 16-19, 2006, Troy, NY, pp. 205-211.

[8] Hefner, A., Jr.; Bouche, S., "Automated parameter extraction software for advanced IGBT modeling,"Computers in Power Electronics, 2000. COMPEL 2000. The 7th Workshop on 16-18 July 2000, pp. 10-18.

[9] N. Yang, T. Duong, J.O. Jeong, J. Ortiz, A. R. Hefner, K. Meehan, "Automated Parameter Extraction Software for Silicon and High-Voltage Silicon Carbide Power Diodes" Proceedings of the IEEE COMPEL Workshop 2010, IEEE COMPEL 2010, Boulder, CO, United States, 06/28/2010 to 06/30/2010, 8 pp., (24-Jun-2010).