Device-Level Experimental Observations of NBTI-Induced Random Timing Jitter

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***Abstract*—This paper utilizes device-level eye-diagram measurements to examine negative bias temperature instability (NBTI)-induced changes in timing jitter at circuit speeds. The measured jitter is examined for a variety of ring oscillator and pseudo-random gate patterns. The ring oscillator patterns were chosen to mimic typical NBTI reliability characterizations, whereas the pseudorandom patterns act as an approximation for real-world random logic. Our observations indicate that NBTI-induced jitter is gate pattern dependent and most severe for the pseudorandom case. Collectively, this paper strongly suggests that typical NBTI ring oscillator characterization methods are insensitive to random logic timing jitter.**

***Index Terms*—Eye diagram, jitter, NBTI, reliability.**

I. Introduction

THE negative bias temperature instability (NBTI) is, most notably, the dominant wear-out mechanism in p-channel devices [1]–[3]. Investigations into this elusive phenomenon typically employ a wide array of clever device-level (or simple ring oscillator) measurements designed to monitor stress-induced parametric (or frequency) shifts [4]–[11]. Through careful calibrations, these parametric or frequency shifts are translated to the circuit environment in an attempt to provide estimates of circuit lifetimes [4], [7], [10], [11]. This approach has led to several successful embodiments which link parametric drift to circuit timing shifts [4], [7], [10], [11].

While this methodology clearly has merit, recent reports in highly-scaled devices link NBTI to a random, fast charge trapping/de-trapping mechanism [3]. The areal averaging associated with this, seemingly random, charge trapping/de-trapping in larger devices has been shown to correlate with the observed parametric drift/circuit timing shifts [12]. However, in highly-scaled devices (no area averaging), it follows that charge trapping/de-trapping should instead introduce parametric variability [12] and a subsequent increase in circuit timing *jitter*. Increases in timing jitter are more troubling than timing shifts due to their random nature [13]. In the absence of jitter considerations, a well calibrated circuit timing shift can be mitigated and compensated via circuit design [14]. However, increases in circuit timing jitter necessitate increased guard banding at the cost of performance [13]. This troubling circuit consequence of NBTI-induced charge trapping/de-trapping is very difficult to predict and quantify due to the vast gaps between device-level NBTI characterization data and real-world random logic circuit environments.

Real-world circuit environments introduce *random* logic patterns which present effective NBTI stress/recovery times spanning 10^{-10} to 10^{6} s. The most comparable current NBTI characterizations monitor parametric drift due to a regular duty cycle (ring oscillator-like) stress/recovery pattern of period $\approx 10^{-6}$ s [6]. As mentioned above, these device/simple circuit level measurements *do* provide an avenue to predict NBTI-induced circuit timing *shifts*. However, they are *ill-equipped to gauge* NBTI-induced random timing *jitter*. It is the aim of this study to bridge this gap (real-world circuits vs. device-level or simple ring oscillator characterizations) by using a custom high-speed experimental arrangement to measure eye-diagram derived timing jitter directly at the device level.

In this study we extend our recent observations [15] of NBTI-induced timing jitter using pseudo-random bit sequences designed to mimic a real-world random logic circuit environments. We demonstrate the utility of eye-diagram measurements to gauge stress-induced timing jitter increase. We also demonstrate that more conventional (ring oscillator-like) square waveforms (50% duty cycle) are insensitive to the NBTI-induced increases in timing jitter which are, presumably, present in random logic. Additional jitter measurements after a long-term recovery period, reveal a partial recovery in timing jitter degradation. Collectively, this work provides the impetus to generate NBTI measurements at the device-level which characterize not only parametric/circuit timing shifts, but also the parametric variability and consequent circuit timing jitter.

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II. Experimental Methods

A. Eye-Diagram Considerations

Typical device studies monitor NBTI-induced changes in threshold voltage (V_{th}), linear drain current (I_{dlin}), or saturation drain current (I_{dsat}) [3]. These parametric shifts necessarily introduce changes in the device transfer characteristics [14]. Eye diagram measurements are a convenient methodology to visualize the changes and directly extract their impact on timing [16], [17]. An eye diagram is constructed by repetitively

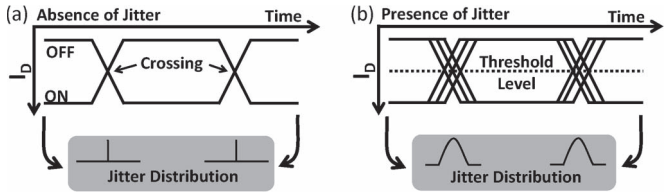

Fig. 1. Superimposing many sampled drain current transitions in response to an input bit sequence is used to construct an eye diagram. (a) In the absence of timing irregularities, the jitter distribution is essentially a delta function. (b) When irregularities are present, the jitter has some distribution corresponding to the device turning on and off at slightly different times for each bit.

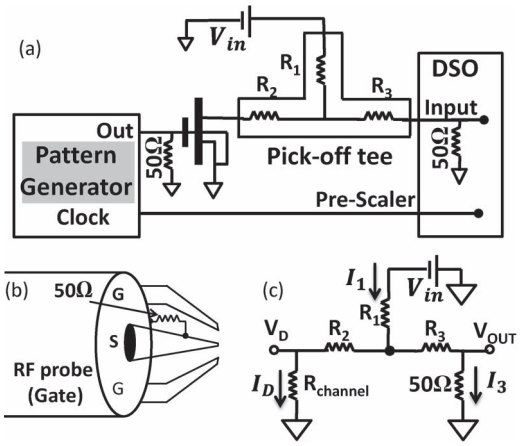

Fig. 2. (a) Schematic illustration of the measurement setup. (b) A high speed pattern generator provides the stress/sense bit sequence through a custom 50 Ω terminated probe. (c) Equivalent circuit of transient measurement on drain side.

superimposing the $I_D - V_G$ characteristic responses to a user-defined pulse train gate logic pattern [16], [17]. The drain current response to each "bit" of the logic pattern is overlaid such that the rising and falling edges intersect [16], [17]. This pattern is often referred to as the "eye." In the ideal-case (perfect device transfer characteristics), the eye-diagram rising and falling edges cross at a single point in time. This is illustrated in Fig. 1(a), and is often referred to as "eye-opening." In the presence of charge trapping/de-trapping, the rising and falling edges instead cross at a distribution of times (jitter distribution). This case is illustrated in Fig. 1(b), and is referred to as "eye-closing." Throughout the rest of this work, we monitor the NBTI-induced changes to the jitter distribution measured via eye-diagram measurements.

Eye diagram measurements are achieved using the experimental arrangement schematically shown in Fig. 2(a). The user defined pulse train is generated by a high-speed pattern generator with fixed rise and fall times $\approx$25 ps. The logic pattern is reliably transmitted to the gate electrode via an RF probe in a ground-signal-ground configuration. This specially designed probe has a micron-sized 50 Ω termination between the signal and ground connections [Fig. 2(b)]. The drain electrode is biased (V_D) via a "pick-off tee" and a voltage source (V_{in}). This experimental arrangement also facilitates measurement of the drain current response on the "output terminal" of the same pick-off tee. The measured response (V_{out}) is captured using a high-speed sampling oscilloscope with 50 Ω input impedance. Knowledge of the pick-off tee resistances (R_1, R_2, and R_3) allows for a direct correlation [Fig. 2(c)] between the measured

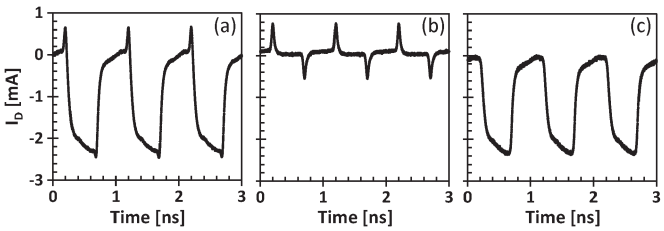

Fig. 3. Drain current response to a fast RO type bit sequence on the gate with drain biased (a) at −1 V and (b) at 0 volt. Subtracting (b) from (a) offers (c) a clean drain current response.

oscilloscope response (V_{out}) and the device drain current (I_D) as shown by:

$$I_D = \frac{V_{in} - V_{out}\left(\frac{R_3+50\ \Omega}{50\ \Omega}\right)}{R_1} - \frac{V_{out}}{50\ \Omega} \tag{1}$$

with

$$V_D = V_{out}\left(\frac{R_3}{50\ \Omega} + 1\right) - I_D R_2. \tag{2}$$

Note that as the transistor turns on, the reduction in channel resistance induces a V_D droop. Careful experimental calibrations ensure that this droop is insufficient for the device to leave the saturation regime, thus minimizing the effect.

Considering the extremely short time scales associated with the gate patterns utilized in this study, the parasitic components (device pad capacitance) must be well understood. Comprehensive measurements have been performed to quantify and mitigate the parasitics associated with the experimental arrangement (wafer probes, cabling, and most importantly the pick-off-tee. Minimizing these experimental parasitics is an absolute necessity to ensure suitable jitter measurements.

While our experimental arrangement is well optimized to ensure proper signal integrity, the parasitics of the device under test also play a role in these measurements. Fig. 3(a) illustrates the drain current response to a 2 Gb/s ring oscillator-like square waveform ($V_{on} = -1.30$ V, $V_{off} = 0.00$ V, $V_D = -1.0$ V) applied to the gate of a (2 nm/1 nm) HfO_2/SiO_2 p-channel device (10 μm × 0.18 μm). Fig. 3(b) illustrates the drain current response to the same gate waveform with $V_D =$ 0 V. At this low V_D, the drain current response is dominated by the charging/discharging parasitic gate pad. Correction of the operation drain current response, accomplished by subtracting the gate pad parasitic component, results in a proper drain current response [Fig. 3(c)] and is a strong indicator that the pad capacitance of these devices ($\cong$480 fF) dominates these measurements. Careful calibrations (not shown) were performed to identify the practical parasitic-derived rate limitation for the remainder of these measurements ($\leq$ 2 Gb/s). Note that, this limitation is entirely device layout dependent (not measurement equipment imposed). While it is seemingly trivial to remove the pad capacitance component from the time series data for illustrative purposes, it is considerably more difficult to remove the pad capacitance from the corresponding eye diagram as it requires an extremely memory intensive de-embedding process. The parasitic components result in overshoot/undershoot on the rising/falling edges of the eye diagram. These unavoidable transients do increase the floor of the jitter measurement. However,

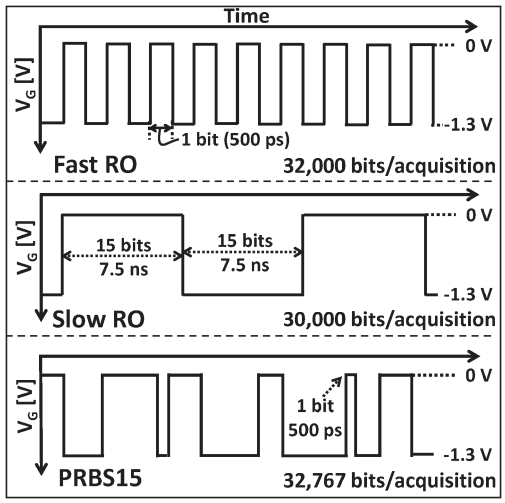

Fig. 4. The bit sequences used in this study for sensing the NBTI degradation. The three gate patterns are (a) fast RO, (b) slow RO, and (c) PRBS bit sequences. The PRBS sequence allows for the most realistic stress and jitter sense measurements possible as it closely mimics the environment experienced by real world digital logic gates.

NBTI-induced changes in the jitter distributions (Δjitter) are still quite reliable.

B. Sample Details and Gate Patterns

This study involves the same aforementioned (2 nm/1 nm) HfO_2/SiO_2 p-channel devices ($10\ \mu m \times 0.18\ \mu m$) with full ground-signal-ground layout. Each device was subject to a repetitive sequence as follows:

1) Measurement: consisting of both conventional $I_D - V_G$ characteristics as well as the construction of an eye-diagram from a specific gate pattern ~30 000 bits in length at 100 °C.
2) Stress: consisting of the application of DC stress conditions ($V_G = -2.0$ V, $V_S = V_D = V_B = 0$ V at 100 °C).
3) Recovery: consisting of several hundred seconds with all electrodes floating at 100 °C.

Each sequence was carried out for 5000 s of accumulated stress time. All jitter measurements represent the arithmetic mean of 18 nominally identical devices for each gate waveform pattern.

We investigate the role of the gate waveform pattern on the observed NBTI-induced jitter via eye diagram construction by using three different gate pattern variations (Fig. 4). These include: (1) a fast ring oscillator (fast-RO), (2) a slow ring oscillator (slow-RO), and (3) a pseudo random binary sequence of length $2^{15} - 1$ bits (PRBS15). The fast-RO pattern consists of a 50% duty cycle square waveform running as fast as the gate pad parasitics will allow (2 Gb/s). The slow-RO pattern is also a 50% duty cycle square waveform, however in this case the pattern is slowed to mimic the ring oscillator patterns typically employed in NBTI studies (~100 Mb/s) [6]. The PRBS15 pattern is a random sequence of $2^{15} - 1$ bits at 2G S/s which is chosen to mimic "real world" random logic. Inclusion of such a pattern should provide realistic worse-case information for a given technology. In this experimental arrangement, all drain current responses are captured, allowing jitter in the rising/falling edges to be observed and quantified in a statistical manner.

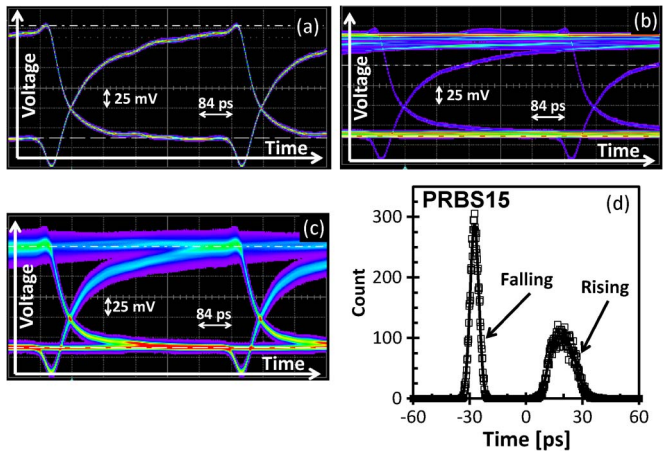

Fig. 5. Typical eye diagram of drain output for 3 input patterns: (a) fast RO, (b) slow RO, (c) PRBS15. (d) Extracted PRBS15 jitter histogram from eye diagram at 50% threshold signal level.

TABLE I
PRE-STRESS JITTER VALUES

Pattern	Rising Edge[a] [ps]	Falling Edge[a] [ps]
Fast-RO	0.89	0.73
Slow-RO	0.85	0.52
PRBS15	31.5	14.58

[a] Average of 12 consecutive acquisitions.

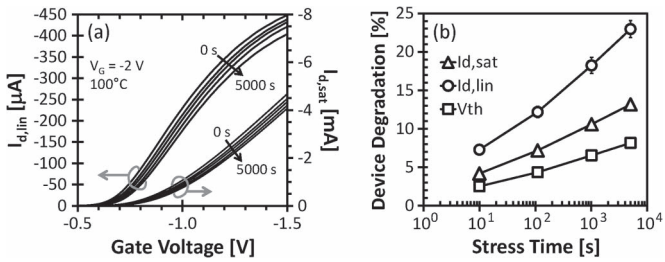

Fig. 6. $I_d - V_g$ curves measured versus stress time in linear regime and (a) in saturation regime, and (b) the degradation of extracted device parameters.

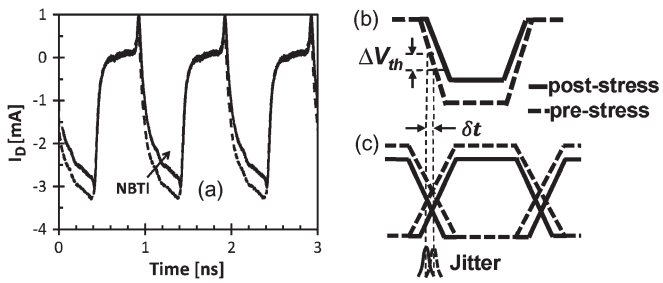

Fig. 7. (a) Pre- and post-stress output waveforms of a fast RO gate pattern. (b) "time-shift" in the transfer characteristic caused by NBTI degradation

Typical pre-stress eye diagrams for the various logic patterns are shown in Fig. 5(a)–(c). Note the aforementioned parasitic capacitance overshoot/undershoot at the transition edges of the eye diagram. For all these measurements, jitter is taken as the full width of the jitter distribution at the 50% threshold signal level [Fig. 5(d)]. Jitter distributions for both the rising/falling

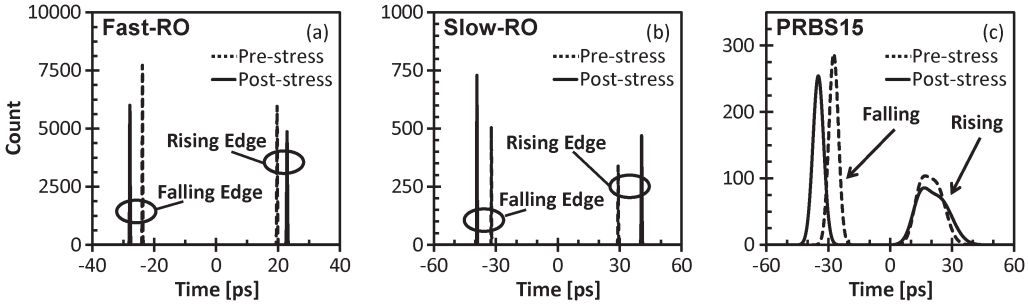

Fig. 8. NBTI-induced timing jitter distributions change for the (a) fast-RO, (b) slow-RO, and (c) PRBS15 pattern measurements.

edges are extracted separately. Note that throughout this work (regardless of gate pattern), the rising edge jitter is always larger than the falling edge jitter. This observation is also linked to the parasitic capacitances involved in these device structures. The parasitic charging/discharging cycles are not quite symmetric about the threshold level (50%) where jitter distributions are extracted. While this asymmetry may seem troubling, the NBTI-induced changes to these jitter distributions are still quite valid and will form the major conclusions of this work. Table I illustrates this rising and falling edge asymmetry for all gate patterns and lists the nominal pre-stress baseline timing jitter values for the device/experimental arrangement described above.

III. Results and Discussion

Representative linear and saturation $I_D - V_G$ characteristic curves as a function of NBTI stress time are shown in Fig. 6(a). The cumulative averages (from 18 devices) of the stress-induced saturation drain current (I_{dsat}), linear drain current (I_{dlin}), and threshold voltage shift (V_{th}) are illustrated in Fig. 6(b). In all cases, we note the expected NBTI-induced accumulation of positive charge in the gate stack. More importantly, we note that this NBTI stress introduces levels of degradation which are comparable to common NBTI studies.

These parametric shifts can also be observed in the time-series transfer characteristics as illustrated for a typical fast-RO pattern measurement [Fig. 7(a)]. The NBTI-induced drain current degradation necessarily introduces a "time-shift" in the transfer characteristic [Fig. 7(b) and (c)]. This can be thought of like the threshold voltage shift making the clock cycle late/early for the rising/falling edges respectively. The corresponding NBTI-induced timing jitter distributions for the fast-RO, slow-RO, and PRBS15 pattern measurements are shown in Fig. 8. We observe that the fast-RO and slow-RO patterns reveal large timing shifts proportional to the magnitude of the ΔV_{th} for both the rising and falling edges of the waveforms. It is also somewhat interesting to note that the observed timing shifts are larger for the slow-RO pattern measurements. This is perhaps an indicator that the slow-RO pattern cadence is such that there is sufficient time to populate/generate gate stack traps but insufficient time to completely de-trap during the off-portion of the cycle.

In an attempt to better relate these observed timing shifts to parametric shifts, we perform a calibration in which the baseline waveform voltage is shifted to simulate an artificial

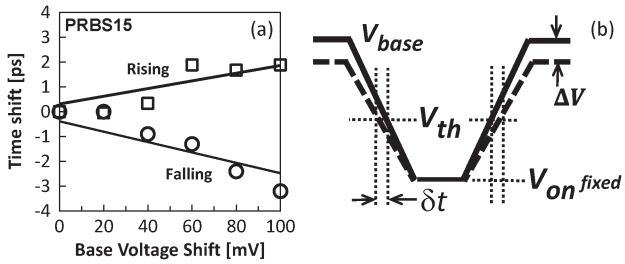

Fig. 9. Calibration of time shift by artificial shifting of the base voltage: (a) Measured time shift versus the change of base voltage for PRBS15. (b) Correlating the voltage shift to time shift.

ΔV_{th} (Fig. 9(a)). Since the rise and fall times of the input gate pattern are fixed (25 ps), a baseline voltage shift can be related to an artificial ΔV_{th}. The consequent time shift (associated with the baseline voltage shift) can then be loosely linked to ΔV_{th}. Fig. 9(b) illustrates this calibration curve and indicates that 1 ps of timing shift corresponds to ~50 mV of ΔV_{th}. Applying this calibration to the observed timing shifts in Fig. 8, illustrates that at circuit speeds, the effective ΔV_{th} can be quite large. This observation is consistent with a large body of work which indicates that decreasing measurement time increases the observed ΔV_{th} [18].

While the observed timing shifts are quite intriguing, they have been well explored in previous studies. Monotonic time shifting is an issue that can be well mitigated through clever circuit design and is reasonably well understood [9], [10]. However, the focus of this work (jitter) is actually much more troubling in that mitigation typically involves guard-banding at the cost of performance.

A hint of the NBTI-induced timing jitter changes can be observed through a close examination of the PRBS15 measurement of Fig. 8(c). NBTI clearly introduces a timing shift but, more importantly, introduces an increase in the breadth of the timing distribution (or jitter). Note that the breadth of the jitter distribution for the PRBS15 measurement is much larger than the fast-RO and slow-RO measurements. This difference is related to the nature of the gate patterns. In RO-type measurements, the device experiences the same ON/OFF times (same amount of trapping/de-trapping) for each cycle. Thus, while the stress-induced time shifting (net defect density) could be quite large, the random trapping/de-trapping (jitter) that occurs during each cycle is actually quite small. In the PRBS15 case, the random ON/OFF times correspond to random trapping/de-trapping which leads to an enhanced jitter (compared to RO).

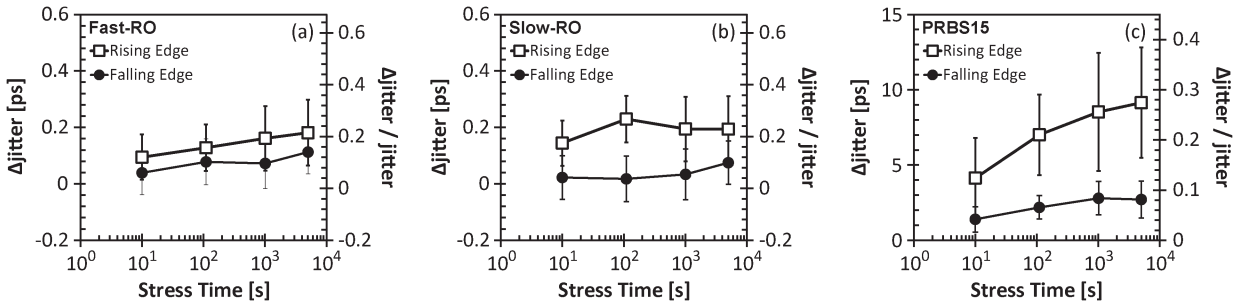

Fig. 10. Jitter degradation versus stress time with standard deviation from 18 devices for (a) fast RO, (b) Slow RO, (c) random logic of PRBS15.

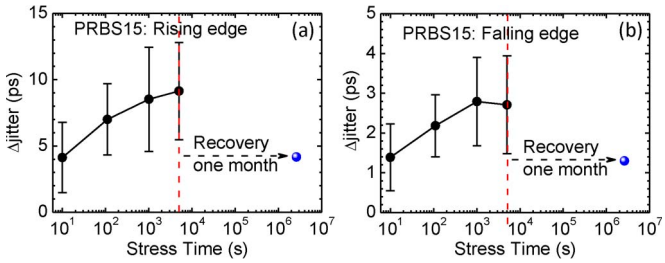

Fig. 11. One month-recovery of PRBS15 measurement for both (a) the rising and (b) falling edges. Jitter degradation can be attributed to a large recoverable component and a small permanent component.

These observations are further illustrated in Fig. 10 for the fast-RO, slow-RO, and PRBS15 pattern measurements as a function of NBTI stress time. Note that the NBTI-induced change in jitter for both the fast-RO and slow-RO measurements is quite small and is approaching the noise floor of the measurement.

Comparatively, the PRBS15 measurement yields a relatively large NBTI-induced increase in jitter (much larger than the noise floor) for both the rising and falling edges as a function of stress time. In this scenario the PRBS15 gate pattern introduces a "random" stress/recovery balance for each time period. The corresponding random ΔV_{th} associated with such a gate pattern necessarily introduces a larger distribution of transfer characteristics (increased jitter). Considering that the eye-diagram consists of a superposition of $\sim$30 000 bit segments, the stress-induced increase in jitter is consistent with the notion that NBTI generates new defects which participate in the trapping/de-trapping present in random logic.

In an effort to investigate the permanency of these newly generated NBTI-induced fast traps, the devices were allowed to recover at room temperature with all electrodes floating for a time period of 1 month. The post-recovery PRBS15 measurement is illustrated in Fig. 11 for both the rising and falling edges. After this long term recovery, the measured NBTI-induced PRBS15 jitter recovers (though not completely). Thus, it would appear that the DC NBTI stress introduces a larger recoverable jitter component and a much smaller more permanent jitter component. Typical studies frame the NBTI degradation picture as a combination of two components (permanent and recoverable) which introduce a ΔV_{th} linked to time shifting [19], [20]. It is interesting to note that in these measurements there is seemingly the same two components (permanent and recoverable) which instead affect fast trapping/de-trapping associated with jitter.

The observed PRBS15 increase is a strong indicator that the typical waveforms (fast-RO, slow-RO) used to gauge NBTI reliability are insensitive to the timing jitter seemingly present in the critical pathways of random logic (PRBS15). We also note that the magnitude of the jitter increase represents a significant obstacle for high-performance circuits. While we recognize that these results are specific to the samples investigated, the mere observation of a pattern-dependent jitter increase is troubling.

It is also important to delineate the differences between NBTI recovery (as it is usually discussed [21]) and the recovery present in these measurements. The recovery between the stress and measurement phases most certainly introduces a ΔV_{th} recovery and consequent recovery in the observed time shift. However, it is unclear how this recovery affects the random trapping/de-trapping associated with jitter. While we agree that the net trapped charge is linked to the recovery between stress/measure, we cannot be sure that recovery-induced changes in the trapped charge impact the jitter. Thus, the link between published NBTI recovery studies and the stress/measure recovery in these jitter measurements is quite murky and should be further investigated.

IV. Conclusion

In this work we have shown that device-level eye-diagram measurements are a useful approach to examine the impact of NBTI on circuit-speed device operation. This experimental approach allows for an examination of the impact of NBTI-induced degradation on the timing shift and timing jitter at relevant circuit speeds. We find that the measured jitter depends strongly on the chosen gate pattern. Pseudo-random gate patterns, chosen to mimic random logic, exhibit the largest stress-induced jitter increases while the ring oscillator gate patterns are seemingly insensitive to these same jitter increases. Collectively, these results strongly suggest that the typical methods (DC or simple ring oscillator characterizations) used to translate reliability measurements to circuit reliability underestimate the circuit impact of NBTI.

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Authors' photographies and biographies not available at the time of publication.