PBTI-Induced Random Timing Jitter in Circuit-Speed Random Logic

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***Abstract*— Accurate reliability predictions of real-world digital logic circuits rely heavily on the relevancy of device-level testing. In the case of bias temperature instability (BTI), where recovery plays a significant role, a leap of faith is taken to translate device-level reliability data into a practical information for the real-world circuit implications. In this paper, we develop a methodology to bridge this gap by employing an eye diagram approach, which allows us to monitor, at circuit speed, device-level random jitter degradation in response to stress. By employing a variety of positive BTI gate voltage stress and sense bit sequences (including dc, ring oscillator (RO), and pseudorandom), we are able to compare the effectiveness of these approaches at capturing random timing jitter. We find that conventional RO-type measurements are unable to capture the random jitter degradation. This calls into question the effectiveness of using RO structures as a proxy for real-random logic circuits. Only when a pseudorandom bit sequence is employed does the true extent of jitter degradation become observable. This is an important development and serves as an accurate means to translate device-level reliability data to predict real-world digital logic circuit degradation.**

***Index Terms*— Jitter, positive bias temperature instability (PBTI), pseudorandom bit sequence (PRBS).**

I. Introduction

THE most accurate reliability information is gleaned directly from actual products subject to real-world use conditions. However, this is almost impossible to accomplish in the semiconductor industry, where technology generations are short and companies cannot afford to wait months or years to establish reliability metrics. Thus, accelerated testing is preferred in which individual devices or simple circuits are stressed and then used to predict actual product reliability under use conditions. Ensuring an accurate prediction based on this methodology relies heavily on the relevancy of the way in which the accelerated testing is performed compared with the product and its use conditions. Unfortunately, this is not a simple or straightforward task.

For example, bias temperature instabilities (BTIs), including both positive BTI (PBTI) and negative BTI (NBTI), have emerged as one of the most critical reliability issues in modern devices [1], [2]. While earlier studies had focused mainly on dc or quasi-dc degradation [1]–[3], the vast majority of more recent works focus heavily on the so-called recoverable degradation [4]–[7]. The reason being that a naïve dc-stress/dc-measure approach fails to capture the true extent of the degradation itself and the device physics involved. Thus, attempting to translate dc-stress/dc-measure data (in which recovery is essentially ignored) to real-world logic circuit operation (where recovery can very much be in play) will result in an unrealistic reliability prediction. The trouble arises because, in the real world, different logic gates are randomly cycled ON or OFF while dc data assumes an always ON scenario. Supporting this viewpoint is the fact that recovery is now being viewed as a vehicle to extend a products' lifetime [8]–[10]. Simply put, the reliability testing must be relevant to the way in which the actual products' circuit will operate in the field.

As such, the community has evolved to include somewhat more realistic BTI Testing, including device-level fast measurements (including fast IV) and ring oscillator (RO)-type measurements [11]–[20], both of which have serious drawbacks for predicting random logic circuit reliability. Fast IV, as a research tool, has allowed very extensive recovery investigations [5], [11], [14], [20]–[22], but is unfortunately limited in the speed at which the phenomena can be observed meaning that recovery can occur on time scales not observable via these techniques. While microsecond and even hundreds of nanosecond time scales are routinely reported, real-world modern logic circuits easily operate with clock frequencies well into the gigahertz range. One must take a leap of faith that extrapolations to the circuit speeds remain accurate. Additionally, these studies are limited to testing individual devices; a very different environment compared with real logic circuits containing a vast multitude of interacting logic gates.

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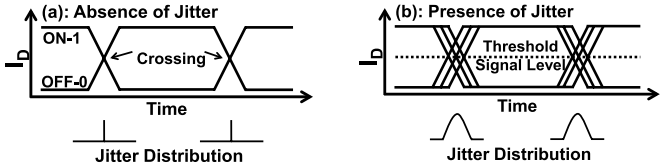

Fig. 1. Construction of an eye diagram is accomplished by superimposing many sampled drain current transitions in response to an input bit sequence. (a) In the absence of timing irregularities, the jitter distribution is essentially a delta function. (b) When irregularities are present, the jitter has some distribution corresponding to the device turning ON and OFF at slightly different times for each bit (jitter).

RO structures, on the other hand, are actual circuits and are capable of high frequencies, but they do not accurately represent the random nature of digital logic circuits since they are limited to predictable periodic cycling [15].

Thus, there is an extreme need to develop device-level measurement capabilities that are accurate, relevant, and can be easily translated to real-world environments experienced by random digital logic gates. Recently, we have developed such a measurement technique that meets these requirements and have presented preliminary NBTI [23] and PBTI results [24].

The key aspects of our measurement capability are: 1) the ability to stress a device at circuit speeds in a manner consistent with random logic operation and 2) the ability to sense device timing degradation at circuit speeds in a way that realistically represents the environment experienced by a random logic gate. These two attributes mean that our stress and sense conditions very closely mimic real-world digital logic operation and represent the most realistic and relevant device-level reliability testing possible.

In this paper, we solidify our new methodology with a detailed description of the eye-diagram concept (Section II) and a detailed experimental setup and procedure (Sections III and IV). The experimental results and discussions are based on more statistics (20 devices for each data point in this paper, nine in [24]).

II. Eye Diagram and Jitter

Our highly realistic circuit-speed stress/sense methodology takes advantage of two main capabilities: 1) the ability to apply a circuit-speed pseudorandom bit sequence (PRBS) to the transistor gate in a stress or sense mode and 2) the ability to measure the drain current response at circuit speeds through the use of a so-called eye diagram measurement.

It is useful to first explain the construction and meaning of an eye diagram, which is schematically illustrated in Fig. 1. In the simplest sense, an eye diagram is the superposition of many sampled bit sequence responses, all of which are aligned to some clock edge [25]. In our measurements, an ON/OFF binary bit sequence is applied to the gate while the drain current response is repetitively sampled. The drain current transitions (transitions between ON and OFF) are aligned with the bit sequence clock such that, in the absence of timing jitter, the assembled eye diagram resembles that of Fig. 1(a), forming the so-called eye [25].

The eye diagram allows us to observe the device response under high-speed circuit conditions. More importantly, it allows us to visualize and quantitatively analyze the

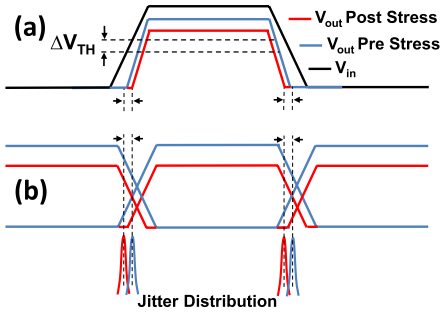

Fig. 2. Schematic describing how a deterministic V_{TH} shift will necessarily introduce a shift in the mean jitter distribution. (a) V_{TH} shift is analogous to the device turning on at a slightly different time (δt). (b) When measured via an eye diagram, it is clear that the jitter distribution will shift an amount δt, proportional to ΔV_{TH}.

timing characteristics of the device in response to some input bit sequence. In the real world, all devices have some timing distribution corresponding to the device turning ON or OFF at slightly different times for each bit. This is called jitter, and in the presence of jitter, the eye diagram effectively closes Fig. 1(b). Here, we define jitter in these measurements as the full width of the jitter distribution at 50% threshold signal level taken on the rising/falling edge of the transition.

Timing jitter is an extremely important consideration in circuit design and directly affects real-world logic circuit critical timing budgets, meaning that logic errors occur if a device does not switch ON or OFF within some required timing window. With our approach, we can directly quantify the timing jitter of a particular device at circuit-speed and, more importantly, we are able to monitor the timing jitter change in response to stress. This means that we can directly quantify, in a highly relevant manner, how device degradation relates to circuit timing characteristics.

A threshold voltage (V_{TH}) shiftis analogous to the device turning on (or OFF) at a slightly different time in response to some input bit. Thus, it is important to note that a deterministic V_{TH} shift will introduce a proportional deterministic time shift in the mean jitter distribution, as schematically illustrated in Fig. 2. This type of circuit timing error has been discussed by others as it is observable via conventional RO type measurements [12], [16], [17]. Additionally, many circuit design studies have presented possible design solutions to address this type of timing error [26]–[28]. This deterministic timing shift (proportional to V_{TH} shift) is the subject of the majority of BTI studies and is admittedly quite interesting. However, in this paper, we will focus not on the timing shift, but instead on the BTI-induced changes in timing jitter. Timing jitter has no known solutions and poses a substantially more troubling problem for circuit reliability. Note that these timing issues are typically investigated using RO test structures. However, a broadening of the jitter distribution (defined here as random jitter) is not observable via RO measurements. It is for these reasons that the focus of this paper is solely on random timing jitter.

III. Bit Sequence

The other unique aspect of this paper involves the actual bit sequence applied to the gate electrode for stress or sense

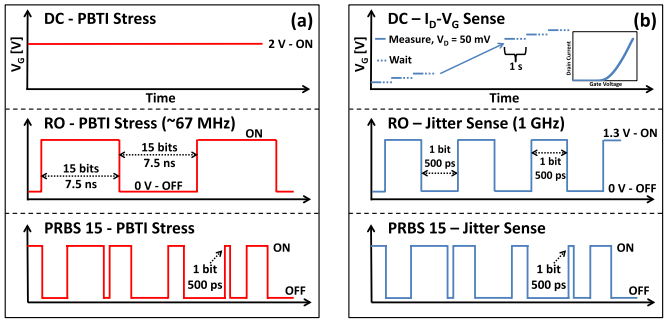

Fig. 3. Bit sequences used in this paper for (a) stress and (b) sense modes. Each mode contains dc, RO, and PRBS bit sequences. The PRBS sequence allows for the most realistic stress and jitter sense measurements possible as it closely mimics the environment experienced by real-world digital logic gates. Eye-diagram construction was based on the sense mode, 32 000 bits were used for RO-jitter sense, and $2^{15}-1$ bits were used for PRBS15-jitter sense.

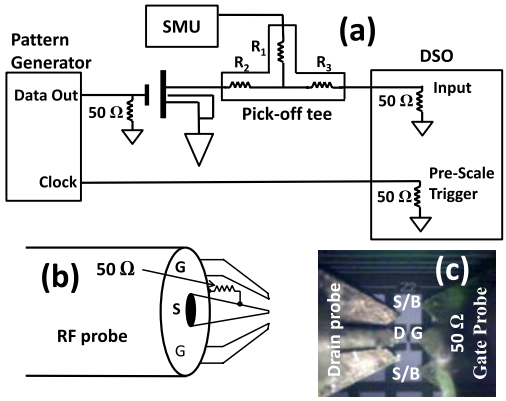

Fig. 4. (a) Schematic of the measurement setup. (b) and (c) High-speed pattern generator provides the stress/sense bit sequence through a custom 50 Ω terminated probe. The drain current response (eye diagram) is sampled via a high speed digital sampling oscilloscope.

modes, schematically illustrated in Fig. 3. Shown is both the stress [Fig. 3(a)] and sense [Fig. 3(b)] sequences, each of which contains three possible modes (dc, RO, and PRBS). dc stress consists of all binary bits in the sequence being turned on (binary 1) and mimics a conventional dc stress. RO stress is a sequence that mimics a conventional 50% duty cycle RO structure stress. Finally, the PRBS stress illustrates the unique manner in which we can mimic real-world random digital logic operation. It consists of a pseudorandom bit sequence (PRBS) consisting of $(2^{15}-1)$ bits (PRBS-15). When input to the gate as a stress, the PRBS-15 sequence accelerates the device degradation in a manner consistent with how the device is switched ON and OFF in real random digital logic.

The same three modes (dc, RO, and PRBS) are also used for the random jitter sense measurements [Fig. 3(b)]. Of course, the dc sense mode is unable to capture jitter and is therefore limited to monitoring V_{TH} degradation via I_D–V_G. The details of measuring the I_D–V_G curve are discussed later. It is worth noting again that the PRBS jitter sense sequence is highly consistent with the manner in which real random digital circuits operate. Thus, we can monitor, via an eye diagram, how the stressed device timing characteristics behave in a highly realistic manner.

It is important to note that the stress bit sequence is independent of the sense bit sequence. The jitter of a device stressed in one mode (RO stress for example) can be measured with a different sense mode (PRBS sense for example). In our experiment, we use 67 MHz bit sequence during RO-stress mode, and 1 GHz bit sequence during the RO-sense mode. This allows us to compare the relative jitter values across all the stress/sense combinations as well as providing a direct comparison of the different sense modes' ability to observe timing degradation.

IV. Experimental Details

Shown in Fig. 4(a) is the experimental arrangement used to apply the stress/sense bit sequence and measure the eye diagram drain current response. A commercially available pattern generator with a maximum data rate of 20 Gb/s is connected to the RF MOSFET gate contact through a ground-signal-ground RF probe. The RF probe, schematically shown

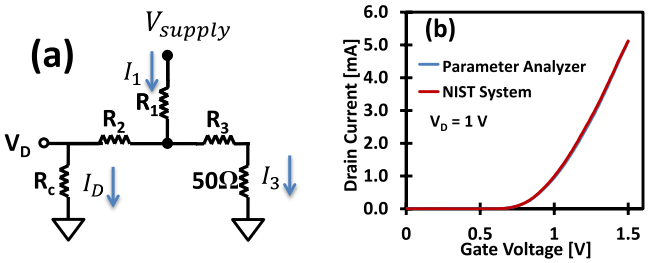

Fig. 5. (a) Equivalent circuit schematic of the pick-off tee allowing the acquisition of dc I_D–V_G curves via the dc sense bit sequence shown in Fig. 3(b). (b) Calibration measurement illustrating the close agreement between I_D–V_G measured by conventional parameter analyzer and our method.

in Fig. 4(b) and through an optical microscope in Fig. 4(c), is terminated with a 50 Ω load at the very end of the tip. This ensures that the integrity of the high-speed bit pattern from the pattern generator to the device.

The RF MOSFET source (V_S) and body (V_B) are grounded while a second RF probe monitors the drain current (I_D). The drain current is fed through a microwave pick-off tee and then monitored via a source-measure-unit (SMU) or is sampled by a high-speed digital sampling oscilloscope with a 100 GHz bandwidth. The oscilloscope constructs the eye diagram by aligning the sampled I_D to the clock of the pattern generator, and the eye-diagram construction is completed by the embedded serial data analysis module of the sampling oscilloscope itself.

The pick-off tee serves as a convenient way to apply dc drain bias (V_D) to the device without sacrificing the fidelity of the high-speed I_D response. The pick-off tee also allows for the acquisition of conventional dc measured I_D–V_G curves of the device without disturbing the high-speed experimental arrangement, eliminating the need to change/re-land probes and the like. Shown in Fig. 5(a) is an equivalent circuit schematic of the pick-off tee arrangement while Fig. 5(b) illustrates a calibration example by comparing I_D–V_G curves measured conventionally with a semiconductor parameter analyzer and through our pick-off tee method. We note the very close agreement between the two methods. Converting the

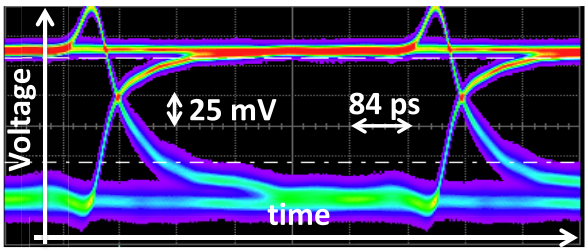

Fig. 6. Typical eye diagram measured via our approach. The non-uniform peak height and current overshoot are a direct result of the device parasitic capacitance. The voltage scale is 25 mV/division, and the time scale is 84 ps/division.

measured SMU values into drain current requires the relations

$$I_D = I_1 - \frac{V_{\text{supply}} - I_1 R_1}{R_3 + 50\ \Omega} \quad (1)$$

$$V_D = V_{\text{supply}} - I_1 R_1 - I_D R_2 \quad (2)$$

where I_D (V_D) is the drain current (voltage), I_1 is the SMU current, V_{supply} is the SMU voltage, and R_1, R_2, and R_3 are the pick-off tee resistor values.

The devices used in this paper are RF type n-channel MOSFETs with gate-stacks consisting of a 1 nm SiO_2 interfacial layer and 2 nm of HfO_2. The device width and length are 10 and 0.18 μm, respectively. Sets of 20 devices are subject to various combinations of the stress and sense sequences, shown in Fig. 3. The same devices are sensed with multiple modes for a given stress condition. All measurements follow a sense/stress/recover/sense sequence at 100 °C consisting of: 1) a pre-stress jitter and/or V_{TH} measurement; 2) PBTI stress is applied with gate voltage (V_G) = 2 V, and source, drain, and body contacts held at ground potential; 3) PBTI recovery phase in which the gate, drain, source, and body contacts are held at ground potential for 600 s following stress; and 4) sense measurements with V_D held at around V_{DD} for jitter measurement, and V_D held to 50 mV for quasi-dc I_D–V_G measurement to monitor V_{TH} degradation. In all cases, ΔV_{TH} was determined using a constant current criterion of 500 nA × (W/L).

A typical eye diagram measured with our system is shown in Fig. 6. The device pad parasitic capacitance is also responsible for the non-uniform peak height and current overshoot seen in Fig. 6. This pad capacitance imposes a device-dependent limit on the bit sequence rate. Thus, measurements of these devices are limited to 2 Gb/sto minimize parasitic overshoot/undershoot.

V. Results and Discussion

While our technique is capable of a wide variety of stress and sense bit sequences (Fig. 3), we first discuss the simplest combinations in which the stress sequence is limited to that of a conventional dc stress and then sensed with dc, RO, or PRBS sequences. Shown in Fig. 7 is PBTI-induced degradation versus stress time including: 1) dc measured threshold voltage degradation; 2) Δjitter measured via the RO sense mode; and 3) Δjitter measured via the PRBS sense mode. The term Δjitter denotes the difference in the values of jitter measured before any stress and after certain duration of stress.

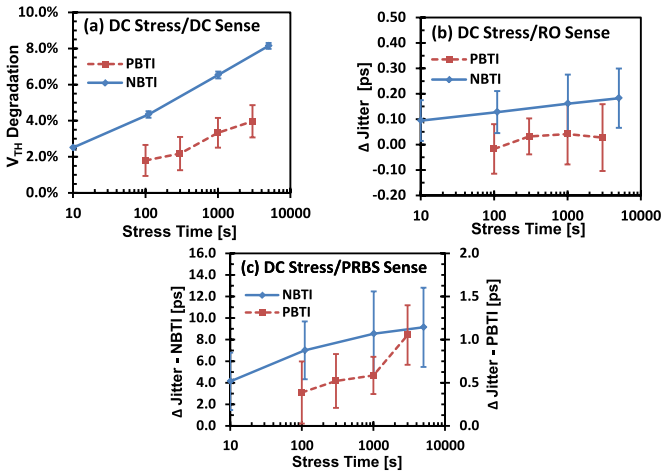

Fig. 7. PBTI- and NBTI-induced degradation as a function of dc stress time. (a) ΔV_{TH} measured via the dc sense mode. Δjitter measured via (b) RO sense mode or (c) PRBS sense mode. Note that significant jitter degradation is observable via the (c) PRBS sense mode while the (b) RO sense mode is seemingly blind to the degradation.

For comparison and discussion purposes, we have also included in Fig. 7 very similar NBTI data taken on nominally identical devices using identical stress/sense techniques with the same experimental setup. Further details of the NBTI work can be found in [23]. It is important to note that the data points represent the mean value (of either ΔV_{TH} or Δ jitter) measured across 20 devices with the error bars representing the standard deviation of the mean value.

For the dc measured case, in Fig. 7(a), the V_{TH} degradation for both NBTI and PBTI are quite expected and monotonically increase with stress time. However, when measured via the RO-type sense pattern, in Fig. 7(b), the jitter degradation of both NBTI- and PBTI-stressed devices change very little. Without further measurements, one would assume then that jitter degradation is not an issue. When identical measurements are made using the PRBS sense mode, shown in Fig. 7(c), we see that this tact would be a poor approach. Significant jitter degradation is clearly observed in this case.

Two interesting observations can be made about Fig. 7. First is the most troubling in that the jitter degradation measured via PRBS is unobservable when utilizing the more conventional RO-type sense mode. This indicates that RO-type experiments do not accurately capture the random logic timing implications of stress and, compared with PRBS, are an inferior vehicle to study the phenomena. The second observation is that NBTI clearly has a larger jitter than its PBTI counterpart, regardless of the sense mode. While both are serious reliability problems in modern devices, this disparity agrees well with recent reports pointing toward a more dominate role for NBTI, possibly due to NBTIs larger permanent degradation component [29]. Nevertheless, Fig. 7 clearly indicates that PRBS sense measurements are able to capture timing degradation due to dc stress, which is not observable via RO-type sequences.

Building on the previous discussions, we now explore the role that the stress sequence plays by employing the use of the RO and PRBS stress modes, shown in Fig. 3. Shown in Fig. 8 is V_{TH} degradation, measured via the dc I_D–V_G mode, for the three modes of stress, including dc, RO, and PRBS.

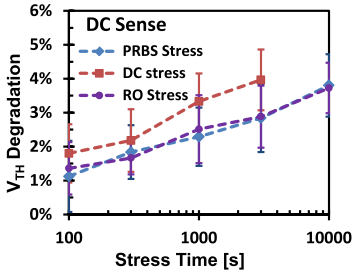

Fig. 8. PBTI-induced V_{TH} degradation measured via the dc sense mode for the three stress modes. The RO and PRBS stress introduce quite similar degradation.

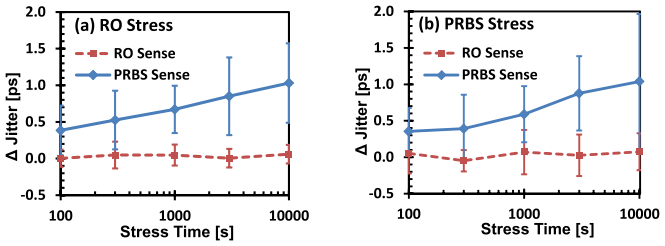

Fig. 9. Jitter degradation measured for (a) RO stress mode and (b) PRBS stress mode. The degradation is measured with both RO and PRBS sense in both cases. We note the inability of the RO sense mode to detect any noticeable jitter change in either case while the PRBS sense mode clearly captures the degradation.

For the case of RO and PRBS stress modes, the stress time was extended to introduce similar degradation as the dc stressed case. While the dc stress clearly introduces the most severe degradation, the RO and PRBS stresses introduce quite similar V_{TH} degradation when measured in this mode.

While Fig. 8 is interesting in its own respect, we next, compare the RO stress mode [Fig. 9(a)] and PRBS stress mode [Fig. 9(b)], each measured with both RO sense and PRBS sense modes. In both cases of Fig. 9, the RO sense does not display any characteristic jitter degradation over the entire stress time. However, when the same devices are measured via the PRBS sense mode, both stress modes clearly introduce a significant increase in Δjitter. Similar to Fig. 7, the RO sense measurements are blind to the random jitter increase, strongly indicating that RO sense measurements are a poor vehicle to observe random digital logic random timing degradation. As mentioned previously, this is a troublesome observation as random jitter, which is unobservable via conventional RO measurements, is the most worrisome type of error in random digital logic.

We also compare the jitter response for all three stress modes (dc, RO, and PRBS) measured with RO sense [Fig. 10(a)] and PRBS sense [Fig. 10(b)]. Similar to our previous measurements, the RO sense mode shown in Fig. 10(a) does not capture any noticeable jitter degradation, regardless of the stress mode. This is in agreement with our previous discussions regarding the inability of RO sense measurements to observe random jitter degradation. However, when the same devices are measured via PRBS sense mode, clear random jitter degradation occurs. Additionally, all three stress modes introduce similar magnitudes of Δjitter. This is an important observation as dc stress is typically defined as a worst case degradation mode [8]. Subsequent ac circuit analysis uses

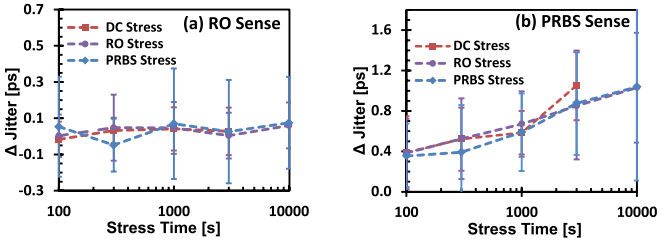

Fig. 10. Jitter degradation for all three stress modes measured via (a) RO sense mode and (b) PRBS sense mode. While RO is blind to the degradation, the PRBS sense clearly captures significant Δjitter. DC stress is not necessarily a worst case stress as it introduces a similar change in jitter, which is shown in (b).

this dc worst case assumption and typically allow for the availability of additional timing margin (usually attributed to recovery). The results of Fig. 10 suggest otherwise as the worst case stress (dc) introduces similar jitter degradation as the other, more realistic sense modes.

In RO Sense measurements, the device experiences the same ON/OFF times (same amount of trapping/de-trapping) for each cycle. Thus, while the BTI-induced time shift (due to net defect density) could be quite large, the random trapping/de-trapping (jitter) that occurs during each cycle is actually quite small [23, Fig. 6], which means the breadth of the timing distribution (or jitter) is quite small.

The PRBS15 sense measurement yields a relatively large PBTI-induced increase in jitter (much larger than the noise floor) for both the rising and falling edges as a function of stress time. In this scenario, the PRBS15 gate pattern introduces a random trap/detrap balance for each time period. The corresponding random ΔV_{th} associated with such a gate pattern necessarily introduces a larger distribution of transfer characteristics (i.e., increased jitter). Considering that the eye-diagram consists of a superposition of $\sim$30 000 bit segments, the stress-induced increase in jitter is consistent with the notion that PBTI generates new defects which participate in the trapping/de-trapping present in random logic.

VI. Conclusion

We introduce a circuit-speed eye diagram methodology to monitor device-level random jitter degradation in response to stress. The key capability involves the application of a highly realistic bit sequence and the subsequent high speed capture of the drain current response. We investigate PBTI-induced random timing jitter degradation for several different stress and sense modes. We find that more conventional ring oscillator-type measurements fail to capture the jitter implications in a real random logic circuit. Only when the pseudo-random bit sequence sense mode is utilized, is the jitter degradation observable. This calls into question the relevancy of using ring oscillator structures as a BTI test vehicle for real-world logic circuits. Additionally, we observe dc, RO, and PRBS stress modes all introduce quite similar increases in random timing jitter when measured via PRBS bit sequences. This should have important implications as a dc stress is usually considered a worst case scenario and the assumption is made that additional timing budget headroom will be available in the final product. While more extensive measurements and

more substantiation should be made to validate that, this paper serves to provide an initial glimpse of the real-world digital logic implications of PBTI. Our approach provides a foundation for bridging the gap between device-level reliability testing and highly realistic circuit lifetime estimations.

Finally, we need also point out that since our transistors are quite large ($W = 10\ \mu$m), the effect of random telegraph noise (RTN) should not be severe, but it is worth mentioning that jitter may be also contributed by RTN (and other sources), which merits further investigation.

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Authors' photographs and biographies not available at the time of publication.