Device-Level PBTI-induced Timing Jitter Increase in Circuit-Speed Random Logic Operation

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Introduction: Bias temperature instability (BTI) has proven to be one of the most perplexing challenges facing modern circuit design [1-6]. While the well-known recoverable threshold voltage (V_{th}) component [7] represents a clear device-level lifetime extension, the translation from device to circuit is still quite tenuous [1-6, 8-12] due the general inability to characterize devices at circuit speeds. It is perhaps more disconcerting to realize that circuit-level BTI verification is restricted to observations in ring-oscillator (RO) "test" circuits [8-12]. While RO results do provide some useful BTI guidance, regular RO patterns are comparatively poor representations of random digital logic. The root of this very complex problem is centered on the absence of reliable device-level BTI characterizations which readily translate to "real-world" digital logic. This translation has been very recently explored in a *limited NBTI study currently under review* [13].

In this work, we *greatly expand* this effort [13] via device-level PBTI examinations in which *both "sense" and "stress" utilize pseudo-random binary sequence (PRBS) gate waveforms designed to mimic random logic circuit environments.* This allows for acquisition of device-level eye-diagram measurements that capture PBTI-induced changes in random timing jitter. Eye-diagram timing jitter "sense" measurements involve both RO and PRBS waveforms. PBTI "stress" conditions involve more conventional DC and RO waveforms as well as PRBS waveforms. This unique experimental vector allows for unambiguous device-level examinations of PBTI-induced random timing jitter at circuit speeds.

We show that: (1) eye-diagram analysis is well suited to study PBTI's impact on random logic and (2) PBTI-induced timing jitter increase associated with random logic (PRBS) is much larger than anticipated using regular RO test circuit patterns. *These observations indicate that RO measurements underestimate the PBTI-induced increase in random timing jitter.* These differences are consistent with the fast trapping / de-trapping transients of very short time scales. The very short time scales involved in these measurements (500 ps to 7.5 ns) are shorter than all other reported transient BTI studies.

Experimental: The devices used for this study are 10 x 0.18 μm^2 (2 nm/1 nm) HfO_2/SiO_2 nFETs with ground-signal-ground RF layouts. Fig. 1a illustrates the experimental arrangement. The DC gate bias and the RO/PRBS gate waveforms are supplied by a high-speed pattern generator via a custom 50 Ω terminated RF probe (Fig. 1b). The drain current response is captured by a high-speed sampling oscilloscope through a pick-off tee. The pick-off tee provides a method to apply drain biases without sacrificing signal integrity (Fig. 2). Timing jitter is quantified by recording the transition of ≈32,000 bits repetitively superimposed (such that clock edges are aligned) to construct an eye-diagram (Fig. 3). The gate waveform bit-rate (2 GB/s) is limited by the device parasitic capacitance which manifests as non-uniform peak height and is directly responsible for the observed overshoot (Fig. 3).

Devices are each subject to a measure-stress-recovery-measure sequence at 100 °C (9 devices per stress condition). The DC and AC PBTI stresses (V_D=V_S= V_B=0 V) include RO (≈ 67 MHz) as well as PRBS stresses with sequence length of (2^{15}-1) bits (Fig. 4). Devices were allowed to recover (V_G=V_D=V_S=V_B=0 V) for 600 s after each PBTI stress. After each recovery step, a series of DC (I_D-V_G with V_D = 50 mV) and AC jitter measurements were performed to assess ΔV_{th} and timing jitter increase (Fig. 5). In all cases, ΔV_{th} was determined using a constant-current criterion (500 nA x (W/L)).

Results and Discussion: Fig. 6 schematically illustrates that a deterministic ΔV_{th} necessarily introduces a proportional deterministic time shift in the mean jitter distribution. Such time shifts are well-captured in the conventional RO-type measurements and circuit design solutions have been well publicized [2, 9-12]. While the observed time shifts are noteworthy, we instead focus our efforts on an examination of the changes in stress-induced *random* timing jitter. Random timing jitter is manifested as a broadening of the jitter distribution and is a substantially more formidable circuit reliability obstacle.

DC-stressed PBTI degradation of (a) DC-measured ΔV_{th}, (b) RO measured Δjitter, and (c) PRBS measured Δjitter is shown in Fig. 7. DC-stressed NBTI measurements (V_G = -2 V, V_S=V_D=V_B=0 V) for nominally identical pFETs [13] are included for comparison. Both BTI stresses introduce a measurable ΔV_{th} which seemingly has very little impact on Δjitter increases measured using RO-type waveforms. However, a significant disparity exists between NBTI and PBTI random (PRBS-measured) Δjitter response (Fig. 7c). For PRBS measurements, NBTI introduces a relatively large Δjitter increase while the PBTI Δjitter increase is comparatively smaller. This is consistent with recent reports [8] indicating a dominant role for NBTI. The NBTI/PBTI disparity may be related to NBTI's, proportionally larger, permanent degradation. Regardless of the origin, it is unsettling that (more conventional) RO measurements are seemingly blind to random (PRBS) Δjitter increases.

These NBTI/PBTI observations collectively indicate that the random (PRBS) timing measurements reveal larger timing uncertainties. It is therefore quite conceivable that differences in stress waveforms (RO and PRBS) may also play a role in the observed timing jitter (otherwise unobservable using DC stresses). Accordingly, we performed an additional set of experiments utilizing AC (RO and PRBS) stresses. Fig. 8 illustrates the PBTI-induced ΔV_{th} for devices subject to RO and PRBS stress waveforms as well as the DC stress case. AC stress times were extended (≈ 2x) to introduce similar ΔV_{th} in all DC and AC stress cases.

Figs. 9 and 10 illustrate the RO- and PRBS-measured Δjitter increase in devices subject to both *RO PBTI* and *PRBS PBTI* stresses, respectively. Similar to the DC stress case (Fig. 7), we observe no measurable RO-measured Δjitter increase, regardless of stress waveform. Contrastingly, we observe an increase in the PRBS-measured random timing Δjitter. Fig. 11 summarizes these differences in PRBS-measured Δjitter for all three stress conditions (DC, RO, and PRBS) at 3000 s of stress time. In all stress cases, the RO measurements are blind to the Δjitter increases. This indicates that BTI-based RO measurements are poor predictors of relevant timing in random digital logic. However, the PRBS-measured random Δjitter measurements are comparatively much more sensitive to the jitter in "real" random digital logic. Fig. 11 also illustrates that the DC, RO, and PRBS stresses introduce comparable random (PRBS-measured) Δjitter increases. This strongly suggests that *an assignment of DC stress as the "worst-case degradation" with the presumption of additional available margin in an AC circuit environment is an overly optimistic practice.* Since PRBS stress/measure sequences are extremely close proxies for random-logic device degradation, *our observations indicate that the most frightening types of timing errors (random) are missed by common RO-type test-circuit interrogations.*

Conclusions: We utilize eye-diagram measurements of timing jitter to investigate the impact of PBTI in devices subject to DC as well as ring oscillator (RO) and pseudo-random binary sequence (PRBS) stress waveforms. We observe that RO measurements miss the relevant random timing jitter increases which are well captured using PRBS measurements. We also observe that DC, RO, and PRBS stresses all introduce similar increases in random timing jitter. This calls into question the widely assumed degradation headroom between DC and AC measurements. This work collectively provides a snapshot of PBTI degradation in "real" circuit environments. It provides a path for more accurate and realistic circuit lifetime estimations and circuit timing budget criteria.

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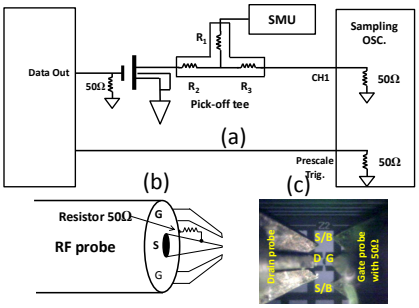
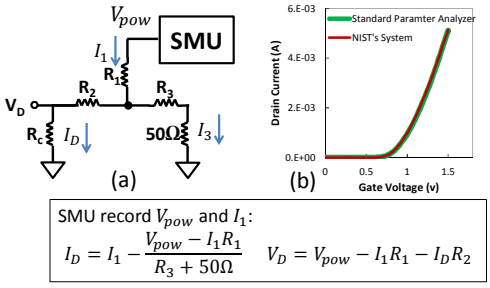


Fig. 1: (a) Experimental arrangement supporting the DC/AC stress modes and AC jitter measurements with a bit-rate of 2 GB/s. Impedance matching and proper grounding is essential to maintain the high-speed signal integrity. The waveforms are applied to the gate using a custom 50 Ω terminated RF probe (b) and (c).



SMU record V_{pow} and I_1:

$$I_D = I_1 - \frac{V_{pow} - I_1 R_1}{R_3 + 50\Omega} \qquad V_D = V_{pow} - I_1 R_1 - I_D R_2$$

Fig. 2: (a) Equivalent circuit schematic of the pick-off tee circuit allowing for the simultaneous acquisition of quasi-DC I_D-V_G measurements and high-speed jitter measurements in an integrated experimental arrangement without sacrificing signal integrity. (b) Calibration against standard parameter analyzer reveals consistent I_D-V_G curves.

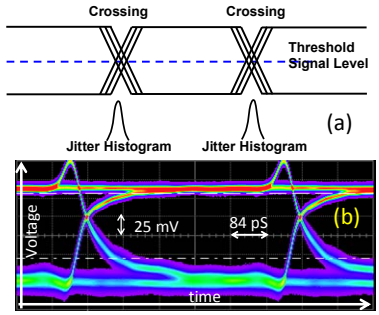


Fig. 3: (a) Eye-diagram construction via alignment of the clock edges of ≈32,000 superimposed bits. (b) Jitter (rising edge) is defined as the full width at half maximum of the jitter distribution at 50% of the threshold signal level. The bit rate (2 GB/s) is limited by the device parasitic capacitance which is directly responsible for the observed overshoot.

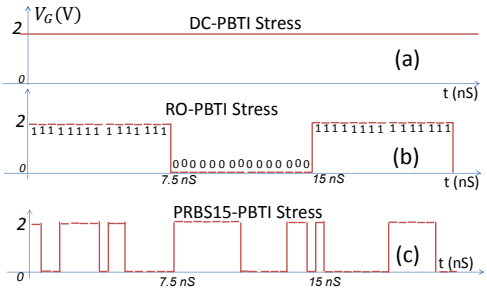


Fig. 4: Schematic illustration of the **three PBTI "stress" modes**. (a) Conventional DC stress, (b) ring oscillator (RO) stress, and (c) pseudo-random binary sequence (PRBS) stress. The PRBS stress represents the closest possible proxy to the waveforms experienced by devices in real logic

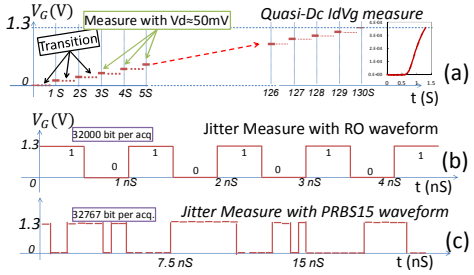


Fig 5: Schematic of **three PBTI "sense" measurements** used following stress/recovery phases. (a) Construction of quasi DC I_D-V_G for ΔV_{th} extraction. RO (b) and PRBS (c) AC gate patterns used to probe stress-induced timing jitter.

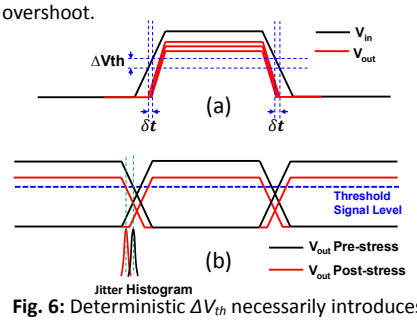


Fig. 6: Deterministic ΔV_{th} necessarily introduces a proportional deterministic time shift in the mean jitter distribution, as schematically shown.

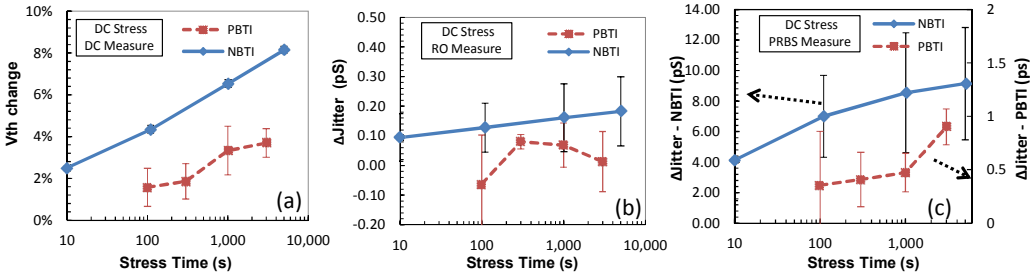


Fig 7: Comparison of NBTI (from [13]) and PBTI degradation as a function DC-stress. (a) V_{th} degradation is clearly evident for both NBTI and PBTI while (b) neither mode induces noticeable increases in jitter when measured via RO waveforms. (c) When jitter is measured via PRBS waveforms, the NBTI/PBTI response is notably larger. This is a good indicator that RO measurements do not capture the relevant random (PRBS) stress-induced jitter.

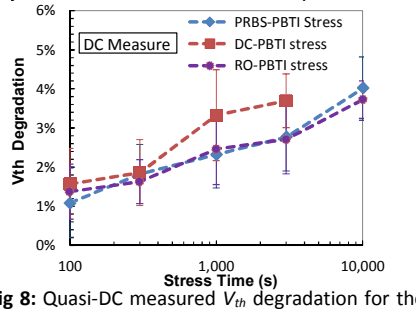


Fig 8: Quasi-DC measured V_{th} degradation for the three modes of PBTI stress including DC-stress, RO-type stress, and PRBS-type stress. The two AC stresses were extended to induce similar V_{th} degradation for all three stress modes.

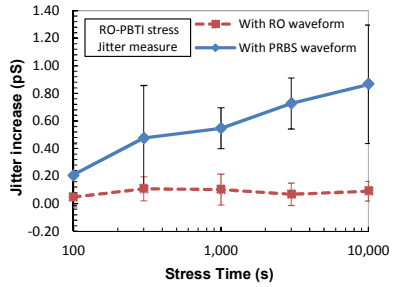


Fig. 9: Random jitter following the AC **RO stress** measured via RO and PRBS waveforms. When measured via RO, no noticeable increase in jitter is observed. However, when measured via PRBS, we note a stress-time dependent increase in random timing jitter.

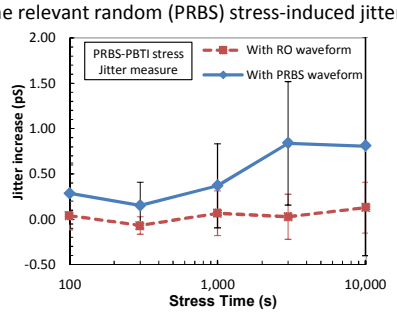


Fig 10: Random jitter increase following the AC **PRBS stress** measured via RO and PRBS waveforms. Similar to the DC and RO stress modes, random (PRBS) timing jitter increase is only observed when utilizing the PRBS measurement waveforms.

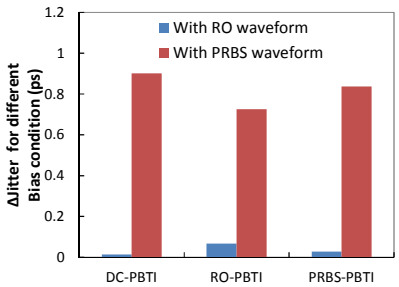


Fig. 11: Summary of the PBTI induced jitter increase for all three stress modes (DC, RO and PRBS). The PRBS jitter measurement successfully captures the jitter increase in all three cases while the RO jitter measurement is unable to capture the degradation. This strongly indicates that RO type test circuits are poor predictors of "real" digital logic.