Circuit Speed Timing Jitter Increase in Random Logic Operation after NBTI Stress

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Abstract: **Recently, much effort has been spent trying to relate NBTI observations to real circuit impacts. While many of these efforts rely on circuit simulation to bridge this gap, an experimental approach is, of course, preferred. In this study we provide this experimental solution in the form of eye-diagram measurements to quantify NBTI-induced changes in timing jitter. We investigate these NBTI-induced jitter increases using a variety of ring-oscillator as well as pseudo-random gate patterns. The pseudo-random gate pattern is a close approximation to real world random logic. We observe that the NBTI-induced jitter increase depends strongly on the chosen gate pattern and is most severe for the pseudo-random case. These observations strongly suggest that more regular gate pattern (ring-oscillator) measurements underestimate the circuit impact of NBTI.**

I. Introduction

The serious implications of NBTI-induced device drift have led to substantial and sustained research efforts [1-6] which have recently grown to include circuit implications [4, 5, 7-10]. These studies employ regular ON-OFF device aging conditions accessible via ring oscillator (RO) test circuits [7-10]. However, "real" digital circuits, instead, subject devices to random bit sequences (random aging conditions). Since it is well known that transient charge trapping and de-trapping dominate most modern NBTI studies [2-5, 11], an intuitive expectation is that random ON (trapping) and OFF (de-trapping) bit patterns will lead to random device parametric shifts and a subsequent increase in random timing jitter. Such random timing jitter cannot be captured in RO type studies. Here we report the first experimental observation of random timing jitter increase due to NBTI by using an eye-diagram methodology measured at real world circuit speed.

It is well established that NBTI in modern devices involves an electric field which supports significant tunneling and a consequently dominant role for charge trapping/de-trapping in the observed ΔV_{th} [2, 6]. The NBTI-induced ΔV_{th} leads to timing shifts on the rising and falling edges of digital logic. A systematic ΔV_{th} leads to a deterministic logic timing shift. In RO-based NBTI investigations, the trapping and de-trapping times are fixed, which only allows for observations of these systematic ΔV_{th}-induced delay shifts [8-10]. All of the proposed design solutions for NBTI deal with such systematic degradations. However, real digital circuits involve random bit patterns leading to random NBTI-induced charge trapping /de-trapping and random timing shifts which, in total, *may be larger than the systematic shifts*. This suspicion has never been properly investigated due to experimental difficulties associated with NBTI measurements at "real" circuit speeds.

In this work, we show that: (1) eye-diagram analysis of digital logic is well suited to study NBTI's impact on random logic and (2) NBTI-induced timing jitter increase associated with random logic is significant. This is consistent with fast transients being larger at shorter time. The very short time scales involved in our measurements (0.5 ns to ~10 μs) are shorter than all transient studies reported.

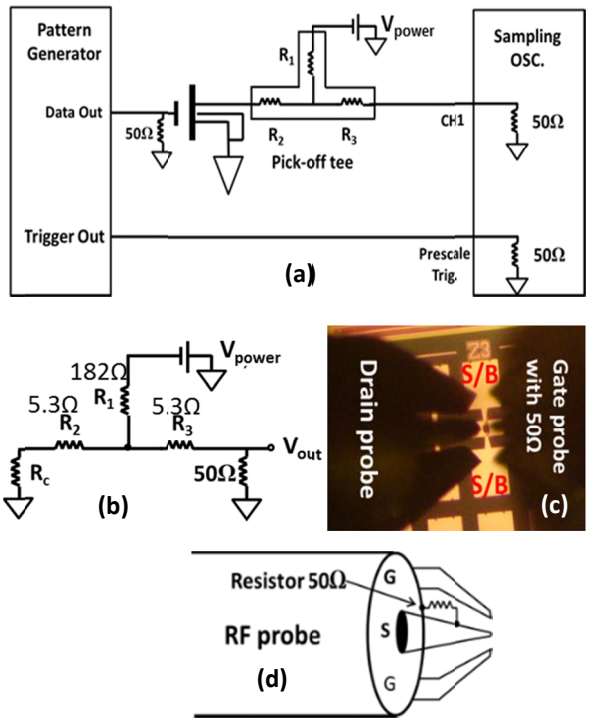

Fig. 1 (a) Experiment setup of the measurement. Transition time (t_r and t_f) of the input signal is 25 ps. All instruments are matched to 50 Ω to maintain signal integrity. (b) Equivalent circuit of transient measurement on drain side. (c) Photo of GSG RF probes and RF electrode patterned pMOSFET. (d) Schematic drawing of gate RF probe with 50 Ω termination allowing reflection-free application of gate patterns.

II. Experimental Considerations

A schematic representation of the experimental arrangement is shown in Fig. 1. In eye diagram measurements, a high-speed pattern generator supplies a user-defined pulse train which is reliably transmitted to the device gate electrode using a high-speed microwave probe in a ground-signal-ground (GSG) arrangement with a micron-sized 50 Ω termination at the probe tip. The transition time (t_r and t_f) of the input signal is fixed at 25 ps by the pattern generator. The drain bias is supplied at the "pick-off terminal" of a pick-off tee. This experimental arrangement also facilitates measurement of the drain current response on the "output terminal" of the same pick-off tee. The drain current response is captured using a high-speed sampling oscilloscope (50 Ω input impedance). Note that as the transistor turns on, the channel resistance drops such that the drain bias is subjected to a droop (as shown in Fig. 1a-b). Careful experimental calibrations (not shown) ensure that this droop is insufficient for the device to leave the saturation regime, thus minimizing the effect.

In this study, we examine the changes in jitter due to 3 different logic patterns chosen to approximate common experimental practices as well as real world random logic. As

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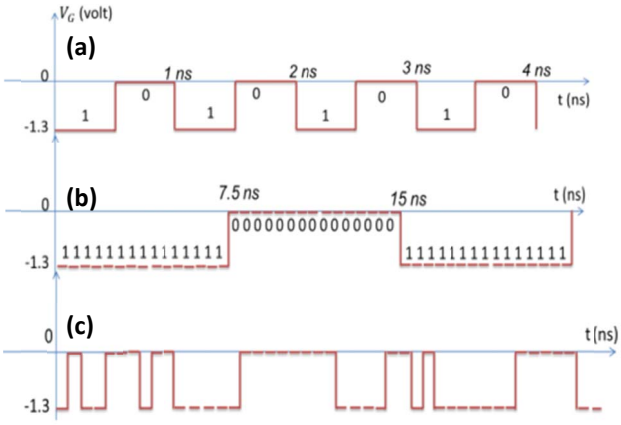

Fig. 2 Schematic drawings of gate input signals. (a) Pattern a (fast RO). (b) Pattern b (slow RO). (c) PRBS15. The input gate pattern bit rate is 2 Gb/s. One bit is 500 ps and has 512 samples.

illustrated in Fig. 2, these patterns include (1) a fast (0.5 ns period) regular RO type pattern (pattern a), a slow (7.5 ns period) regular RO type pattern (pattern b), and a pseudo-random binary sequence of length 2^{15}-1 bits (PRBS15). Eye diagrams are constructed by a repetitive superposition of all these finite length bit segments such that the clock edges are aligned (Fig. 3). In this manner, all drain current responses are captured, allowing jitter in the rising/falling edges to be observed and quantified in a statistical manner.

This study involves (2 nm/1 nm) HfO_2/SiO_2 pMOSFETs (10 × 0.18 μm^2) with GSG layouts. Each device was subject to a repetitive measure-stress-recovery-measure sequence. The "measure" phase consists of eye-diagram construction using ~30,000 bits for each of the aforementioned logic patterns at 100 °C. "Stress" consists of the DC application of V_G = -2 V, $V_S = V_D = V_B$ = 0 V at 100 °C. "Recovery" involves several hundred seconds at 100 °C with all electrodes floating. For each pattern, 18 nominally identical devices from the same wafer were investigated.

For these measurements, jitter is taken as the full width of the jitter distribution at the 50 % threshold signal level. Jitter distributions for the rising/falling edges are extracted

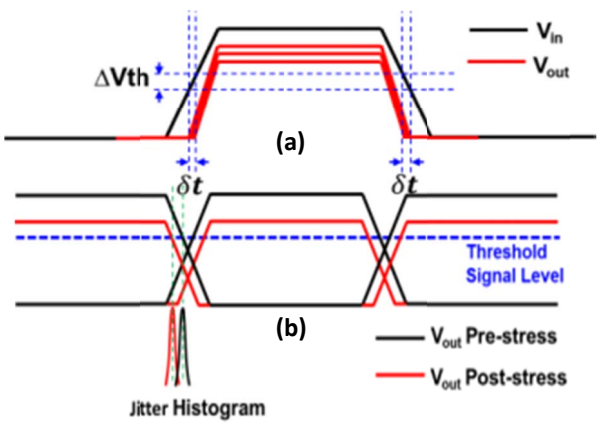

Fig. 3 (a) Gate voltage variation ΔV_{th} induces drain output pulse edge variation, δt, which increases the corresponding jitter. (b) Eye diagram is constructed by repetitively superimposing all the finite length bit segments of a captured waveform. The NBTI-induced ΔV_{th} leads to timing shifts on the rising /falling edges of digital logic.

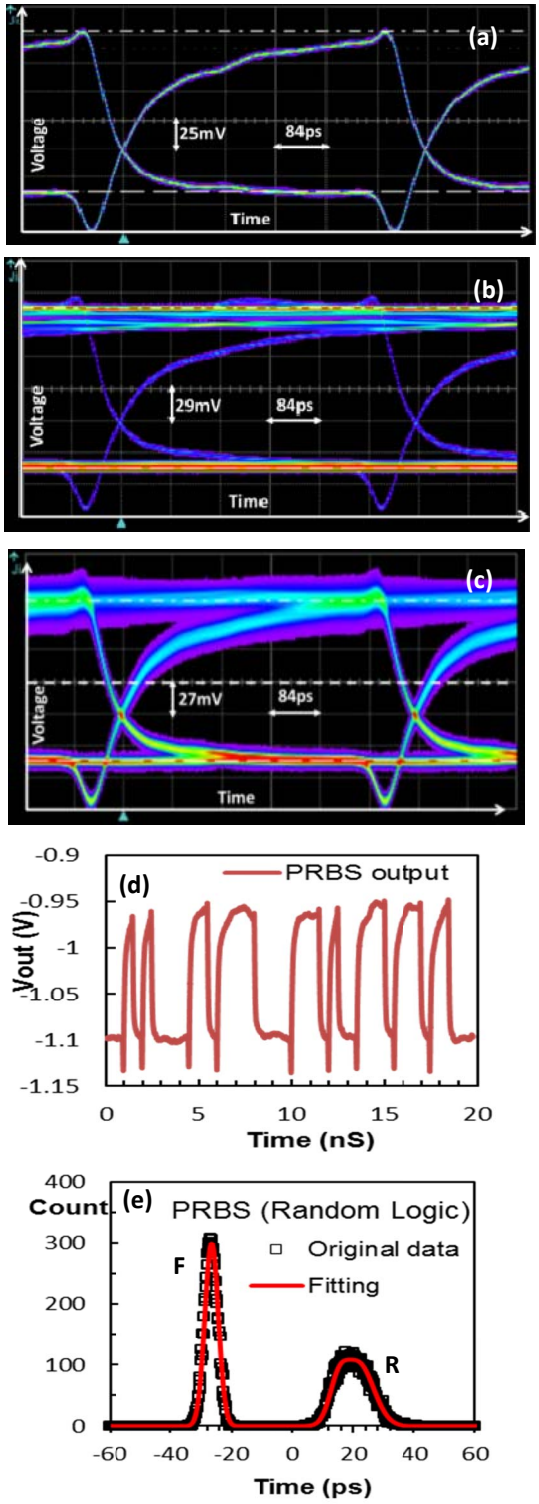

Fig. 4 Typical eye diagram of drain output for 3 input patterns: (a) pattern a, (b) pattern b, (c) PRBS 15. (d) A segment of a PRBS15 output waveform. (e) Extracted jitter histogram from eye diagram at 50% threshold signal level (F (R) is falling (rising) edge).

separately. Pre-stress eye diagrams for the various logic patterns are shown in Figs. 4(a-c). A gate waveform bit rate of 2 Gbit/s was used throughout these measurements; the bit rate was limited by the device probe pad parasitic capacitance (480 fF). This parasitic capacitance manifests as a slow rising edge, non-uniform peak height (Fig. 4d), and is directly responsible for the observed overshoot (peaking at

Table I: Initial jitter value of experimental set-up before stress.

Pattern	a	b	PRBS
Rising edge (ps)	0.89	0.85	31.5
Falling edge (ps)	0.73	0.52	14.58

the rising/falling edges of Figs. 4(a-c)). The jitter of the experimental setup is less than 0.5 ps for RO-like patterns, and less than 2 ps for random logic patterns (PRBS15) (not shown). A representative PRBS15 jitter histogram of the rising/falling edges at 50% threshold are shown in Fig. 4e (initial jitter values for different patterns are listed in Table I).

III. Results and Discussion

Examples of pre- and post-stress I_D-V_G (quasi-DC) in linear and saturation regimes are shown in Figs. 5a and 5b, respectively. Threshold voltage (V_{th}), linear drain current ($I_{D,lin}$) and saturation drain current ($I_{D,sat}$) degradations are shown in Fig. 5c. The corresponding output waveform degradation is shown in Fig. 6a for the fast RO input pattern (Pattern a). Typical timing jitter distributions extracted from the eye-diagrams are illustrated in Figs. 6(b-d) for both rising and falling edges. It is clear that NBTI stress introduces: (1) a timing shift in the peak locations for all patterns and (2) a significant increase in peak widths for PRBS15.

The observed timing shifts, as shown in Figs. 6(b-d), are expected and captured in previous RO type experiments and design solutions to deal with these shifts are widely studied [8-10]. The magnitude of the timing shift is proportional to the magnitude of V_{th} degradation. It is interesting to note that the shift for pattern b is significantly larger than those of pattern a and PRBS15. This is consistent with the longer "on" state of pattern b which facilitates charge trapping at deeper sites or generation of new traps. To quantify these shifts, we performed a series of calibration experiments in which the base level of the gate waveform was artificially shifted to simulate V_{th} shift. In this manner, a timing shift can be approximately correlated to ΔV_{th} (Fig. 7). An examination of

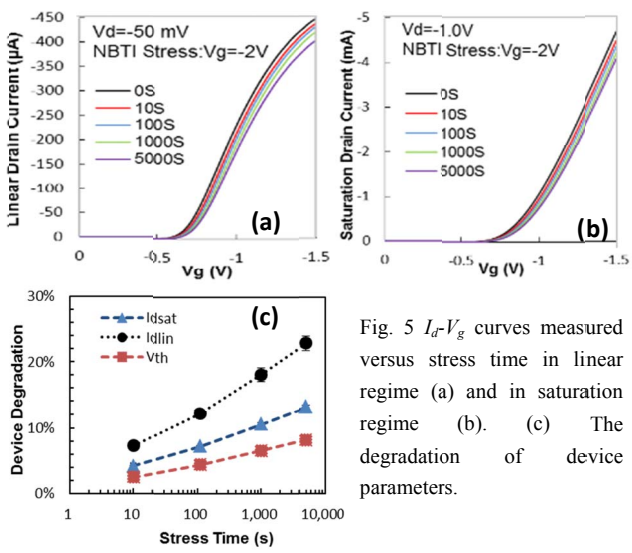

Fig. 5 I_d-V_g curves measured versus stress time in linear regime (a) and in saturation regime (b). (c) The degradation of device parameters.

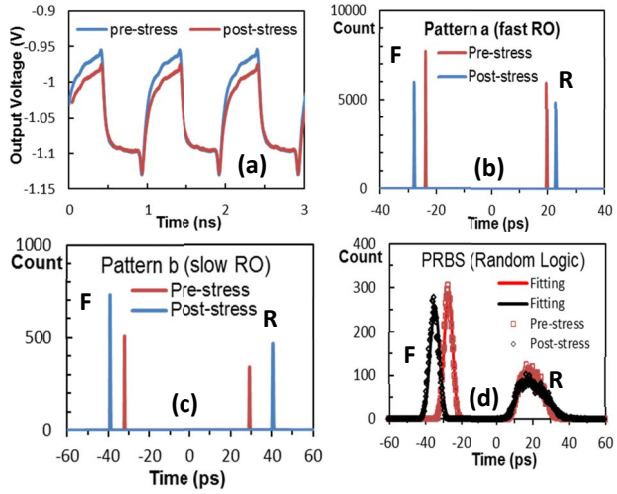

Fig.6 (a) Pre- and post-stress output waveforms of pattern a; Pre- and post-stress jitter histograms extracted from the eye diagrams of (b) pattern a, (c) pattern b, and (d) PRBS15. F (R) is falling (rising) edge.

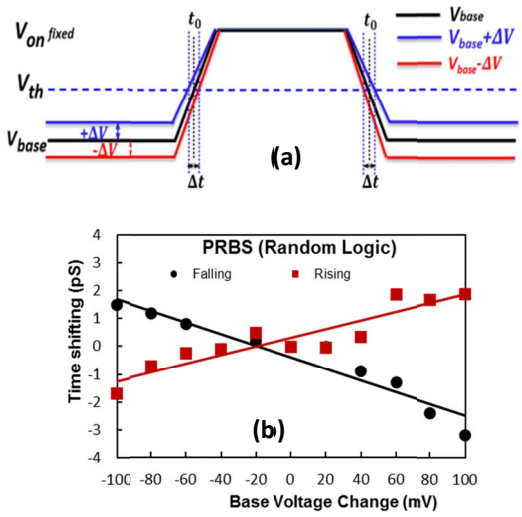

Fig. 7 (a) Artificial shifting of gate waveform base level to simulate a ΔV_{th} induced timing shift. (b) Measured time shift versus the change of base voltage for PRBS15.

the timing shifts in Fig. 7 indicate that a 1 ps timing shift corresponds to ~ 50 mV ΔV_{th}. Clearly, if ΔV_{th} is random, timing shift is also random.

While the timing shift observations are intriguing, the NBTI-induced timing jitter increase, particularly for the PRBS15 case, is the focus of this work. Fig. 8 illustrates the key result of this study; NBTI-induced increase in random timing jitter. The jitter evolves with stress time for both falling and rising edges for all patterns (Fig. 8). The observed jitter increase is negligible for the regular RO patterns (a) and (b), owing to the fixed ON and OFF times. On the contrary, for the PRBS15 pattern, the observed jitter, for both falling and rising edges, increases significantly with stress time. Considering that eye-diagram construction is the superposition of ~30,000 bit segments, the observed NBTI-induced random timing jitter increase is consistent with a stress-induced V_{th} increase due to increased defect density.

We also note that the magnitude of the jitter increase represents a significant obstacle for high-performance

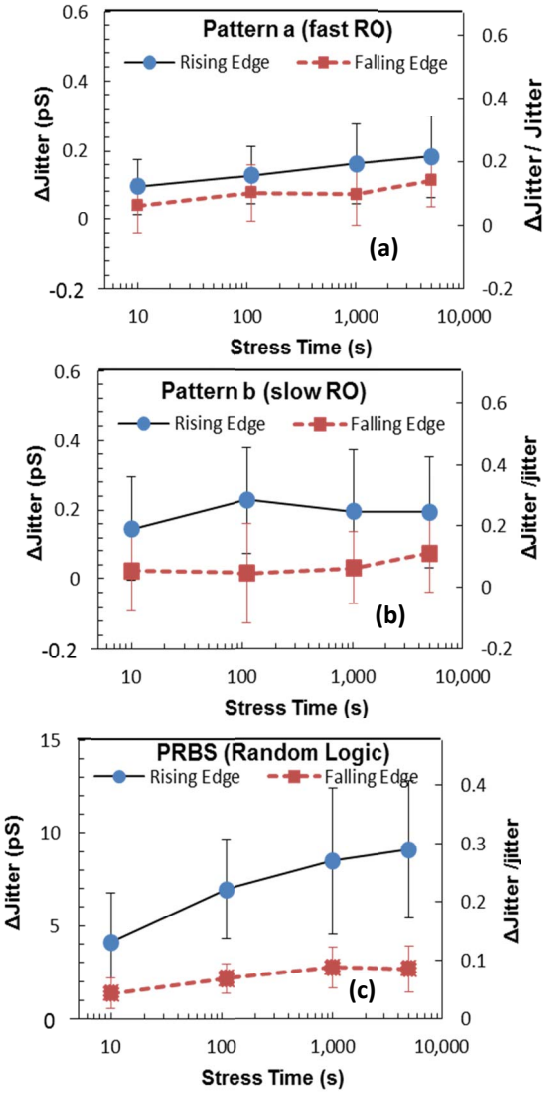

Fig. 8 Jitter degradation versus stress time with standard deviation from 18 devices for (a) regular pattern a (b) regular pattern b; (c) random logic of PRBS15.

circuits. While we recognize that these results are specific to the samples investigated, the mere observation of a pattern-dependent jitter increase is troubling. Furthermore, in a real circuit environment with a large number of devices, the jitter adds statistically such that the observed increase is a serious issue.

IV. Conclusions

The eye-diagram measurement methodology provides a useful tool to investigate the impact of stress-induced defects on high-speed (ps) circuit operation and bridges the gap between conventional reliability measurements and "real" circuit degradation. In this study, we observe a bit pattern-dependent NBTI-induced increase in timing jitter (i.e. the observed jitter depends on the pattern used to measure the jitter). Stressed devices measured using a pseudo-random binary sequence, which closely approximates random logic, exhibited the largest increase. These observations strongly suggest that regular pattern (RO) measurements underestimate the circuit impact of NBTI.

V. Acknowledgments

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VI. References

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