Unusual Bias Temperature Instability in SiC DMOSFET

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***Abstract*— We observe an unusual instability in the SiC DMOSFET transistor characteristics. From a series of bias conditions at elevated temperatures, we conclude that a high density of hole traps in the oxide near the SiO_2/SiC interface are responsible.** **Keywords—SiC; DMOSFET; BTI;**

Introduction

Silicon Carbide power DMOSFETs are starting to become commercially available for power electronics applications [1]. Their high temperature operation, in particular, makes these devices very serious competitors to their silicon counterparts. In addition, the increasing implementation of clean and renewable energies is growing the power electronics market to quadruple in the next decade [2]. However, the quality of the oxide and its interface in SiC MOSFETs remains a concern [3,4] that needs to be addressed in order to build the required confidence for market acceptance.

Among the SiC devices that are being developed for the next generation of high-frequency and power switching applications is the vertical DMOSFET (Fig. 1). The buried p-well channels and the large vertical n-bulk drain are designed to mitigate high electric fields and allow these devices to operate in the range of 1.2-1.7 kV. Despite substantial efforts to improve SiC DMOSFET reliability, device instabilities still persist. Much work has been done to study this degradation under accelerated stress conditions such as high electric field and high temperature [5-7]. In this study we show some unusual instabilities associated with the intrinsic quality of the thermally grown SiO_2 gate oxide and its interface.

Experimental Setup

A group of 16 nominally identical power DMOSFETs (n-channel) with 50nm thermally grown SiO_2 and 200x200 µm active area were studied. The devices characteristics were monitored after a sequence of treatments. Table I shows the details of each treatment condition.

Table I. Summary of stress conditions utilized in this study.

Stress Condition	*Duration (hours)*	*Eox (MV/cm)*	*T (C)*
High temperature treatment	1700	No electrical connection	150
Room temperature storage	1000	No electrical connection	21-24
Positive bias temperature stress	1	2	150
Negative bias temperature stress	1	-2	150
Positive bias Temperature stress	24	2	150
Negative bias temperature stress	50	-2	150
Positive bias Temperature stress	24	2	150

All electrical characterizations were performed at room temperature before and after each stress condition using a parameter analyzer.

In addition, another nominally identical group of 16 devices was kept under a moderately accelerated time -dependent dielectric breakdown (TDDB) inversion stress of 6.78MV/cm at 150°C. The stress was interrupted after 1700 hours to monitor the evolution of the I_D-V_G characteristics during stress.

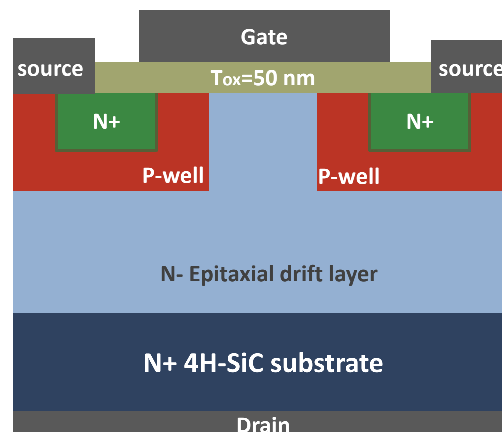

Fig. 1. Cross section of a power DMSOFET

Results and Discussions

Figure 2 shows the evolution of the I_D-V_G characteristics after interruption of the TDDB stress compared to a set of fresh devices (shown by the black lines). The fresh devices used for comparison are from different dies from the same wafer. The tight I_D-V_G distribution of the fresh devices indicates very little die-to-die variability, and in general suggests reasonably good quality devices. The long TDDB stress resulted in a widely spread (generally) negative shift in *Vth*. In general, SiC MOSFETs are known to have a large density of interface states which is apparent in the observed hysteresis (even in the fresh devices). But for the devices that experienced a TDDB stress, the threshold voltage shift is accompanied with a large increase in hysteresis. Thus, the *Vth* shift is an indication of generation of positive charge in the

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gate stack while the hysteresis is a signature of the increased charge trapping.

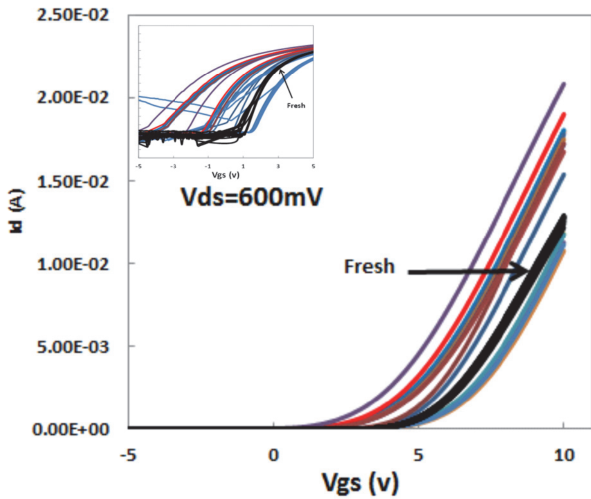

Fig. 2. Progression of I_D- characteristics during TDDB

Unexpectedly, the group of devices that had undergone a long storage at 150°C (adjacent devices to those under TDDB stress) showed a large improvement in ON current (Fig. 3). This improvement of more than 30% in peak *Gm* was accompanied with a decrease in *Vth.* The improved characteristics show a very tight current distribution and no increase in hysteresis which is inconsistent with the creation of new defects such as that observed after TDDB stress.

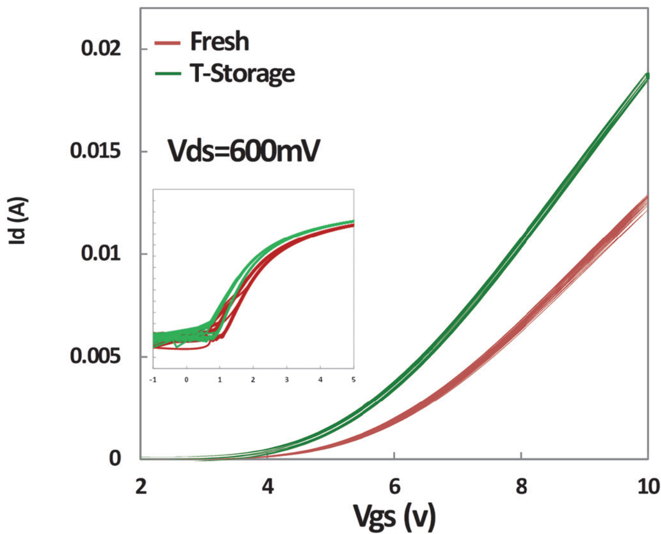

Fig. 3. Large increase in drive current after long storage at 150°C

The origin of this large improvement in performance is often linked to a mobile ion contamination issue. In this scenario, the negatively charged interface traps are compensated by the relocation of positively charged mobile ions closer to the interface. This could conceivably reduce Coulomb scattering by compensating the negative interface trapped charge. This compensation effect has been used to explain why sodium contamination in gate oxide can improve the effective mobility in SiC MOSFET [8-9].

Unfortunately, the improvement in drive current was not permanent. As shown in Fig. 4, after storing the devices for 1000 hours at room temperature the ON current regresses back towards the fresh device levels with a wide spread in current distribution but no *Vth* shift. One possibility is that this regression could result from moisture incorporation as the devices were left in a room temperature air ambient.

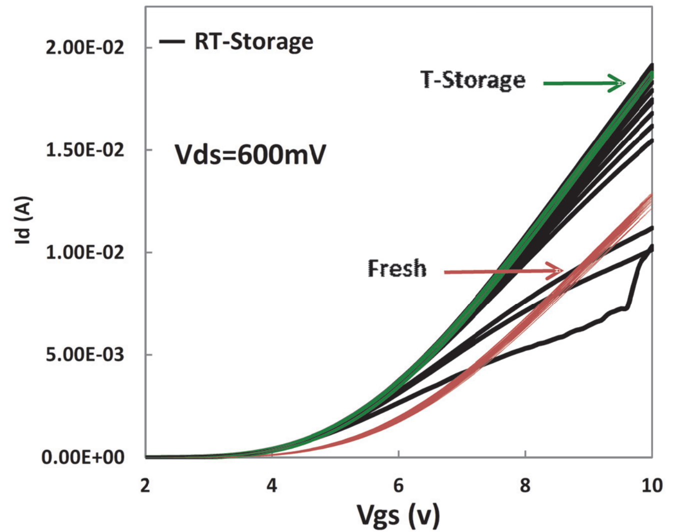

Fig. 4. On current regression after storage at room temperature

To further investigate the possibility of mobile ion contamination, the devices were subject to a series of bias temperature tests. The first of which included a "stress" of 150 C at ±2 MV/cm for 1 hour. Upon the conclusion of each bias temperature stress, the bias was kept continuous while the temperature was removed. This approach was thought to "freeze" the mobile ions close to the interface (PBTI) or at the gate side (NBTI).

Fig.5 shows the I_D-V_G characteristics after 1 hour long PBT and subsequent 1 hour NBT stresses. The ON current shows a tendency to decrease after PBT and increase after NBT but the change is insignificant. In addition, no threshold voltage shift was observed.

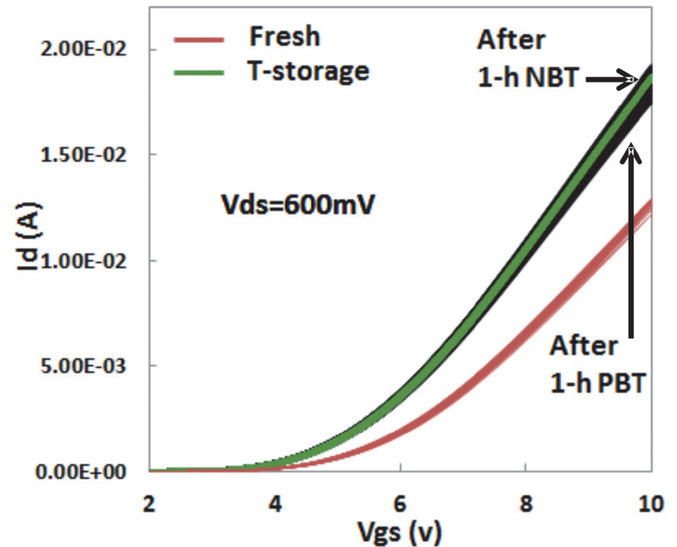

Fig. 5. Current shift after 1-hour long PBT and NBT stress at 150°C.

This unrevealing observation led us to further examine the mobile ion drift kinetics which might be at play in these devices. The most encountered (at least in silicon) mobile ion is sodium. However, sodium is a very unlikely culprit considering its drift velocity at 150°C is so high that it would have traversed the entire 50nm thick oxide within minutes. Our observations must include a larger mobile ion. The next largest column I ion, potassium, would need more than an hour to drift across the dielectric film. Thus, we revisited our earlier bias temperature stresses with a series of longer stresses. The stress sequence consists of a 24 hour PBT stress followed by a 50 hour NBT stress and then followed again by an additional 24 hour PBT stress. Room temperature characterizations took place between each stress. In this fashion, mobile charge can be shuttled back and forth across the dielectric while monitoring the effects on the device electrostatics.

Fig. 6 illustrates that the ON current was significantly reduced after the first 24-hour long PBT. A subsequent 50 hours of NBT stress resulted in a further improved ON current (larger than the temperature storage value). The subsequent (and final) 24-hour long PBT stress shifts the ON current back towards the previous PBT stress value.

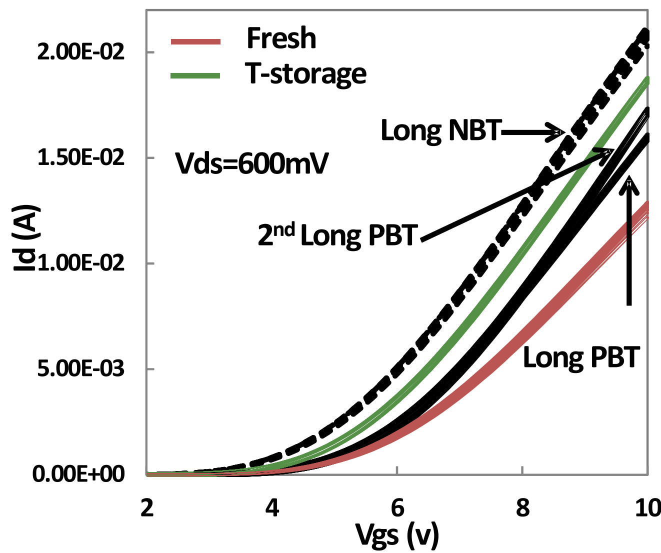

Fig. 6. I_D-V_G characteristcs after long PBT and NBT stresses

Fig.7 summarizes the progression of the average peak *Gm* and threshold voltage *Vth* after each stress condition. If our initial conjecture is correct (mobile ions compensate interface state charges thereby improving mobility), the PBT stress should move the possible mobile ions close to the interface and improve compensation thereby resulting in an increase in mobility. The following NBT stress should then move the mobile ions closer to the gate which should reduce compensation decrease mobility. A close examination of Fig.7, reveals a trend opposite of that expected (*Gm* improves after NBT stress while the PBT stress results in *Gm* degradation as well as a reduction in threshold voltage). Thus, these results are inconsistent with the presence of mobile species in the oxide film and distinctly different than the recent observations involving sodium mobile ion mobility improvement [8-9]

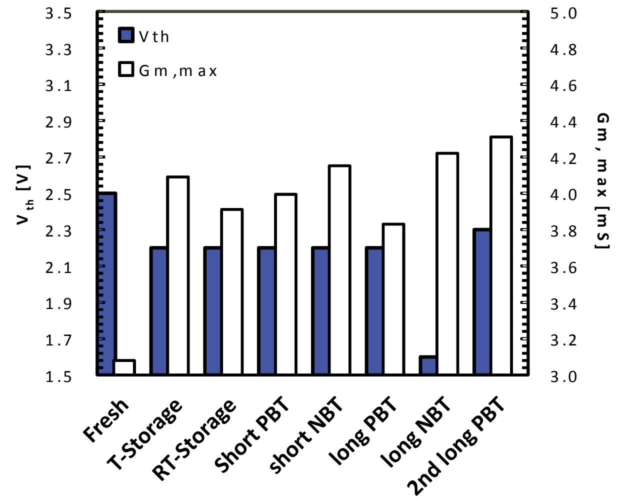

Fig. 7. Average *Vth* and peak G_m after each stress condition.

These observations can however be explained by a high density of hole-traps at energy levels above but near the top of the valence band (Fig. 8). These traps are mostly empty as fabricated. The long temperature treatment filled these traps with holes (thermally). The captured holes reduce the coulomb scattering caused by the negatively-charged interface traps and improve the effective mobility. The holes trapped after the NBT stress also results in a reduction of *Vth.* The PBT stress de-traps the holes which increases the threshold voltage. Note that these hole traps did not significantly contribute during the 1-hour long stresses. This suggests that these hole traps are located slightly deeper compared to the interface traps.

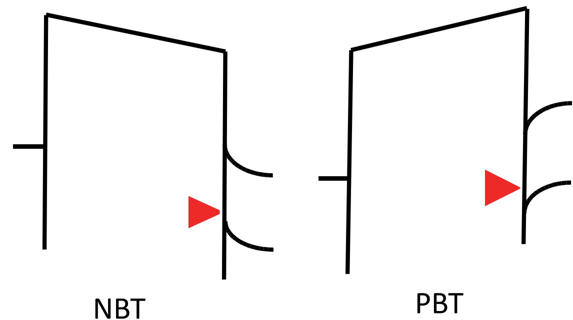

Fig. 8. Hole traps near the interface close to the valence band.

Moreover, no increase in hysteresis was observed until the devices were subject to the longer stresses. Fig.9 illustrates the increased hysteresis after the long PBT stress. Thus, after all holes are detrapped following the long PBT, the subsequent I_D-V_G shows an increase in hole trapping (hysteresis). This indicated that a long PBT frees some spatially shallower traps, to be accessed within the measurement time scale. This hysteresis effect was also observed after the second PBT stress (not shown).

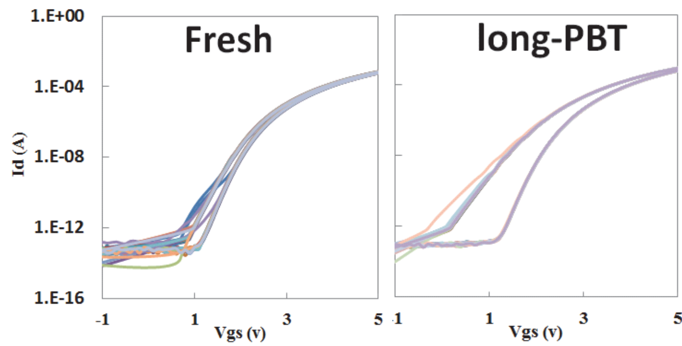

Fig. 9. Larger hysteresis after long PBT indicates larger charge trapping

Conclusion

A set of "strange" instability phenomena associated with SiC DMOSFET is observed. While it is widely known that high density of defects exist at the band edge for these devices, the consequences are not well appreciated. Our observations suggest that there is a (very surprising) thermally assisted activation of band edge hole-traps under very moderate operating conditions.

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