Fast-Capacitance for Advanced Device Characterization

P. Shrestha^{1,2}, K. P. Cheung^{1,*}, J. P. Campbell¹, J. T. Ryan¹ and H. Baumgart^{2,3}
¹Semiconductor and Dimensional Metrology Division, NIST, 100 Bureau Drive, Gaithersburg, MD 20899
²Old Dominion University, Norfolk, VA 23529, ³Applied Research Center, Newport News, VA 23606
*email: kpckpc@ieee.org, phone: 301-975-3093, fax: 301-975-8069

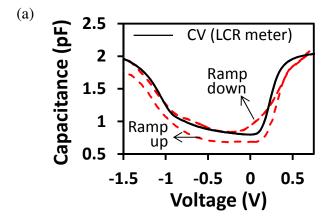
Abstract—Fast-CV measurements are frequently being used to study transient phenomena associated with advanced devices. In this study, we show that many artifacts plague this measurement and then provide a proper method to legitimize fast-CV measurements as trustworthy. We show a remarkably accurate correspondence between a complete fast CV measurement, from accumulation to inversion, and a conventional CV measurement on the same device. The results distinguish fast-CV as a powerful tool for device characterization and reliability measurements.

Keywords—Fast-CV; capacitance measurements; transient characterization

I. INTRODUCTION

Transient phenomena, which impact the performance and reliability of advanced devices, have captured a lot of recent attention [1-4]. Both charge pumping and fast-IV have been used extensively to characterize the post-stress degradation and trap filling aspects of these transient phenomena [5-8]. However, the complex nature of transient phenomena has lead researchers to examine the feasibility of using fast-CV [3, 9-12]. Fast-CV measurement artifacts have limited its usage to merely a monitor of stress-induced deviations in accumulation capacitance [3,9, 12-14]. In this work, we present a methodology to measure the full fast-CV characteristic accurately. These results establish fast-CV as an extremely powerful tool for present and future advanced device characterization and reliability studies.

As shown in Fig. 1a, the as-measured fast-CV without using our methodology is error ridden and can lead to a misinterpretation of the results. With careful consideration of the experimental approach and the sources of measurement error, accurate and precise fast-CV measurements are readily possible, as shown in Fig. 1b. In this study we identify and eliminate the major error sources to achieve accurate fast-CV device characterization.



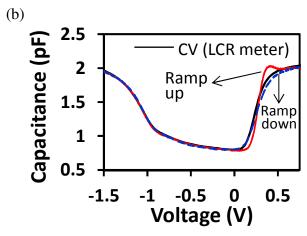
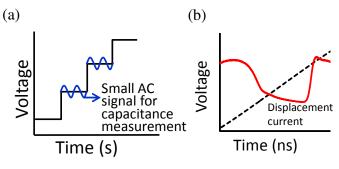


Fig. 1. a) Erroneous fast-CV and b) accurately measured fast-CV during ramp-up and ramp-down. a) is an example of the susceptibility of fast-CV to measurement errors. b) is obtained by careful consideration of the experimental approach and the sources of error on the same device as in a).

II. EXPERIMENTAL

For conventional CV measurements utilizing an LCR meter, the gate voltage (V_G) is stepped slowly (minutes) between accumulation and inversion with a phase sensitive impedance measurement at each V_G step as shown in Fig. 2a. In the fast-CV measurement, V_G is subject to a fast (100's of ns) trapezoidal pulse spanning accumulation to inversion while the displacement current is monitored during the entire sweep (Fig. 2b). The result is two fast-CV curves for each pulse (ramp-up/ramp-down). A simple schematic of the

experimental set-up for fast-CV is shown in Fig. 2c. The voltage is applied at the gate using a pulse generator. The transient current through the substrate, source and drain is measured using a current amplifier. Conventional CV (LCR) and fast-CV measurements were all performed on $10~\mu m \times 10~\mu m$ nMOSFETs with 1.6 nm EOT SiON gate dielectrics. All conventional CV measurements were performed at 1 MHz. For simplicity, pad capacitance has not been corrected for in any of the measurements.



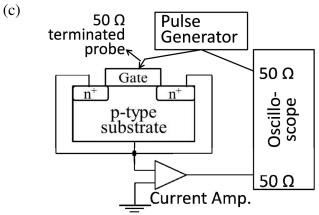


Fig. 2. Schematic diagram of a capacitance measurement using a) an LCR meter b) fast-CV. For a) the voltage is swept at a very slow rate and a small ac signal is applied at each step to measure the capacitance using a phase sensitive detector. c) experimental set up of the fast CV measurement.

The measured fast-CV transient current, as presented in Fig. 2b, is the summation of displacement current ($I_{displacemnet} = C^*(dv/dt)$) and leakage current through the gate dielectric. Fig. 3a shows this transient current waveform. Fig. 3b shows the leakage current waveform obtained by slowing the V_G ramp rate by a factor of 1000. The slower ramp rate ensures that the displacement current is a negligible component of the total measured current. The purely capacitive displacement current waveform (Fig. 3c) can be obtained by subtracting the leakage (Fig. 3b) from the measured transient current (Fig. 3a). Knowing the ramp rate (dv/dt) of gate voltage (V_G), the CV characteristic can be extracted using the displacement current ($I_{displacemnet} = C^*(dv/dt)$). The extracted value of the capacitance versus the V_G is shown in Fig. 3d.

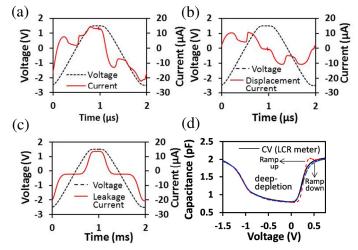


Figure 3. Fast CV waveform response to a ramp voltage applied to the device. a) the measured transient current is equal to the displacement current plus the leakage current through the gate. b) 1000x smaller ramp voltage compared to a) to measure leakage current. c) displacement current obtained after subtracting the leakage current. d) fast-CV curve obtained using the displacement current shown in c).

III. MEASUREMENT CONSIDERATIONS AND DISCUSSION

As shown in Fig 1 one can easily obtain a fast CV curve that is plagued with measurement artifacts and far from the actual CV. Some of the measurement considerations to avoid such artifacts and there impact on the interpretation of the CV measurement are discussed below.

Delays associated with cable length and amplifier can result in small timing skews between the V_G pulse and the measured current waveform. If unaccounted for, this skew mimics a flatband voltage shift and can easily be misinterpreted. One such example is shown in Fig. 4. Small skew in the actual and the measured V_G as shown in the inset of the Fig. 4a leads to shift in the ramp up and down CV curve in reverse direction as shown in Fig. 4b. This difference in the ramp up and down CV curve can easily be mistaken as the difference in the flatband shift during ramp up and down. Furthermore, for a fixed timing skew, a faster ramp rate leads to a larger discrepancy between ramp-up /ramp-down CV curves. This rise time-dependent CV curve shift can easily be mistaken as a device transient phenomenon and lead to a misinterpretation of the device physics [13].

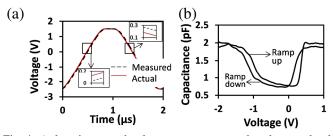


Fig. 4. a) skew in ramped voltage sweep compared to the actual voltage sweep and b) resultant CV curve skew due to the ramped voltage skew in a). The CV curve during ramp-up shifts to the negative voltage as the measured voltage sweep is lower than actual voltage. The same is true during ramp-down.

2013 IIRW FINAL REPORT 27

Another important factor is the bandwidth limitation of the current amplifier. Fig. 5 compares a fast CV measurement with the LCR meter CV. The fast CV in Fig 5 clearly does not follow the LCR meter measurement. This is due to the slow response of the amplifier while measuring $I_{displacement}$. The bandwidth must be sufficient to capture the displacement current which is the capacitance transient. Note that this *much* faster than the rise time of the V_G pulse. Fig 5 clearly shows that fast CV measured with slow amplifier would lead to an incorrect estimation of threshold voltage, V_{th} .

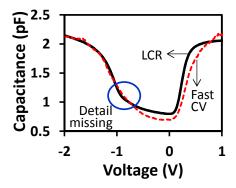


Fig. 5. Plot comparing LCR meter CV and fast-CV done at 25 MV/s using an amplifier with 14 MHz bandwidth. This bandwidth is insufficient to correctly capture the displacement current in response to the ramped voltage. For this particular measurement, an amplifier with 62.5 MHz of bandwidth is required.

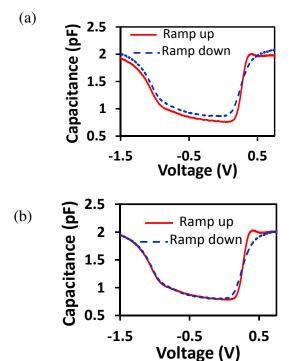


Fig. 6. Ramp-up and ramp-down CV curve a) with and b) without error in correcting temperature dependent amplifier offset. If the offset measurement is not done at the time of CV measurement, the measured offset might deviate from the actual offset leading to erroneous results.

Current amplifiers also have an inherent temperature sensitive DC offset which can result in an apparent DC shift in ramp-up/ramp-down capacitance. Fig 6 shows ramp-up/ramp-down with (Fig 6a) and without (Fig 6b) DC offset error in the displacement current measurement. This offset must be properly calibrated within the same time frame as the fast-CV measurements to minimize temperature drift induced offset errors. Otherwise, the fast-CV measurements which fail to account for amplifier offset can easily result in erroneous t_{ox} .

A careful examination of the fast-CV characteristics in Fig. 7a reveals a systematic discrepancy between the ramp-up/ramp-down inversion transitions. This error is due to deep depletion (even though a transistor is used). For these relatively large area devices ($10 \times 10 \ \mu m^2$), there is not enough time (during the fast ramp pulse) for inversion carriers to diffuse from source and drain regions into the channel as shown in Fig 7b. The time taken for the inversion charges to diffuse certain distance L is given by the equation in the inset of Fig 7b. The deep depletion [15] issue is more pronounced for ramp-up as inversion is already established during ramp-down. Ramp-up/ramp-down deep depletion discrepancies can be avoided by better matching ramp rates with appropriate channel lengths.

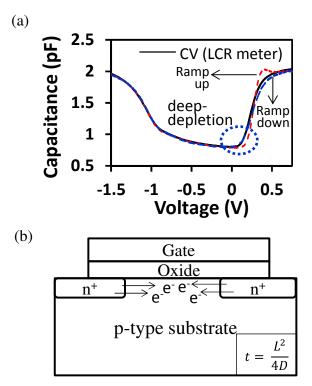


Fig. 7. a) Fast-CV obtained during ramp-up and ramp-down compared to CV with LCR meter on device with 10 μm channel length with deep-depletion occurring at inversion and b) schematic showing inversion carrier diffusion from source and drain during inversion. It is the time taken by the inversion carriers to diffuse into the channel of length L in a substrate with diffusion coefficient of D.

28 2013 IRW FINAL REPORT

Intuitively, fast-CV measurements can handle highly scaled devices (small capacitances) via an increase in the V_G ramp rate. This makes the displacement current larger therefore making it easier to measure. Since the ramp rate is higher, amplifier with larger bandwidth will be required. Therefore the key limiting factor is the current amplifier as larger bandwidth usually leads to higher noise. If proper care is taken to choose the appropriate amplifiers and careful experimental set-up, we expect this approach to extend the fast-CV measurement to \approx 1fF level.

IV. CONCLUSION

Fast-CV can be an accurate and trustworthy technique which (with proper measurement care) is well suited to characterize highly scaled devices. Measurement artifacts due to careless high speed measurements and error inflicted by choice of amplifier are some of the challenges limiting highly accurate fast CV measurements. However, none of these challenges are impossible to resolve. We have discussed how all of these possible errors should be approached and outlined a methodology to correct for them. Thus, this approach opens up the efficacy of fast CV measurements for future studies of a variety of transient phenomena.

REFERENCES

- [1] T. Grasser, H. Reisinger, P. J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The Time Dependent Defect Spectroscopy (TDDS) for the Characterization of the Bias Temperature Instability," 2010 International Reliability Physics Symposium, pp. 16-25, 2010.
- [2] R. S. Scott, N. A. Dumin, T. W. Hughes, D. J. Dumin, and B. T. Moore, "Properties of High Voltage Stress Generated Traps in Thin Silicon Oxides," 1995 IEEE International Reliability Physics Proceedings, 33rd Annual, pp. 131-141, 1995.
- [3] D. Veksler, G. Bersuker, H. Madan, L. Vandelli, M. Minakais, K. Matthews, C. D. Young, S. Datta, C. Hobbs, and P. D. Kirsch, "Multi-technique study of defect generation in high-k gate stacks," 2012 Ieee International Reliability Physics Symposium (Irps), 2012.
- [4] E. Cartier, A. Kerber, T. Ando, M. M. Frank, K. Choi, S. Krishnan, B. Linder, K. Zhao, F. Monsieur, J. Stathis, and V. Narayanan, "Fundamental Aspects of HfO2-based High-k Metal Gate Stack Reliability and Implications on t(inv)-Scaling," 2011 IEEE International Electron Devices Meeting (Iedm), 2011.
- [5] A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of the V-T-instability in SiO2/HfO2 gate dielectrics," 41st Annual Proceedings:

- International Reliability Physics Symposium, pp. 41-45, 2003.
- [6] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumot, and F. Martin, "Characterization and modeling of hysteresis phenomena in high K dielectrics," IEEE International Electron Devices Meeting 2004, Technical Digest, pp. 737-740, 2004.
- [7] D. S. Ang, G. A. Du, Y. Z. Hu, S. Wang, and C. M. Ng, "Energy distribution and electrical characteristics of NBTI induced Si/SiON interface states," 2008 IEEE International Reliability Physics Symposium Proceedings - 46th Annual, pp. 737-738, 2008.
- [8] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, B. Zhao, K. Matthews, G. A. Brown, and G. Bersuker, "Interfacial layer dependence of HFSi(x)O(y) gate stacks on VT instability and charge trapping using ultra-short pulse in characterization," 2005 IEEE International Reliability Physics Symposium Proceedings 43rd Annual, pp. 75-79, 2005.
- [9] D. R. Aguado, B. Govoreanu, W. D. Zhang, M. Jurczak, K. De Meyer, and J. Van Houdt, "A Novel Trapping/Detrapping Model for Defect Profiling in High-k Materials Using the Two-Pulse Capacitance-Voltage Technique," IEEE Transactions on Electron Devices, vol. 57, pp. 2726-2735, Oct 2010.
- [10] G. Puzzilli, B. Govoreanu, F. Irrera, M. Rosmeulen, and J. Van Houdt, "Characterization of charge trapping in SiO2/Al2O3 dielectric stacks by pulsed C-V technique," Microelectronics Reliability, vol. 47, pp. 508-512, Apr-May 2007.
- [11] Z. A. Weinberg, M. V. Fischetti, and Y. Nissancohen, "Sio2-Induced Substrate Current and Its Relation to Positive Charge in Field-Effect Transistors," Journal of Applied Physics, vol. 59, pp. 824-832, Feb 1 1986.
- [12] W. D. Zhang, B. Govoreanu, X. F. Zheng, D. R. Aguado, A. Rosmeulen, P. Blomme, J. F. Zhang, and J. Van Houdt, "Two-pulse C-V: A new method for characterizing electron traps in the bulk of SiO2/high-k dielectric stacks," IEEE Electron Device Letters, vol. 29, pp. 1043-1046, Sep 2008.
- [13] T. L. Duan and D. S. Ang, "Capacitance Hysteresis in the High-k/Metal Gate-Stack from Pulsed Measurement," IEEE Transactions on Electron Devices, vol. 60, pp. 1349-1354, Apr 2013.
- [14] M. Rosmeulen, E. Sleeckx, and K. De Meyer, "Electrical Characterisation of Silicon-Rich-Oxide Based Memory Cells Using Pulsed Current-Voltage Techniques," in Solid-State Device Research Conference, 2002. Proceeding of the 32nd European, 2002, pp. 471-474.
- [15] E. H. Nicollian and J. R. Brews, MOS (metal oxide semiconductor) physics and technology. New York: Wiley, 1982.

2013 IIRW FINAL REPORT 29