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This work examines Si overgrowth to encapsulate 3C-SiC quantum dot arrays epitaxially grown on Si substrates. Using transmission electron microscopy, we show how the crystalline quality of the Si cap depends on the growth conditions. Overgrowth at 300 °C leads to a planar, epitaxial Si cap, but with small crystallographic rotations in the cap above each quantum dot. At 400 °C growth temperature, Si exhibits reduced sticking to the SiC, leading to a non-planar cap. However, a two-step process, with thin layer grown at 250 °C followed by growth at 500 °C, leads to a planar cap with a much-reduced density of defects. © 2014 AIP Publishing LLC.
[http://dx.doi.org/10.1063/1.4859695]

The ability to deterministically localize charge or spin on precisely defined nanostructures at below 10 nm length scales could enable new paradigms in logic devices.[1,2] Such localization can be achieved in principle via directed self-assembly methods that strongly constrain quantum dot nucleation and growth, although getting to the nanometer length scale remains very challenging.[3–7] A method developed by Guise *et al.*, created arrays of nanoscale silicon carbide quantum dots, which were formed by electron beam induced deposition (EBID) of carbon nanodots, followed by thermal conversion to SiC, on the Si (001) surface.[8] Guise *et al.*, achieved well-ordered, highly monodisperse arrays of SiC quantum dots (QDs), with resultant interdot spacings down to 35 nm. Recently, Petz *et al.*, showed that the SiC quantum dots were the 3C polymorph, and cube-on-cube epitaxially aligned to the Si (001) substrate.[9] They created patterned arrays of these dots with interdot spacings as small as 22 nm.

The intent of these prior studies was to use the SiC dots to guide the nucleation of Ge quantum dots during subsequent molecular beam epitaxial (MBE) growth. In this work, we focus on the SiC dots themselves, in particular, examining how epitaxial overgrowth of Si to encapsulate the array can be controlled to minimize extended defect formation. A two-step capping process is found to accomplish this by providing high Si/SiC sticking during initial cap deposition at low temperatures, and then recovering fully oriented, epitaxial growth during final capping at elevated temperatures. This provides an enabling technology for integrating SiC QDs with Si, with potential applications to spintronics and optoelectronics.

SiC quantum dots were written by EBID. The EBID process and subsequent conversion to SiC are reported in detail elsewhere.[10,11] In brief, the SiO$_2$ native oxide was stripped in HF prior to loading in an electron beam lithography system. Focused electron beam irradiation of ambient hydrocarbon adsorbates on the Si (001) surface yielded square arrays of islands of amorphous carbon, referred to here to as aC:H.

Next, the templated nanodots were exposed to UV-ozone to eliminate excess hydrocarbon contamination. The wafers were then heated to 500 °C for 3 h in an ultra-high vacuum (UHV) MBE chamber (base pressure = 1.3×10^{-8} Pa). This dwell was found to be critical to control the dot size distribution.[12] During subsequent SiO$_x$ desorption at 780 °C, the aC:H nanodots convert to 3C-SiC.[9] Ge, 1 monolayer (ML) to 3 ML thick, was then deposited at 600 °C. Finally, the SiC QDs were encapsulated by Si overgrowth. In this study, we used three different capping strategies: (1) all low temperature (300 °C), (2) elevated temperature (400 °C), and (3) two step capping, 5 nm at 250 °C followed by 45 nm at 500 °C. Typically, low capping temperatures are chosen to ensure conformal Si growth;[13] however, this may be at the expense of crystalline quality.

Select samples were examined in cross-section by high-resolution transmission electron microscopy (HR-TEM) and high-angle annular dark field (HAADF) scanning transmission electron microscopy. Specimens were prepared by focused ion beam lift-out and thinning using a Ga$^+$ beam down to 1 keV. Samples were only examined in the ⟨110⟩ zone axis. The thin Ge layer here serves primarily as a marker for ease of delineating the interface between the Si cap and the substrate; owing to the greater atomic number, this layer is significantly higher contrast under HAADF imaging conditions. At thicknesses below 4 monolayers, Ge grows as a planar, coherent layer, and does not affect the cap morphology. Further, we showed in Ref. 9 that Ge does not accumulate on the SiC nanodots under these growth conditions, and thus will not affect the capping results shown herein.

Figure 1(a) shows a SiC nanodot at the substrate interface, formed using a 1 pAs electron dose per site to write the original aC:H features. This is one QD from a large, square array with 50 nm inter-dot spacing; details of SiC QD structure, size, and evolution are described elsewhere.[9] Important to note here is that the 3C-SiC QDs are epitaxially aligned with the Si substrate in cube-on-cube orientation, but for the
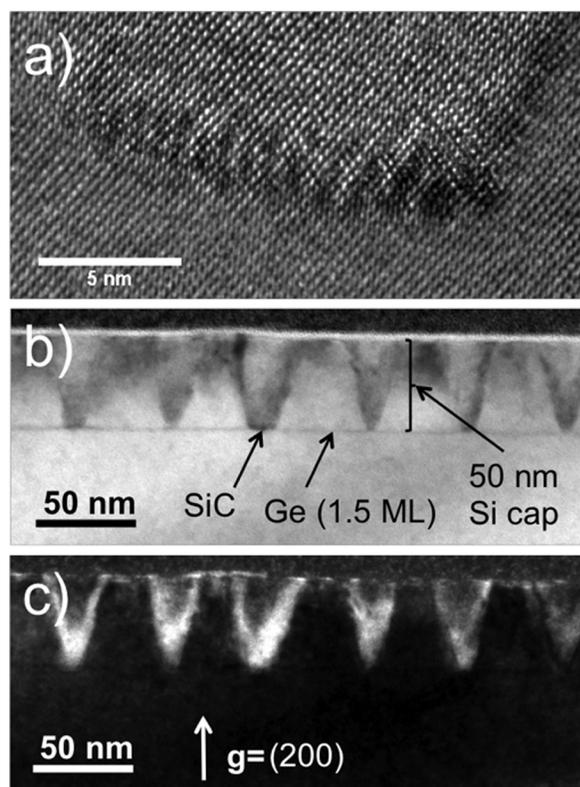
FIG. 1. (a) HR-TEM micrograph of a SiC nanodot with observed Moire fringing. (b) Low magnification bright field image of 300 °C Si capping layer over the SiC QDs. (c) WBDF image of the same area with $\mathbf{g} = (200)$.

QD shown in Fig. 1(a)), a 2° tilt about the $\langle 110 \rangle$ zone axis, relative to the Si lattice, was observed. Si encapsulation of the QDs at 300 °C leads to V-shaped regions above each SiC. The angle of the V-region sidewall does not correspond to any low-index crystallographic facet. Figs. 1(b) and 1(c) compares bright field (BF) and weak beam dark field (WBDF) with $\mathbf{g} = (002)$. The latter shows that local strain is present in the V-regions near the boundary with the Si matrix.

High-resolution micrographs of the boundary of one V-region are shown in Figs. 2(a) and 2(b). The low temperature Si cap layer is fully epitaxial with the Si substrate. The V-regions likely contain {111} stacking faults, although these remain mostly localized to the boundary itself. Furthermore, by plane-tracing, we find that the (002) atomic planes are continuous across the dark boundary, whereas (111) planes are not. Bragg filtering (inverse-fast Fourier transform) around the (111) and (002) spots (not shown), also supports the presence of a $^1/_2$ plane disregistry error along the {111}. This disregistry along only a single set of atomic planes suggests uniaxial rotation of the material inside the V relative to the matrix, with an axis perpendicular to the continuous plane set, i.e., (002). To confirm this, we employ microdiffraction, shown in Figs. 2(c) and 2(d), from areas inside the V-region and from the unperturbed Si matrix (labeled s2 and s1 in Fig. 2). Using image simulation, the Kikuchi pattern under small rotations is calculated and compared to experimental results allowing determination of the exact zone axis. From the observed data, we calculate that the material inside the V-region has a rotation of $1.8 \pm 0.1°$, about a [001] axis.
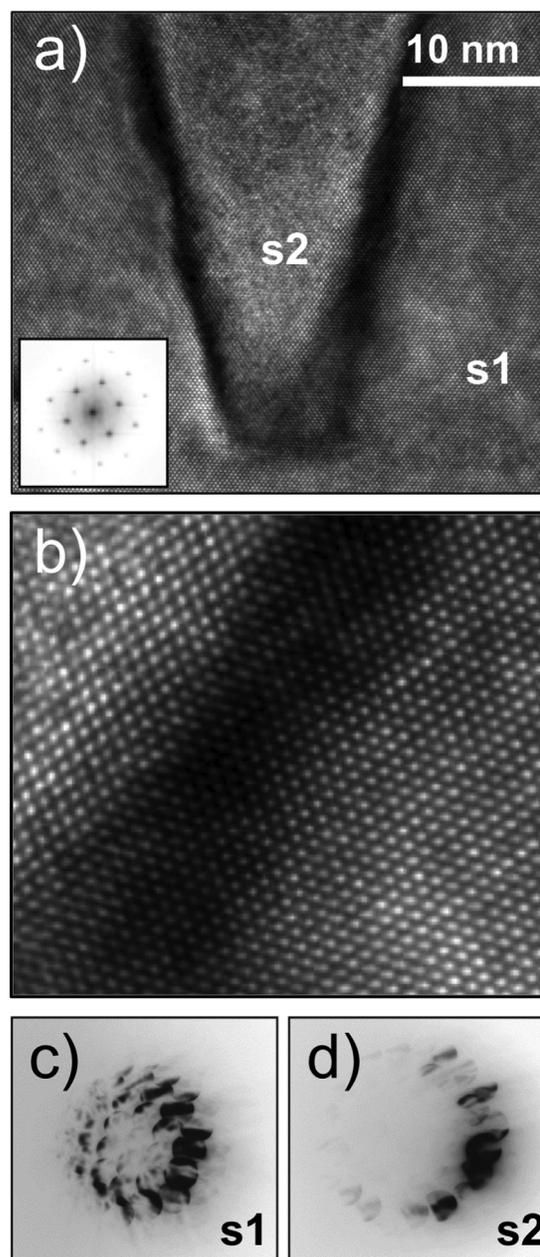

FIG. 2. (a) HR-TEM image of a Si defect V (inset is a corresponding fast Fourier transform of the image). (b) Higher magnification image of the V boundary in (a). (c) and (d) Kikuchi lines from microdiffaction in regions labeled s1 and s2 in (a).

The V-regions of the Si cap have a *twist* misorientation relative to the underlying SiC, but a *tilt* misorientation relative to the surrounding Si matrix. The overall misorientation directly implies that Si cap overgrowth occurred via independent nucleation of Si on the SiC (001) surface, rather than by lateral overgrowth from the matrix. Since we show below that Si wetting of SiC is unfavorable, this further suggests that on-top nucleation of the Si is fostered by reduced surface diffusion of Si on SiC (001) at 300 °C. Although extended defects are not directly observed in the cap layer, the rotation about [001] creates a low-angle tilt grain boundary in the Si cap, implying the presence of geometrically-necessary edge dislocations threading up the V-region boundary. Since the tilt is small, however, only a few dislocations per V-region are required.

Higher growth temperatures were examined in an attempt to avoid extended defects and epitaxial misorientation above the SiC. Fig. 3 shows that for 10 nm Si encapsulation at 400 °C, pyramidal pit formation occurs above each template site, with a distribution of sizes likely related to the variation in carbide size.[12] None of the pits extend back to the original interface. The pits appear faceted, although the sidewall angles (10°–12°) and orientations do not correspond to known facets on the Wulff surface of bulk Si. Note that pits were not observed in the Si cap growth at 300 °C, despite the significant defectivity. Pit formation could occur for several reasons. Inhomogeneous strain associated with buried defects and the carbide particles could lead to reduced Si growth rates above the carbides. However, we reject this as a primary mechanism given the lack of pit formation in the defective caps grown at 300 °C. Reduced sticking of Si to the SiC itself, associated with high interfacial energy, would lead to pit formation in the early stages of cap growth, as Si condensing on the carbide from the vapor diffuses off the nanodot to the nearby Si regions. The resulting pit might persist transiently even once the carbide is finally covered (assuming some non-zero sticking) if Si surface diffusion at 400 °C is insufficient to allow full replanarization. Finally, if there is residual unreacted carbon, it could segregate on the growth surface, leading to reduced Si attachment. We think this mechanism is more likely in larger SiC nanodots described below.

In an attempt to redress these issues, we employed a two-step capping process, where the first 5 nm of Si is deposited at 250 °C, to suppress Si migration off the SiC, followed by 45 nm of Si at 500 °C to reduce subsequent defectivity. Figure 4 shows two epitaxially embedded SiC nanodots formed using a 1 pAs electron dose per site. We note the absence of the V-shaped misorientation regions, or any extended defects. Since the SiC QDs are known to be mostly strain relaxed (the lattice mismatch strain is 20%),[14–18] the QDs must each be bounded by an array of closed misfit dislocation loops, leading to an incommensurate interface with the surrounding Si. When larger carbide precipitates are overgrown, as shown in Fig. 5, some propagation of defects into the cap occurs, although the spatial extent is still quite limited compared to the single-step growth at 300 °C. Pit formation is observed at the free surface of the cap in XTEM (AFM was not performed on these samples prior to sectioning), indicating reduced Si sticking above these larger carbide QDs. As mentioned above, in addition to reduced Si accumulation in the early stages of overgrowth, these larger precipitates could contain some unreacted carbon that can segregate onto the growth surface of the cap and affect the morphology.

In conclusion, we find that by controlling the growth kinetics we can control Si/SiC-QD overgrowth to minimize lattice rotations, extended defectivity and surface roughening. At 300 °C growth temperatures, Si overgrowth leads to fully conformal coating, but allows local formation of faults and lattice misorientation in the Si layer above each templated SiC site. At 400 °C, reduced Si sticking on the SiC leads to partial rejection of Si from SiC, forming shallow pyramidal pits in the cap. Greatly improved crystalline quality is observed when employing a two-step capping procedure. Kinetically-limited   adatom   diffusion   during   initial
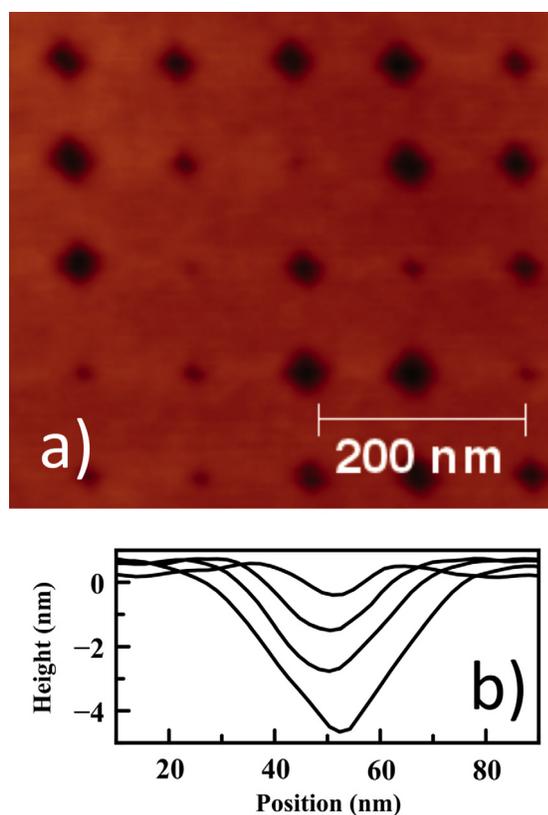

FIG. 3. (a) Atomic force micrograph showing surface of the 10 nm thick Si layer, grown at 400 °C, capping a SiC nanodot array with 100 nm spacing. (b) Selected profiles showing the range of pit depths and geometries.
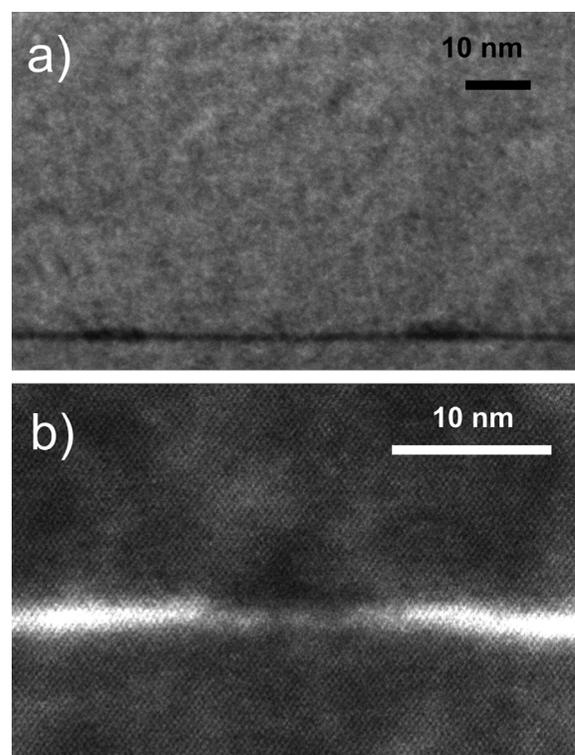

FIG. 4. HR-TEM of SiC nanodots formed using 1 pAs electron dose per site, encapsulated in Si using a two-step procedure. Panel (a) shows a bright-field image of two dots while (b) shows a HR-HAADF STEM image of an individual SiC QD.
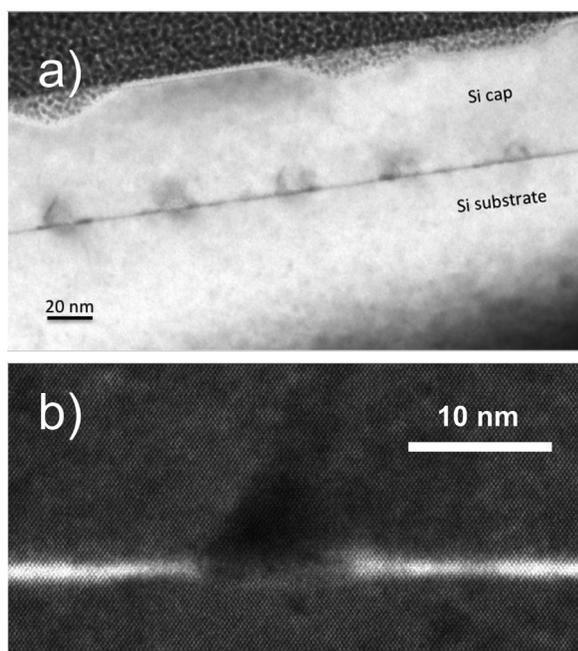
FIG. 5. HR-TEM of SiC nanodots formed using 3 pAs electron dose per site, encapsulated in Si using a two-step procedure. Panel (a) shows a bright-field image while (b) shows a HR-HAADF image of an individual SiC QD.

overgrowth ensures carbide encapsulation, which, when followed by elevated-temperature deposition, allows recovery of a fully epitaxial growth front. Additional annealing affects during the latter high-temperature capping step also aids in defect reduction and confines dislocations to the Si/SiC/Si heterointerfaces. This approach appears very promising for epitaxial incorporation of nanoscale SiC quantum dots in Si with minimal defectivity.

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