Formation of strain-induced quantum dots in gated semiconductor nanostructures

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A long-standing mystery in the field of semiconductor quantum dots (QDs) is: Why are there so many unintentional dots (also known as disorder dots) which are neither expected nor controllable. It is typically assumed that these unintentional dots are due to charged defects, however the frequency and predictability of the location of the unintentional QDs suggests there might be additional mechanisms causing the unintentional QDs besides charged defects. We show that the typical strains in a semiconductor nanostructure from metal gates are large enough to create strain-induced quantum dots. We simulate a commonly used QD device architecture, metal gates on bulk silicon, and show the formation of strain-induced QDs. The strain-induced QD can be eliminated by replacing the metal gates with poly-silicon gates. Thus strain can be as important as electrostatics to QD device operation operation. [http://dx.doi.org/10.1063/1.4928320]

Electrical transport through QDs, which are nanometer-scale regions confined in all three dimensions, are enabling exciting physics. A lot of work is being done to make silicon QDs to build an electron-spin based quantum computer,[1,2] because the spin of an electron in a silicon QD has a long coherence time.[3,4] Silicon QDs are also being pursued for electrical standards because charge pumps built from silicon QDs are more stable as a function of time than metallic charge pumps.[5,6] To pursue these applications, many different methods are used to create silicon QDs.[2] In this letter we will focus on one common method of creating silicon QDs: metallic gates on bulk silicon. In this method voltages are applied to a patterned set of metallic gates to form tunnel barriers and QDs in the silicon below.[4,7–11] This method of creating QDs is attractive because the QDs are tunable and the device architecture is similar to modern silicon transistors.

However, a major problem for this method (and, in fact, several other methods) of creating QDs is that it is common to observe many-electron QDs in situations where the device has been designed, and control voltages are set, to generate only one tunnel barrier.[7–9,12] In particular, one striking observation is that these QDs are routinely detected in the same location in different devices. Previously, these QDs have been attributed to charged defects such as dopants and interface traps;[7–9] however, the observation of consistent location is inconsistent with QDs caused by randomly located charge traps. Although steps have been taken to reduce the interface trap and dopant density, this has not eliminated these QDs. We can explain why many-electron QDs are observed in the same location in different devices by considering strain from the metal gates. This is not to suggest that charged defects such as dopants or interface traps cannot cause unintentional QDs, but for unintentional QDs that are in reproducible locations a systematic cause, such as strain, might be a more likely explanation.

Because elastic strain changes the band structure of a crystal, it is deliberately used in many silicon nanostructures.[13] For example, a silicon superlattice can be made with periodic strains rather

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than a heterostructure;[14] this has the advantage of avoiding materials interfaces. Another example is in phosphorus donors in silicon, which are being studied as qubits.[3,15] Strain changes the hyperfine coupling,[16] so local strains can be used to address individual qubits.[17] As a final example, strain increases the mobility of electrons in silicon,[18,19] which has led to strain engineering in the channel of modern silicon transistors. Each of these three examples uses intentional strains to alter the band structure of silicon to enable or improve a silicon nanostructure. In this paper we will consider the unintentional effects of strain arising from metal gates and contacts in a semiconductor nanostructure when operating a device at low temperatures. Specifically, we will show that the strain-altered conduction band (CB) can explain previously observed but unexplained quantum dots (QDs). This means that the effect on the CB from the strain from a gate or contact can be as important as the electrostatic effect of the gate or contact.

In this letter, we will show that metal gates, which are routinely used to electrostatically create QDs in silicon nanostructures, will also create strains large enough to induce a QD. First, we will go through a general argument that suggests that the typical strain from putting metals on a semiconductor nanostructure can be large enough to create strain-induced QDs. This general argument applies to many different materials systems and architectures. Then, we will simulate a device with metal gates on bulk silicon to show that the strains can induce a QD. The location of the strain-induced QD can explain why QDs are frequently observed where there should be only an electrostatic tunnel barrier. The strain-induced QD should either be harnessed or elminated. We will discuss the potential advantages of strain-induced QDs. Then we will show how the strain-induced QD can be eliminated by replacing the metal with highly-doped poly-silicon. To demonstrate that strain-induced QDs can be a problem for many different architectures, we consider another device architecture in Appendix A 4: silicon nanowires with metal contacts.

A lot of work has been done previously in optical strain-induced QDs in III-Vs by placing small stressors on top of a quantum well.[20,21] Strain from oxidizing a mesa-etched nanowire has been shown to cause tunnel barriers,[22,23] at the ends of the nanowire. Strain from lattice mismatch is needed to explain the properties of resonant tunneling diodes in Si/SiGe nanowire heterostructures.[24] It has been suggested that strains from lattice defects can be problematic in Si/SiGe QDs.[25] In contrast, we focus on the impact of the strain from metal gates, which are routinely used without consideration of the elastic strain caused by them.

We will first go through a general argument which could apply to many different semiconductor nanostructures. This will also establish the theoretical framework used in the later simulated examples. We begin by discussing the physical origin and typical magnitude of the strain. Then, we will discuss how strain changes the energy of the CB. Finally, we will discuss when the change in the CB minimum is enough to induce QDs.

Strain is inevitable in a semiconductor QD device. The strain may arise from how the device was manufactured or from operating at cryogenic temperature. During fabrication, for example, growing a thermal oxide on a silicon nanowire will induce stress in the nanowire, because thermally grown SiO_2 must expand to incorporate the extra oxygen atoms. Most of this volume expansion occurs perpendicular to the growth plane, but some remains as compressive strain in the SiO_2.[26] Strain can also come from cooling the device to its cryogenic operating temperature. Because no silicon QD consists only of silicon, the silicon must have interfaces. Coefficient of thermal expansion (CTE) mismatch at the interface will cause strain when cooled. For example, the CTEs of aluminum and silicon are 23 x 10^{-6} K^{-1} and 2.6 x 10^{-6} K^{-1}. This mismatch can setup strains as large as 0.6 % for a 300 K change in temperature.

Figure 1 shows schematically how CTE mismatch can strain a device. In this example, metal is deposited on top of a semiconductor. Metals typically have larger CTEs than semiconductors, so the metal will contract more than the semiconductor when cooled. Far away from the semiconductor-metal interface, the metal is free to contract, but near the interface the semiconductor prevents the metal from contracting, causing tensile elastic strain in the metal. Conversely, the semiconductor side of the interface is under compressive elastic strain.

The CB minimum will change linearly with strain.[27] For electrons in the $\pm k_z$ valleys (see Appendix A 1), the change in energy of the CB minimum as a function of strain is

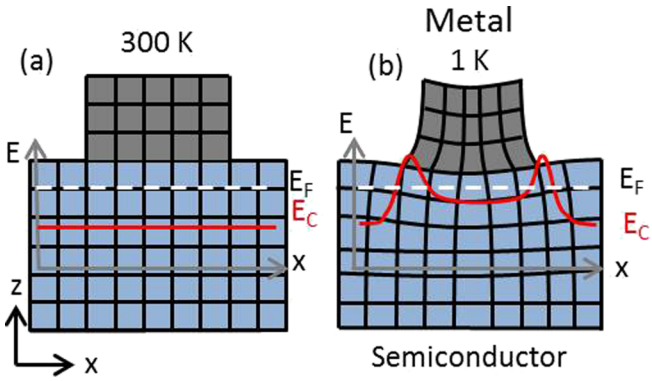

FIG. 1. Thermal contraction of metal on top of a semiconductor from (a) room temperature to (b) cryogenic temperatures. We also show a schematic of the change of the CB (E_C) in the silicon immediately below the metal, showing peaks near the corners of the metal box due to stress concentration.

$$\Delta E_C = \Xi_u \epsilon_z + \Xi_d(\epsilon_x + \epsilon_y + \epsilon_z) \tag{1}$$

where ϵ_x , ϵ_y and ϵ_z are the components of the strain, the relative change in length, and the deformation potentials are Ξ_u = 10.5 eV and Ξ_d = 1.1 eV.[27] Because $\Xi_u >> \Xi_d$, the first term dominates this equation. Thus, the energies of the $\pm k_z$ valleys will change by about 10 meV for every 0.1 % strain in ϵ_z. The change in energies of the $\pm k_x$ and $\pm k_y$ valleys can be determined by replacing ϵ_z in the first term of the right-hand-side with ϵ_x and ϵ_y. To explain the physical origin of the deformation potential, we first need to understand which atomic orbitals make up the CB. Near the valleys the CB has a significant contribution from the bonding 3d-orbitals. Because these are bonding levels, the energy of the bond decreases ($\Delta E_C < 0$) as the atoms are brought closer together ($\epsilon < 0$). Therefore, the deformation potentials of the CB are positive.

Now that we know the typical magnitude of the strain and understanding how strain modifies the CB, we will return to our simple example. Figure 1(b) shows a schematic of the effect of the strains on the CB. Strains in the semiconductor near the metal raise the CB with respect to the CB far away from the metal, where there is no elastic strain. The peaks in the CB beneath the corners of the metal are due to stress concentration at the corners of the metal. There is a local minimum of the CB between the peaks because there is less strain underneath the center of the metal.

To determine if this strain-altered CB can induce a QD, we need to consider both the shape and the magnitude of the confining potential. The shape of the CB in figure 1(b) can result in a QD, because electrons can be trapped in the local minimum (underneath the center of the metal), and the peaks (underneath the corners of the metal) form tunnel junctions. To trap an electron, the confining potential (barrier height) must be larger than kT and the charging energy (the amount of energy it takes to add an electron on the QD). At cryogenic temperatures kT is less than 0.1 meV. A typical charging energy for a QD of this size is ~ 1 meV. Therefore, 10 meV, the typical magnitude of the strain-induced change in the CB is large enough to confine electrons. In fact, a barrier height of 10 meV is the same magnitude as an electrostatic tunnel barrier[28] and the change in CB due to interface traps.[7] This example shows that, for a wide range of semiconductor nanostructures, CTE mismatch can lead to strains that have the right shape and magnitude to induce a QD. In Appendix A 2 we consider the resistance of the tunnel barriers (of order MΩ) and discuss the robustness of the barriers with respect to gate voltage changes (robust to changes of order 0.1 V).

Figure 2(a) shows a device architecture for electrons in a surface-gated bulk-silicon device. This architecture consists of a bulk silicon (lightly p-doped) wafer covered in 10 nm of thermally grown SiO_2, with two aluminum gates (upper gate, UG, and lower gate, LG) on top.[4,7–11] The two aluminum gates are perpendicular to each other and are isolated from each other by 3 nm of AlO_x. The UG is 80 nm tall and 50 nm wide, and the LG has a 25 nm diameter. A positive voltage on the UG will cause an inversion layer a few nanometers thick to form at the Si-SiO_2 interface. Current flows through the inversion layer (current flows from and to a heavily doped source and drain regions that are far from the LG). A negative voltage on LG can deplete the silicon below the

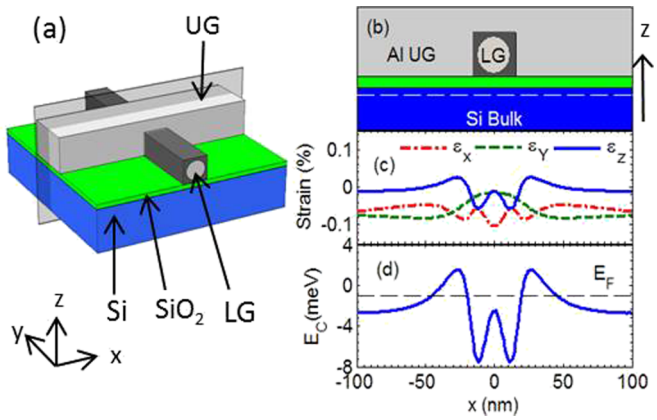

FIG. 2. Calculated strains and CB change for metal gates on bulk silicon. (a) A pseudo-3D drawing of the device showing the bulk silicon wafer (blue), SiO_2 (green), Al UG and LG (grey) and AlO_x (dark grey), not to scale. (b) Cross section of the device through the translucent plane in (a) with same colors as (a), not to scale vertically. Dashed white line represents the inversion layer (1 nm below the Si-SiO_2 interface), electrons flow in the inversion layer from left to right. (c) Calculated strains in inversion layer (white line in (b)), showing the effect of strains from CTE mismatch of Al and AlO_x. (d) CB modulation from strains in (c) showing tunnel barriers at $x = \pm 30$ and a QD between. The dashed line represents the Fermi level. (b)-(d) all have the same horizontal axis.

LG to form a single tunnel barrier, directly below the LG. However, QDs are commonly observed in this location, where there should only be a tunnel barrier.[4,7–11] In this section, we will show how strain from the CTE mismatch can induce a QD directly below the LG.

Figure 2(b) shows the simulated strains for this architecture. We use COMSOL multiphysics[29] to simulate the strains in the device (details in Appendix A 3). The simulation includes both CTE mismatch and intrinsic stress in the SiO_2 (-200 MPa[26]). The intrinsic stress of the Al and AlO_x are small at the fabrication temperature.[30] Unlike figure 1, where the CTE mismatch between metal and semiconductor caused the strain, here CTE mismatch between Al and AlO_x creates stresses that propagate into the silicon below. Al (23×10^{-6} K^{-1}) has a much larger CTE than AlO_x (5.4×10^{-6} K^{-1}). For a change in temperature from 150 C (the fabrication temperature) to 1 K, Al is in tensile stress because the AlO_x is preventing it from contracting. Conversely, the Al is putting the AlO_x in compressive stress. These stresses propagate through the SiO_2 into the silicon. CTE mismatch from the SiO_2 and intrinsic stress from the SiO_2 only results in uniform strain and so cannot induce a QD.

Confining electrons in an inversion layer breaks the six-fold valley degeneracy and only the $\pm k_z$ valleys are occupied (Appendix A 1). In Fig. 2(d) we use eq. (1) to calculate the change in energy of the $\pm k_z$ valleys due to the strains shown in Fig. 2(c). (Because the first term dominates eq. (1), ΔE_C has the same shape as ϵ_z). The peaks at $x = \pm 30$ nm form tunnel barriers for electrons. The height (4 meV) and length (40 nm) of these barriers give them tunneling resistance of 20 MΩ (Appendix A 2). A strain-induced QD forms in the dip between these barriers. This QD is directly below the LG, which can explain the previously observed QDs.[4,7–11]

We have shown that in this device architecture strain can induce a QD. Because strain is often ignored when designing the device, the strain-induced QD would show up as additional QDs. This could explain why such unintentional QDs are a common problem in surface-gated architectures.[7–9,12] Strain-induced QDs have several advantages over electrostatically defined QDs. Making electrostatic QDs requires additional metal gates, limiting the number of QDs that can be operated. Each gate also makes the QD bigger, which makes it harder to reach the few-electron limit. These advantages can be obtained in an architecture which is already being used to make electrostatic QDs, when taking into account strain effects.

If the strain-induced QD is not desirable, then it should be eliminated. In the geometry of Fig. 2, the strain-induced QD can be eliminated by replacing the Al and AlO_X in the gate stack with heavily doped poly-silicon and SiO_2. Electrostatically this device operates just like the Al gated device. This material switch, from Al (CTE 23 x 10^{-6} K^{-1}) to poly-Si (2.9 x 10^{-6} K^{-1}), reduces the CTE mismatch by an order of magnitude. The intrinsic stress in the poly-silicon is -400 MPa.[31]

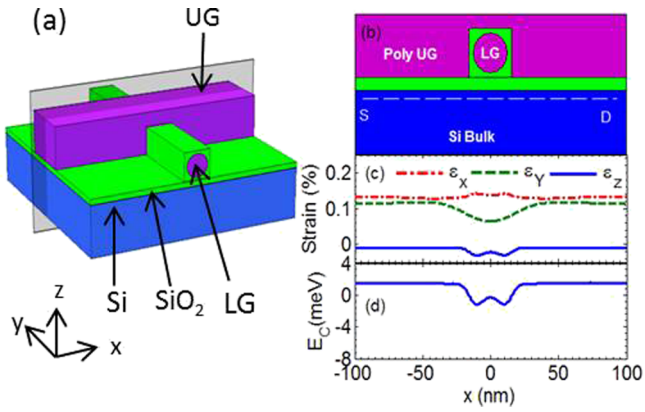

FIG. 3. Calculated strains and CB change for poly-Si gates on bulk Si. (a) A pseudo-3D image of the device showing the bulk silicon wafer (blue), SiO_2 (green), Poly-Si LG and UG (purple), not to scale. (b) Cross section of the device through the translucent plane in (a) with same colors as (a), not to scale vertically. Dashed white line represents the inversion layer. (c) Calculated strains in inversion layer (1 nm below the Si-SiO_2 interface). (d) CB modulation from strains in (c). Note that the change in the CB is much smaller than in Fig. 2(d) due to changing the gate material from aluminum to poly-silicon. (b)-(d) all have the same horizontal axis.

Figure 3 shows the strains calculated for the same geometry and dimensions as for the Al gate device. The strains due to the LG are much smaller than in the Al gated device. This results in a much smaller modulation of the CB due to strain (Fig. 3(d)). Because the peaks that had been the tunnel junctions in the Al gated device are now only 0.1 meV high, this device will not form a strain-induced QD.

We have shown that strain from CTE mismatch can cause QDs. Although we only showed one example geometry, our argument is more general. Most metals have a larger CTE than insulators or semiconductors. Thus our qualitative argument that the typical strains in a nanostructure at low temperatures are large enough to create strain-induced QDs, applies to other material systems such as carbon, germanium and III-Vs. To demonstrate this, in Appendix A 4 we consider another example, a silicon nanowire with metal contacts. Because the typical strains in a nanostructure can induce QDs, we suggest that the strains should either be used or ameliorated. Reducing the strain (perhaps by replacing metal gates with poly-Si gates) would eliminate the strain-induced QDs, allowing an electrostatically gated device to operate as intended. In addition to avoiding unintentional effects due to strain, we can also see some advantages to strain-induced QDs compared to other methods of creating QDs. Strain-induced QDs require fewer gates, allowing them to be smaller than electrostatic QDs.

Because strain can be as important as electrostatics to the operation of a QD device, the effects of strain should be considered when analyzing the results from or designing semiconductor nanostructures.

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APPENDIX

1. Silicon band structure

The bottom of the conduction band (CB) and top of the valence band (VB) are shown schematically in figure 4. In bulk silicon the bottom of the CB is 6-fold degenerate, while the top of the VB is 4-fold degenerate. However, these degeneracies can be broken by confinement and strain.[32,33]

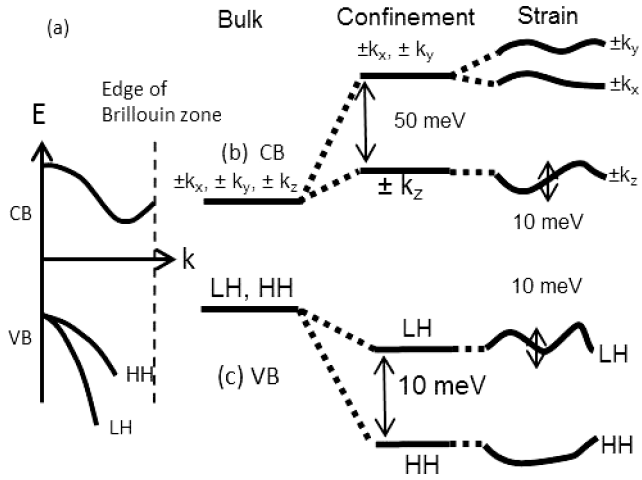

FIG. 4. Diagram of the band structure of silicon. (a) The CB has 6 equivalent valleys, and the VB has LH and HH states. (b) The 6-fold degeneracy of the CB is split by confinement, the energies of the lowest two valley states are further modulated by strain. (c) Similar diagram for VB.

The six valleys in the CB are located at $\vec{k} = (2\pi/a_0)(\pm 0.85, 0, 0), (2\pi/a_0)(0, \pm 0.85, 0)$, and $(2\pi/a_0)(0, 0, \pm 0.85)$, where a_0 is the silicon lattice constant ($a_0 = 0.543$ nm). Around each valley the effective mass is anisotropic. For the $\pm k_z$ valleys, centered at $k_0 = (2\pi/a_0)(0, 0, \pm 0.85)$, the effective mass in the z-direction is $m_l = 0.98\, m_e$, while the effective mass in the x and y directions is $m_t = 0.19 m_e$, where m_e is the free electron mass. Thus the dispersion relation for the $\pm k_z$ valleys is

$$\Delta E_C(\vec{k}) = \frac{\hbar^2}{2}\left(\frac{k_x^2}{m_t} + \frac{k_y^2}{m_t} + \frac{(k_z - k_0)^2}{m_l}\right) \tag{A1}$$

The dispersion relations for the $\pm k_x$ and $\pm k_y$ valleys are similar.

To show how confinement breaks the six-fold valley degeneracy [Fig. 4(b)], consider an inversion layer perpendicular to the z-axis. We can neglect lateral confinement because of the much larger length scale. The potential well confining the electrons can be approximated by an infinite triangular well.[33] In the effective mass approximation, the eigenenergies for the electron are given by

$$E_n = \left(\frac{(e\mathcal{E})^2\hbar^2}{2m_z}\right)^{\frac{1}{3}}(-a_n) \tag{A2}$$

where $e\mathcal{E}$ is the slope of the quantum well ($\mathcal{E}$ is the electric field confining the electron), and a_n are the zeroes of the Airy function ($a_0 \approx$ -2.33). For the $\pm k_z$ valleys, $m_z = m_l$, while the other four valleys $(\pm x, \pm y)$ $m_z = m_t$. Therefore, the $\pm k_z$ valleys have a lower energy ($E_0 = 37$ meV for $\mathcal{E} = 105$ V/cm) than the $\pm k_x$ and $\pm k_y$ valleys ($E_0 = 63$ meV). Because this energy difference is many kT at cryogenic temperatures (for $T = 1$ K, $kT = 86\ \mu$eV), the $\pm k_x$ and $\pm k_y$ valleys will not be occupied.

Strain also changes the energies of the valleys [Fig. 4(b)]. This is due to the atomic lattice being squeezed or pulled by the strain, thus raising or lowering each band within the silicon. The change in energy of the $\pm k_z$ valleys is described by the deformation potentials $\Xi_u = 10.5$ eV and $\Xi_d = 1.1$ eV.

$$\Delta E_C = \Xi_u \epsilon_z + \Xi_d(\epsilon_x + \epsilon_y + \epsilon_z) \tag{A3}$$

The deformation potential, Ξ_u, for the CB in silicon is positive because there is a large contribution to the CB from the atomic 3-d bonding orbitals. We already showed that in an inversion layer electrons will only occupy the $\pm k_z$ valleys, so we will not further consider the $\pm k_x$ and $\pm k_y$ valleys. The local strains, set up by CTE mismatch, are typically of order 0.1 %. Combined with the deformation potentials, these strains will change the energy of the valley by $\approx$ 10 meV. Because the CB is defined with respect to electron energy, a peak in the CB due to strain will cause a tunnel barrier for electrons.

The VB of silicon consists of a light hole (LH), heavy hole (HH), and spin orbit split off (SO) bands[1]. The SO band is 44 meV lower than the LH and HH bands. Because this splitting is many kT at cryogenic temperatures, holes will not occupy the SO band, and it will not be considered further.

The dispersion relations for holes in the LH and HH are

$$\Delta E_V = -Ak^2 \mp (Bk^4 + C(k_x^2 k_y^2 + k_y^2 k_z^2 + k_z^2 k_x^2)) \tag{A4}$$

where the – is for the HH and the + for the LH and $A = -4.25(\hbar^2/2m_e), B = -0.63(\hbar^2/2m_e)$ and $C = 4.9(\hbar^2/2m_e)$.[32] We note that $\Delta E_V \approx (3/2)a_v(\epsilon_y + \epsilon_z)$ for the LH. The a_v term is positive in silicon because the VB consists of the atomic 3p-bonding orbitals.[32] Confinement will split the LH and the HH [Fig. 4(c)]. However, because the VB dispersion relation is more complicated than CB dispersion relation, showing the effect of confinement is more complicated for the VB than for the CB. Restricting ourselves to the case of confinement in a nanowire, recent theoretical work[34] has shown the highest VB state is predominately LH in character with the spin aligned with the axis of the nanowire. Therefore, we assume that we only need to consider the LH in our analysis.

Strain will further change the energy of the VB [Fig. 4(c)]. Ignoring the effect of band mixing due to strain, the change in the VB of silicon due to strain is

$$\Delta E_V = a_v(\epsilon_x + \epsilon_y \epsilon_z) + b_v(\epsilon_x - (\epsilon_y + \epsilon_z)/2) \tag{A5}$$

where a_v = 2.1 eV and b_v = -2.33 eV for silicon.[32] Because the VB is defined with respect to electron energy, a dip in the VB due to strain will cause a barrier for holes.

2. Barrier resistance

To observe a QD the barrier resistance, R, must be larger than the resistance quantum ($R \gg R_K = 26k\Omega$) to observe discrete charging events on the QD.[35] But the resistance must not be so large as to make the current too small to measure, $R < 1G\Omega$. In the main text we determined that the typical modulation of the CB due to strain is of order 10 meV. To calculate the tunneling resistance, we will need the length scale over which the CB changes. 10 nm is a typical gate width or oxide thickness. (The gate width is typically limited by electron beam lithography to greater than 10 nm, and oxide thicknesses are typically of order 10 nm to prevent leakage.) Using a WKB (Wentzel – Kramers – Brillouin) tunneling rate for a parabolic barrier to determine the tunneling resistance,

$$\frac{1}{R} = G = N\frac{e^2}{\hbar} e^{-\frac{\pi}{\sqrt{2}}\frac{\sqrt{m^*}}{\hbar}\sqrt{\phi}L} \tag{A6}$$

where $m^* = 0.19m_0$ and taking the number of channels, N = 1 (because $N \approx w k_f \approx 1$[37]). In the main text we show that the calculated barrier length 40 nm corresponds to 20 MΩ. Given the barrier height we calculated in the main text (4 meV) the barrier could be as short as 10 nm (so $R > R_K$ and discrete tunneling events can be observed) or as long as 60 nm (so $R < 1G\Omega$, and we can still measure current).

3. Simulation Details

The strain was simulated using COMSOL multiphysics. A few simplifying assumptions were made in the simulation: the silicon was simulated isotropically and room temperature materials properties were used, including Young's modulus, Poisson's ratio, density and CTE. The materials properties used in the simulation are shown in Tab. I. We were unable to include the temperature dependence of the CTE because we were unable to locate a complete set of CTE over the entire thermal range for all the materials in the simulation. Thermal contraction is considered from the fabrication temperature (which for the Al and AlOx is 150 C) down to the cryogenic measurement temperatures of 1 K. Because the the simulation were considered from the elevated fabrication temperature (where the CTE is larger than at room temperature) to cryogenic temperature (where the CTE is smaller than room temperature) we think that the room temperature

TABLE I. Materials parameters used in the simulations.

Material	Young's Modulus (GPa)	Poisson's Ratio	Density (kg/m^3)	CTE (x10^{-6}/K)
Si	130	0.27	2300	2.6
SiO_2	73	0.17	2200	0.49
Al	70	0.35	2700	23
AlO_x	300	0.22	3900	5.4
Ni	220	0.31	8900	13
Poly-Si	170	0.22	2300	2.9

values are a reasonable value for the CTE. For example, aluminum which from +150 C to -191 C the total thermal contraction is $\Delta l/l_0 = -70 \times 10^{-4}$.[36] Because the 1 K measurement temperature is below -191 C, this $\Delta l/l_0$ is an underestimate. But it is not a big underestimate, because the CTE drops rapidly below -191 C. Using the room temperature value of CTE we instead calculate $\Delta l/l_0 = \alpha_{Al}\Delta T = -102 \times 10^{-4}$. Thus we think that the room temperature values for CTE are reasonable given that a complete set of temperature dependent CTEs were unavailable for all of the materials needed over the entire temperature range needed.

All simulations were performed in three dimensions. The simulated volume was about 5x10^7 nm^3. Despite the nanoscale features atomistic simulations are not necessary; similar simulations of the stress are performed in similarly scaled commercial transistors.[18] A zero displacement boundary condition was used for the bottom surface of the simulated volume, and a zero force boundary condition was used everywhere else on the surface. We verified that the boundary conditions do not affect the area of the simulation of interest by changing the size of the simulation, and observing that the strains in the area of interest were not affected. Similarly, we verified that refining the mesh did not alter the simulation results. We did not consider the possibility of delamination. Physically, the simulation corresponds to cooling the device adiabatically.

4. Silicon Nanowire with Metal Contacts

VB holes can be confined in a chemically-grown nanowire between metallic contacts.[38–41] Chemically-grown nanowires are attractive because it is easy to grow a small diameter nanowire with low surface roughness.[38] Tunnel barriers near the nanowire-contact interface confine the holes within the nanowire. These tunnel barriers are essential to form the QDs, and so understanding the reason for their existence is important. Sometimes these barriers are due to Schottky barriers; however, the metal-semiconductor pair is often deliberately chosen to prevent a Schottky barrier. For example, in bulk metal-InAs contacts the Fermi level is pinned above the CB,[42,43] and thus a Schottky barrier should not form. Also, many other metal-semiconductor combinations, which form Schottky barriers in bulk, should not form Schottky barriers in a nanostructure, because there are not enough interface states on a nanowire to pin the Fermi level.[44,45] Nevertheless, it is common to observe tunnel barriers in metal-nanowire contacts that should not have Schottky barriers.[46] This mystery has driven us to consider strain-induced tunnel barriers as an explanation.

Figure 5(a) shows a device architecture for a chemically grown nanowire that is frequently used to form QDs for holes.[38–41] A typical device (Fig. 5(a)) consists of an undoped Si nanowire (5 nm radius) on top of a thick SiO_2 layer. Contacts for the source and drain are formed with Nickel (50 nm thick separated by 200 nm). We assume that no Schottky barrier forms at the metal-nanowire interface, so holes can flow freely from the Ni into the nanowire. In this section, we will show that strain can cause tunnel barriers for holes in the nanowire near the metal contacts.

Most of the strain in this device comes from the CTE mismatch of nickel (13x10^{-6} K^{-1}) and silicon (2.6x10^{-6} K^{-1}). Figure 5(c) shows the strains in the center of the nanowire as simulated for a change in temperature of 293 K to 1 K. Strains elsewhere in the nanowire are similar. Because the metal contacts shrink, this pulls on the nanowire. Therefore, the nanowire is stretched (in tension) in the x direction (and has compressive strains in ϵ_x and ϵ_y because of Poisson's ratio).

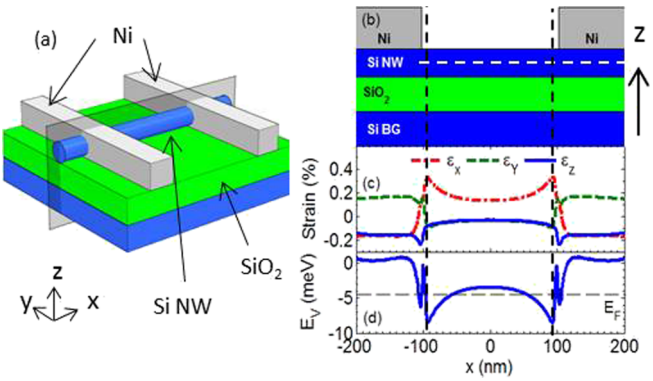

FIG. 5. Calculated strains and VB change for a chemically grown silicon nanowire with nickel contacts. (a) A pseudo-3D drawing of the device showing the bulk Si wafer (blue), SiO_2 (green), Si-nanowire (blue), Ni source and drain contacts (grey). (b) Cross section of the device through the translucent plane in (a) with same colors as (a), not to scale vertically. (c) Calculated strains at center of the nanowire (white dashed line in (b)), showing the effect of strains CTE mismatch of Si-nanowire and Ni contact. (d) VB modulation for LH from strains in (c) showing tunnel barriers at $x = \pm$ 100 and a QD in between. Horizontal dashed line represents the Fermi level. (b)-(d) all have the same horizontal axis. Black vertical dashed line shows the location of the tunnel junctions in (b) to (d).

The VB of bulk silicon consists of degenerate HH and LH bands. Confinement in a nanowire will split the LH and HH bands, and the topmost VB state has been predicted to be predominantly LH in character, with the spin quantized along the direction of the nanowire.[34] We take the simulated strains and use eq. (A5) to calculate the change in the VB for LHs [Fig. 5(d)]. As mentioned below eq. (A5) the change in the VB is due primarily to the sum of the strains, $\epsilon_y + \epsilon_z$. Dips in the VB, like those at $x = \pm$ 90 nm in Fig. 5(c), which are between the edges of the metal contacts, create barriers for holes. Between the barriers, a strain-induced QD forms in the peak in the VB centered at $x = 0$. The tunnel barriers have a height of 5 meV and a length of 30 nm which gives an estimated tunneling resistance of 45 MΩ). This resistance is large enough to quantize the charge on the QD without shutting current off. So we have shown that strain can induce a QD in a nanowire between two metal contacts. We propose this as an explanation of why tunnel barriers are sometimes observed at metal-nanowire interfaces that should not form Schottky barriers.[46]

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