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Charge offset stability in Si single electron devices with Al gates

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Abstract

We report on the charge offset drift (time stability) in Si single electron devices (SEDs) defined with aluminum (Al) gates. The size of the charge offset drift (0.15 *e*) is intermediate between that of Al/AlO_x/Al tunnel junctions (greater than 1 *e*) and Si SEDs defined with Si gates (0.01 *e*). This range of values suggests that defects in the AlO_x are the main cause of the charge offset drift instability.

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Keywords: quantum information, Coulomb blockade, charge offset drift

(Some figures may appear in colour only in the online journal)

Single-electron devices (SEDs) have been proposed for a variety of applications, including electrical metrology (standards of current and charge) [1], ultra-sensitive sensors including charge electrometers [2], and as solid-state qubits [3]. Si-based SEDs are one of the leading candidates for these applications, in part because of their general attractive attributes including tunability [4], compatibility with present-day integrated circuits, and because of their stability (lack of charge offset drift) [5]. Referring specifically to their potential as spin qubits: The weak spin–orbit coupling and low density of nuclear spins in naturally occurring silicon means that it is ideally suited as a host for spin qubits [6], with recent demonstrations of electron spin qubits [7, 8] and a high-fidelity nuclear spin qubit [9]. Furthermore, the coherence time in bulk Si can be made very long when the nuclear spin bath is effectively removed through the use of isotopically-enriched ^{28}Si [10, 11].

One of the important attributes for all of the applications mentioned above is the time stability of the SEDs. This is a particular issue because the inherent sensitivity to the motion of a single electron has both attractive and deleterious implications: it is attractive because SEDs provide the world's most sensitive charge electrometers; it is deleterious because their gross behavior can be markedly changed by small subtle movements of nearby charges. These devices are fabricated with thin-film lithography and processing on the surfaces of substrates; thus, as opposed to bulk single-crystal Si, in these devices there are numerous nearby defects which can possess a net charge or dipole moment. In turn, these charges can modulate the electrostatic potential of the SED island, and thus lead to a random time instability. This manifests itself as a time-dependent random phase offset ϕ [5] to the periodic control curve (e.g., the inset to figure 2), quantified as $Q_0(t) = (\phi/2\pi)\, e$, where e is the electron charge.

In addition to the effect on the prospects for integration, the potential application of SEDs as qubits gives additional impetus to the importance of assessing the time stability. It is generally believed that electron quantum coherence is more 'fragile', i.e., more prone to loss of information, than classical storage, in part due to the effect of nearby defects that can

[4] ftp://ftp.nist.gov/pub/physics/neilz/papers.html (TEL: +1-301-975-5887)

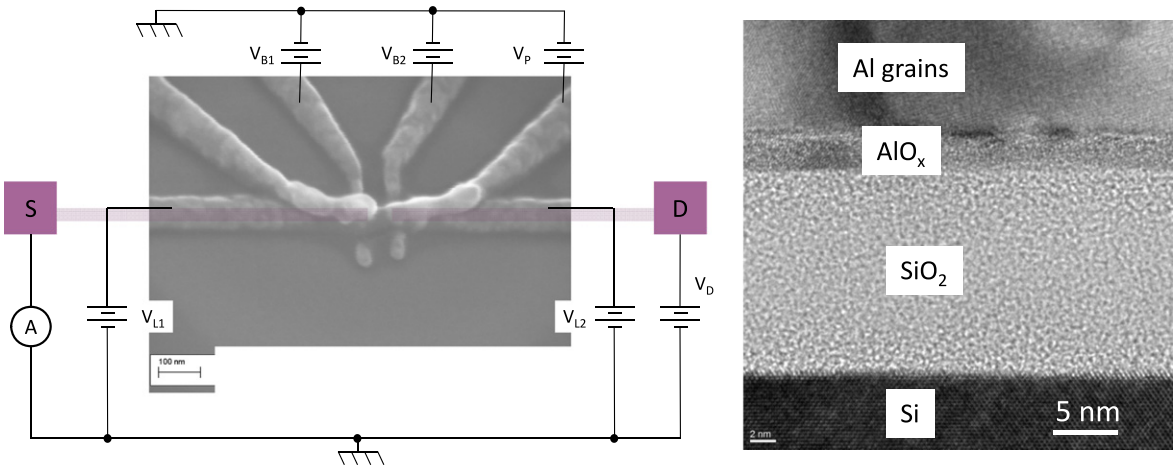


Figure 1. (a) Scanning electron micrograph of Al gate electrodes on Si/SiO_2 substrate (30° tilt) and schematic measurement circuit. The solid pink (gray on paper) squares labelled 'S' and 'D' indicate the heavily-doped n^+ source and drain regions, and the transparent pink rectangle schematically indicates the conducting accumulation layer (generated by V_{L1} and V_{L2}) in the Si at the Si/SiO_2 interface. (b) Cross-sectional transmission electron micrograph taken in the middle of the device in figure 1(a), showing both (i) the general thin-film stack and specifically (ii) the thin AlO_x layer underneath the aluminum gate.

have random fluctuations of their charge or spin. Thus, similar to studies of properties such as electron mobility [12], elucidation of the charge offset drift $Q_0(t)$ can give us additional information as to the suitability of particular materials or device architectures with regard to optimizing fidelity and coherence in qubit devices.

In previous work ([5] and references therein), we have shown that there is a marked difference between $Q_0(t)$ in metal devices (based on Al/AlO_x/Al tunnel junctions) and Si-based devices containing only crystalline and polycrystalline Si and SiO_2: the typical amplitude of $Q_0(t)$ is about 0.01 e in the Si-based devices and greater than 1 e in the metal devices. Recently, Si-based devices with Al gates have been shown to have excellent behavior in a variety of applications [13] including spin qubit coherence [8]. The natural question thus arises, in the context of previous work on $Q_0(t)$: Does the presence of Al gates affect the charge offset drift in Si devices? We aim to answer that question in this paper.

Our fabrication (figure 1(a) and sketch in table left column) followed closely previous work [14, 15]. Starting from a high-resistivity (10 kΩ-cm n-type) Si substrate, we generated by diffusion highly doped n^+ source (S) and drain (D) Ohmic contacts, and then grew a thermal gate oxide (18 nm of SiO_2) at 800 °C in O_2 and dichloroethylene. We then fabricated a three-layer gate stack: (i) Al barrier gates B1 and B2 plus a AlO_x isolation oxide, (ii) Al lead gates L1 and L2 and another AlO_x isolation oxide, and then finally (iii) the Al plunger gate P. Lead gates L1 and L2 terminate slightly inside B1 and B2; P fills the length between B1 and B2. Thus, in various locations (see figure 1(a)), the stack can have one (e.g., far away from center), two (e.g., where P lies over L1 to left of B1) or three (e.g., on top of B1) Al layers.

The gates were all formed by electron beam lithography and lift-off patterning of thermally-evaporated aluminum. The isolation oxides were formed in air at 150 °C, resulting in about 4 nm of AlO_x. Finally, we annealed in forming gas (15 min, 400 °C, 5% H_2), followed by cleaving and wire bonding for electrical contact. Figure 1(b) is a cross-sectional TEM micrograph of the finished device directly underneath gate P (Al metal), showing among other details the undeliberate formation of a thin interfacial layer of AlO_x between the SiO_2 and the Al gate.

As depicted in the schematic circuit in figure 1(a), we applied a small drain voltage to Ohmic contact D, measured the current flowing through Ohmic contact S, used V_{L1} and V_{L2} to induce a conducting accumulation layer between S and D at the Si/SiO_2 interface, and generated tunneling barriers by applying mildly negative (with respect to the threshold voltage) voltages V_{B1} and V_{B2}. The combination of these produced a quantum dot at the center of the device, whose chemical potential we controlled with V_P. We applied voltages and measured the current using commercial voltage sources and current amplifiers. All the measurements presented in this paper were performed at 2.2 K in vacuum in a cryocooled measurement system.

The inset to figure 2 shows the standard Coulomb blockade oscillation (CBO); the peak spacing is constant over a fairly large number of oscillations, and shows an overall mild monotonic increase in current as increasing V_P lowers the height of the tunnel barriers, and thereby increases the current. In order to measure the time stability $Q_0(t)$, we repeatedly make measurements of the CBO, and for each measurement fit [5]

$$I_D(V_P) = A_0 + A \sin\left[2\pi\left(V_P/\Delta V_P + Q_0(t)\right)\right] + BV_P.$$

Here, A_0 is a current offset, $A \approx 0.1$ nA, $\Delta V_P \approx 22$ mV is the period, and $B \approx 0.4$ pA/mV accounts for the mild linear slope as seen in figure 2 inset.

The uncertainty in the measurement, arising from the uncertainty of the fit, is about ± 0.01 e; the sample-dependent fluctuation in $Q_0(t)$ occurs on time scales of about 0.1 day and greater, and yields a total range in $Q_0(t)$ of about ± 0.15 e. We measured identical behavior for two different nominally identical devices using two different sets of measurement

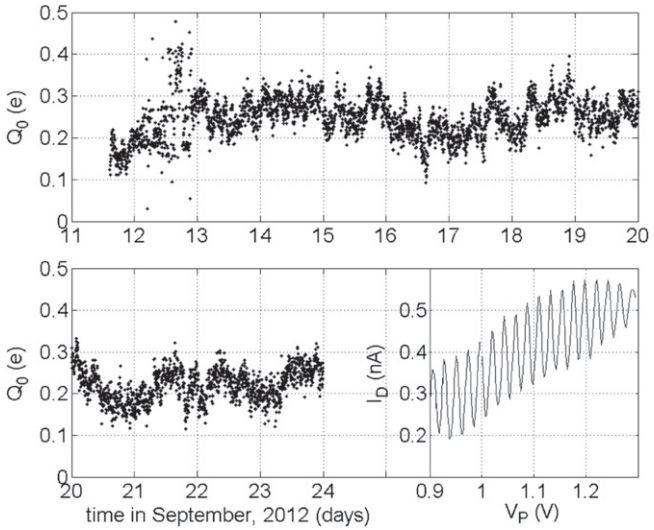


Figure 2. Inset: Coulomb blockade oscillations in the SET. The individual oscillations correspond to adding one additional electron at a time to the quantum dot, and the overall monotonic increase in the drain current reflects the smooth reduction of the tunnel barriers due to the increase in V_P. Main: charge offset drift $Q_0(t)$ as a function of running time, showing a range of about ± 0.15 e overall, during the course of this 13 day measurement. Each individual data point was obtained by fitting a sinusoidal function with a linear offset to the data as exemplified in the inset, for V_P between 1.1 and 1.2 V. $V_D = 0.5$ mV, $V_{L1} = V_{L2} = 1.4$ V, $V_{B1} = 0.296$ V, $V_{B2} = 0.34$ V, $T = 2.2$ K.

electronics and ramp protocols, and also verified the accuracy of the measurement by demonstrating a much smaller drift of about $\pm 0.01\,e$ in a Si/poly-Si device [16] with the same measurement system and temperature.

To put this in context, in earlier work we noted that the typical amplitude [5] of $Q_0(t)$ in metal SEDs (based on Al/AlO_x/Al tunnel junctions) is greater than 1 e, and in Si-based devices containing only crystalline and polycrystalline Si and SiO_2 the amplitude is about 0.01 e. In this earlier work, we demonstrated that the reason for this difference in the behavior of $Q_0(t)$ was due to the instability of the AlO_x as opposed to the SiO_2. In particular, the time-dependent fluctuators which give rise to $Q_0(t)$ exist in both insulators, but interactions between the fluctuators in the AlO_x also give rise to a glassy relaxation and thus to the time instability in $Q_0(t)$. In order to make sense of the present results, we focus on oxide similarities and differences between the CMOS-compatible[5] SEDs and the devices studied in this paper (see table 1).

From the table we note the following correlations between amplitude of $Q_0(t)$ and device characteristics:

Presence of AlO_x (AlO_x thickness) As discussed above.

Total thickness of oxide t Based on two data points (Si/SiO_2/Al gates versus Al/AlO_x/Al), it appears that smaller total oxide thickness is correlated with a larger amplitude of $Q_0(t)$. This is consistent with a simple estimate for the change in charge displacement on the quantum dot as a function of oxide thickness (see below).

Electric field strength in AlO_x (AlO_x E) The fact that the electric field strength is smaller for the largest amplitude of $Q_0(t)$ indicates that the applied voltage is not inducing the drift, and might in fact be inhibiting it. This is consistent with a previous observation of instability as a function of gate voltage in our devices [17].

Current through AlO_x (AlO_x I_D) The devices with the largest amplitude of $Q_0(t)$ are the only ones in which AlO_x exists in the tunnel barriers, and therefore in which the AlO_x current $I_D \neq 0$. This suggests that, among other things, electromigration might be a contributing factor to the charge offset drift (see below).

In addition to the previous discussion of the instability of AlO_x, we also note a previous suggestion [18] that large charge offset fluctuations in a Al/AlO_x/Al SED were due to isolated Al grains. These grains were generated during deposition from thermal evaporation, and were identified by scanning electron micrographs. The hypothesis is that such grains act as sources/sinks of charge which randomly fill and empty on a variety of time scales, depending on the tunneling resistance between the isolated grains.

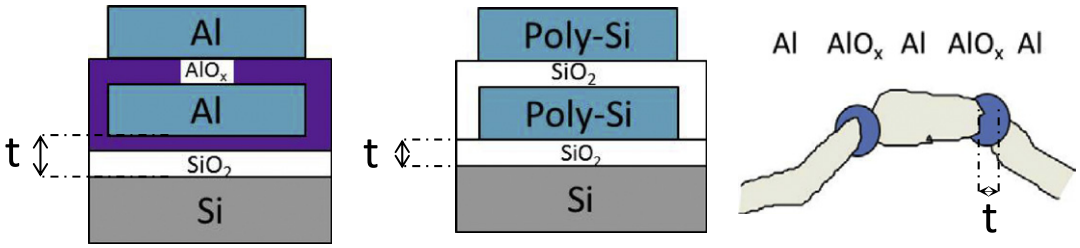
Electromigration [19] is a well-known driving source of atomic motion in microscale (e.g., integrated circuit metallization) and nanoscale (e.g., single atom junctions) conductors. It is generally believed to arise from both electric field-induced motion of the massive ions and from momentum transfer from hot electrons. It has been previously observed [20] that a particularly high level of charge offset drift in a Al/AlO_x/Al SED appeared to be driven by current through the junction. On the other hand, a compendium [5] of $Q_0(t)$ results in Al/AlO_x/Al SETs showed no correlation between I_D and amplitude of $Q_0(t)$. Thus, it appears plausible that in some cases the charge offset drift in Al/AlO_x/Al is due to electromigration, but certainly not in all cases.

A simple estimate [21] for the change in charge displacement ΔQ_0 can be derived as follows: For a bare charge of magnitude e moving a perpendicular distance d in a parallel plate capacitor with insulator thickness t, $\Delta Q_0 \approx d/t\ e$; for typical values ($d$ an interatomic distance, t a few nm), this leads to $\Delta Q_0 \approx 0.1\ e$. If we consider a charge dipole with change in perpendicular dipole length Δl, we obtain $\Delta Q_0 \approx \Delta l/t\ e$, which will yield a somewhat smaller but similar magnitude. These estimates (valid for both gate and barrier insulators) also indicate that the charge offset drift amplitude should scale inversely with insulator thickness.

In contrasting the influence of electric field versus oxide thickness, we can point out that in previous work [22] in which the authors measured and modelled the noise as a function of local position, the devices studied had AlO_x only in the tunnel junctions, and not between the gate and island. For this reason, considering various insulators surrounding the dot, the electric field strength $E \propto 1/t$ and thus was correlated with insulator thickness. In our case, the addition of a vertically-located gate allowed us to discriminate between the effects of applied voltage and insulator thickness.

[5] We use CMOS-compatible as shorthand to mean both: i) only Si and thermally-grown SiO_2 near the device (specifically avoiding metals and metal oxides), and ii) a fabrication process flow that incorporates many of the standard cleanliness protocols. [16].

Table 1. Comparison of important attributes relevant to charge offset drift $Q_0(t)$ for three different classes of devices. In the sketches, 't' represents the total gate or barrier oxide thickness; leftmost sketch represents a region where there are two Al layers above the wafer (e.g., where P and L1 overlap but not B1). For the Si/Al gate devices, total t and electric field strength E refer to the SiO_2/AlO_x between gate P and dot.



	Si/SiO_2/Al gates/AlO_x	Si/SiO_2/poly-Si gates	Al/AlO_x/Al
	Present work	JAP 104, 033710 (2008)	JAP 104, 033710 (2008)
Q_0 (t) amplitude (e)	± 0.15	± 0.01	± 1
thin-film stack	$Si/SiO_2/AlO_x/Al/AlO_x/Al$	Si/SiO_2/poly-Si/SiO_2/poly-Si	$Al/AlO_x/Al$ tunnel junction
AlO_x thickness (nm)	4	None	2
Total gate or barrier oxide t (nm)	20	20 – 40	2
AlO_x E (V/cm)	10^6	None	10^5
AlO_x I_D (nA)	None	None	1

We thus reach the following conclusions from our present work:

(1) Al gates on top of SiO_2 result in a thin interfacial layer of AlO_x [13] (see figure 1(b)), important because it is the only AlO_x which is not electrostatically screened by Al gates.
(2) The amplitude of $Q_0(t)$ in devices containing AlO_x and SiO_2 is larger than devices containing only SiO_2. This is because of either: (i) inherent glassiness of atomic/molecular motion in the AlO_x, or (ii) separated Al grains at the edges of the gates.
(3) The fact that $Q_0(t)$ is smaller for Si/SiO_2/Al devices (t = 20 nm) than for Al/AlO_x/Al) devices (t = 2 nm) is consistent with a very simple model that predicts the dependence of $Q_0(t)$ amplitude upon distance; this suggests that moving AlO_x layers further away from device layers may be very helpful in reducing $Q_0(t)$.

Finally, we can comment on the consequences of our work for future devices. One important goal of single electron metrology [1] is that of a single electron current standard with large value, where one approach is to parallelize a large number of devices. In such parallelized devices, the absence of charge offset drift would be evidently important. For quantum information, a significant candidate for solid-state qubits is spins in Si [6]. Silicon SEDs with the same materials and device architecture as those studied here have recently been used to read out the state of an electron spin qubit bound to a nearby phosphorus (^{31}P) donor [23]. Such SED-donor coupled systems have been used in demonstrations of coherent control of both electron spin [8] and nuclear spin [9] qubits. In the case of the electron spin and the ionized ^{31}P nuclear spin the coherence times appear to be determined by the dynamics of the ^{29}Si nuclear spin bath present in natural Si. For the neutral ^{31}P nuclear spin, however, the coherence time appears to be limited by an additional mechanism. In combination with the present work, since $Q_0(t)$ is the manifestation of chemical potential fluctuations and since defect fluctuations occur on a broad distribution of timescales, charge noise from the AlO_x layers surrounding the Al gates could well be one possibility. It thus appears that by ameliorating or eliminating the effect of Al and AlO_x in our devices, we may be able to improve the coherence times in future experiments. Finally, looking further in the future towards large-scale quantum processors, the use of CMOS-compatible (see footnote[4]) device architectures would appear to be a sensible approach to avoid the deleterious effects of charge noise.

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References

[1] Zimmerman N M and Keller M W 2003 Electrical metrology with single electrons *Meas. Sci. Technol.* **14** 1237–42
[2] Likharev K K 1999 Single-electron devices and their applications *Proc. of the IEEE* **87** 606–32

[3] Petta J R *et al* 2005 Coherent manipulation of coupled electron spins in semiconductor quantum dots *Science* **309** 2180–4
[4] Fujiwara A, Inokawa H, Yamazaki K, Namatsu H, Takahashi Y, Zimmerman N M and Martin S B 2006 Single electron tunnelling transistor with tunable barriers using silicon nanowire MOSFET *Appl. Phys. Lett.* **88** 053121
[5] Zimmerman N M *et al* 2008 Why the long-term charge offset drift in Si single-electron tunneling transistors is much smaller (better) than in metal-based ones: two-level fluctuator stability *J. Appl. Phys.* **104** 033710
[6] Morton J J L, McCamey D R, Eriksson M A and Lyon S A 2011 Embracing the quantum limit in silicon computing *Nature* **479** 345–53
[7] Maune B M *et al* 2012 Coherent singlet-triplet oscillations in a silicon-based double quantum dot *Nature* **481** 344
[8] Pla J J *et al* 2012 A single-atom electron spin qubit in silicon *Nature* **489** 541–5
[9] Pla J J *et al* 2013 High-fidelity readout and control of a nuclear spin qubit in silicon *Nature* **496** 334 –8
[10] Tyryshkin A M *et al* 2012 Electron spin coherence exceeding seconds in high-purity silicon *Nat. Mater.* **11** 143–7
[11] Steger M, Saeedi K, Thewalt M L W, Morton J J L, Riemann H, Abrosimov N V, Becker P and Pohl H-J 2012 Quantum information storage for over 180 s using donor spins in a ^{28}Si semiconductor Vacuum *Science* **336** 1280
[12] Nordberg E P *et al* 2009 Enhancement-mode double-top-gated metal-oxide-semiconductor nanostructures with tunable lateral geometry *Phys. Rev.* B **80** 115331
[13] Lim W H *et al* 2009 Electrostatically defined few-electron double quantum dot in Si *Appl. Phys. Lett.* **94** 173502-1–3
[14] Lai N S *et al* 2011 Pauli spin blockade in a highly tunable Silicon double quantum dot *Sci. Rep.* **1** 110
[15] Hans Huebl *et al* 2010 Electron tunnel rates in a donor-silicon single electron transistor hybrid *Phys. Rev.* B **81** 235318
[16] Koppinen P J, Stewart M D and Zimmerman M N 2013 Fabrication and electrical characterization of fully CMOS-compatible Si single electron devices *IEEE Trans. Electron Devices* **60** 78–83
[17] Yang C *et al* unpublished
[18] Brown K R, Sun L and Kane B E 2006 Electric-field-dependence spectroscopy of charge motion using a single-electron transistor *Appl. Phys. Lett.* **88** 213118
[19] Christou A 1994 *Electromigration and Electronic Device Degradation* (New York, NY: Wiley-Interscience)
[20] Zimmerman N M, Cobb J L and Clark A F 1997 Modulation of the charge of a single-electron transistor by distant defects *Phys. Rev.* B **56** 7675–8
[21] Song D, Amar A, Lobb C J and Wellstood F C 1995 Advantages of superconducting coulomb-blockade electrometers *IEEE Trans. Appl. Supercond.* **5** 3085
[22] Zorin A B *et al* 1996 Background charge noise in metallic single-electron tunneling devices *Phys. Rev.* B **53** 13682–7
[23] Morello A *et al* 2010 Single-shot readout of an electron spin in silicon *Nature* **467** 687–91

Supplementary Information

Figures: C:/Neil/project documents/Papers/12_10 UNSW Q0/13_5 figures.pptx

Figure 1: SEM Zimmer-PC:C:/Neil/project documents/Papers/12_10 UNSW Q0/data/SEM micrographs/individual micrographs/OF 34 T/OF34 T 100 nm 30 deg tilt.tif.
TEM Zimmer-PC:C:/Neil/project documents/Papers/12_10 UNSW Q0/FIB and TEM graphs/TEM/Dec 17 300 kV/300000X-0009_OA50L_rc.
Circuit diagram Z-PC:C:/Neil/project documents/Papers/12_10 UNSW Q0/data/12_11 inset graph and table.pptx page 1.

Figure 2: Main: data file Molec-PC:C/Data/Runs/3.30/Q0_log_3.30_OF34T_Sep11.dat

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Inset: data file Molec-PC:C/Data/Runs/3.30/Q0_log_3.30_OF34T_Sep11_14, 15.dat
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Full plot: main plus inset in Zimmer-PC:C:/Neil/project documents/Papers/12_10 UNSW Q0/data/12_11 inset graph and table.pptx page 2

Table: Zimmer-PC:C:/Neil/project documents/Papers/12_10 UNSW Q0/data/12_11 inset graph and table.pptx page 4