A Detailed Failure Analysis Examination of the Effect of Thermal Cycling on Cu TSV Reliability

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***Abstract*— In this paper, the reliability of through-silicon via (TSV) daisy chains under thermal cycling conditions was examined. The electrical resistance of TSV daisy chains was found to increase with the number of thermal cycles, due to thermally induced damage leading to the formation and growth of defects. The contributions of each identified damage type to the change in the electrical resistance of the TSV chain were evaluated by electrical modeling. Thermo-mechanical modeling showed a good correlation between the observed damage locations and the simulated stress-concentration regions of the TSV.**

***Index Terms*— Failure analysis, finite element analysis, three-dimensional integrated circuits, through-silicon vias.**

I. Introduction

3-D STACKING of chips using through-silicon via (TSV) has become the preferred technology for achieving chip miniaturization and increased functionality [1]. This is due to its short wiring length and reduced resistance and capacitance (RC) delays, thereby improving chip performance.

The continued progress in processing and integration of TSVs requires an understanding of their reliability. Reported electromigration (EM) studies seem to agree that TSV interconnects are resistant to EM-induced voiding; any EM-induced voids were found exclusively at the intersection of Cu pad with the TSV [2]–[4]. On the other hand, there have been discrepancies in the reported studies on the effect of thermal cycling on TSV reliability. While some researchers claim not to have observed any changes in the dc electrical resistance (R_{dc}) in TSVs as a function of thermal cycling [5], [6], others have observed changes [7]. In the latter case, the observed change in the R_{dc} was attributed to the presence of impurities at the TSV bottom. This discrepancy in the reported effect of thermal cycling on TSV R_{dc} necessitates additional studies.

In a previous report, we observed that the RF transmission coefficient of the TSV daisy chain degraded with thermal cycling load [8]. This was attributed to physical changes in the TSV due to the thermal cycling process, based on limited physical analysis of the samples studied.

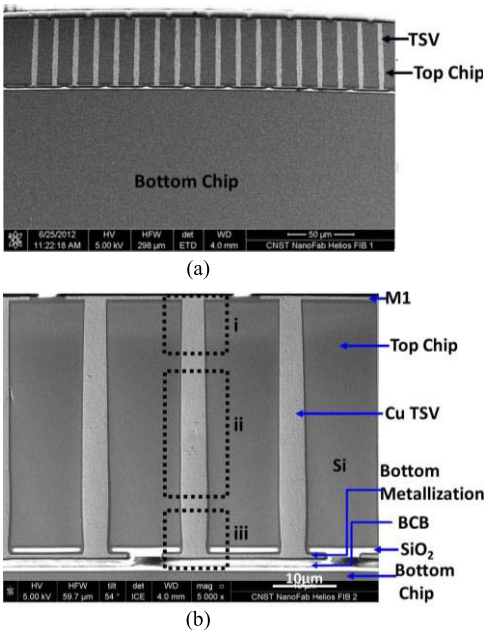

Fig. 1. SEM cross-sectional image of the stack dies used in this paper. (a) Image of the stacked dies, the top die having daisy chain of TSVs. (b) Magnified image of the TSVs. The highlighted boxes are the regions in the TSV that were studied in this paper: (i) top region, (ii) central region, and (iii) bottom region.

As a follow up to that report [8], the effect of thermal cycling on TSV reliability performance is studied by performing R_{dc} measurements in this present paper. The potential root causes for the observed changes in the R_{dc} was investigated through extensive and detailed physical failure analysis.

Additionally, thermo-mechanical modeling was performed to understand how stress distribution in the structure influences defect formation and growth, while electrical modeling was used to relate the contribution of the observed defects to the resulting resistance changes in the TSV daisy chain structure.

II. Experiment

A. Sample

For this paper, two-level stacked dies were used; the top die contained daisy chains of 60 TSVs, as shown in Fig. 1. The bonding of the dies was achieved using benzocyclobutene (BCB), while the top and the bottom metallization were

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achieved via the damascene integration process. The dimensions of TSVs used in this paper were 5 μm in diameter and 50 μm in depth with a pitch of 16 μm between the TSVs. SiO_2 ($\sim$500 nm) was used as the isolation liner, while TaN and Ta served as the diffusion barrier and adhesion layers, respectively. The seed layer for the Cu-fill consisted of Ru and Cu. The dimensions of the connecting metallization were 26 μm long, 10 μm wide, and 0.5 μm thick. TaN barrier and Ta adhesion layers are located between the TSV and the wiring level on both ends of the TSV. The front metallization (M1) is not passivated. More details on the fabrication of the stacked die are found in [9].

For the purposes of this paper, it is important to note the thermal history of the as-received samples. After TSV electroplating the wafers were annealed at 150 °C for 1 h.

The front- and back-side dielectric and etch stop depositions result in additional heat treatment of about 2 min at 350 °C and 400 °C, respectively. After front- and back-side metallization the structure was annealed at 150 °C for 1 h each.

B. Electrical Measurement and Thermal Cycling

The electrical characteristics of the samples were first measured in their as-received state, prior to thermal cycling. Subsequently, they were subjected to extensive thermal cycling in air, in which the samples were heated from 30 °C to 150 °C, then, cooled back to 30 °C. Each thermal cycle was achieved in 5.5 min. The R_{dc} measurement was then performed after every 500 cycles at room temperature. Thereafter, two samples of each test condition were retired for failure analysis purposes. The R_{dc} measurements were conducted with a two-point dc current-voltage (I-V) probe station. In this paper, all the reported error bars represent $\pm$ three times the standard deviation (sigma) of the arithmetic mean of measurements. The data variability is a composite of sample-to-sample variability and systematic experimental variability.

C. Physical Failure Analysis

After a predetermined number of thermal cycles, some samples were retired for physical analyses. The retired samples were mechanically ground and polished to reveal the center of the TSVs in the daisy chain. Thereafter, a dual-beam focused ion beam (FIB)-SEM tool (FEI Helios 650) was used to slice parallel to the cross-sectioned surface.[1] A set of two samples were prepared by FIB for each test condition (i.e., 0, 500, 1000, and 2000 thermal cycles, respectively). The FIB cut was designed to reveal three Cu TSVs per sample. Thus, a sample set comprising a total of six Cu TSVs was examined for each test condition. The duplicate samples analyzed for the as-received and the 2000 cycle test conditions showed similar damage types; hence, the observations on one sample was sufficient to summarize the damage types. However, the duplicate samples analyzed for the 500 and 1000 cycle test conditions showed different damage types, thus, both samples were needed to effectively summarize the analytical observations.

[1]Certain commercial equipment, instruments, or materials are identified in this paper to specify experimental or theoretical procedures. Such identification does not imply recommendation by NIST nor the authors, nor does it imply that the equipment or materials are necessarily the best available for the intended purpose.

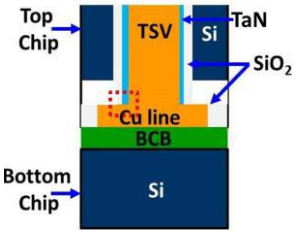


Fig. 2. Schematic of the cross section of the bottom region of the sample. Boxed area is the region where the FIB slice was taken for TEM analysis.

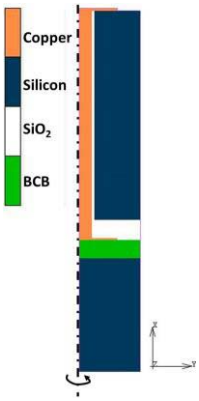


Fig. 3. Schematic of axisymmetric model used for FEM analysis.

Cross-sectional SEM images of the different areas of the TSVs were taken, *in situ*, immediately following the FIB cut. For convenience and ease of discussion, we have segmented the TSV cross sections into the top, the central, and the bottom regions of the TSV, as shown in Fig. 1(b). In performing the failure analysis, we paid particular attention to the microstructure and the presence of defects such as voids and cracks in and around the TSVs. Additionally, bright-field transmission electron microscopy (TEM) images were acquired with a FEI Titan TEM operated at 300 kV[1]. Images were taken after FIB slices of 60 nm thickness had been extracted from bulk of the TSV structures. The region of interest for the TEM study is the dashed box shown in Fig. 2. Only two test conditions were analyzed by TEM; the as-received, and the 2000 cycled samples. In all cases, the sample was first tilted toward the [110] zone axis of the surrounding Si prior to imaging.

D. Finite Element Modeling (FEM)

FEM was used to perform thermo-mechanical and electrical analyses. Thermo-mechanical analysis was performed to understand the relation between stress buildup due to thermal cycling and damage location in the structure, while electrical analysis was performed to understand how different damage types, identified by FIB-SEM analysis, contribute to the observed change in the measured electrical resistance with thermal cycling.

In the thermo-mechanical analysis, an axisymmetric model was built Fig. 3 using MSC Marc software.[1] A stress-free

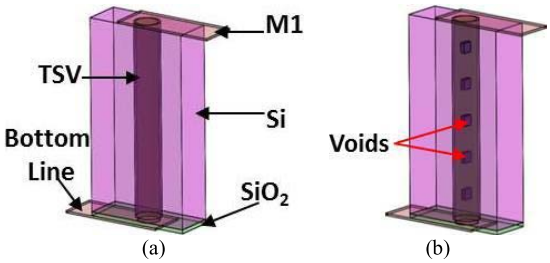


Fig. 4. 3-D model of representative unit cell used for electrical analysis. (a) Defect-free structure. (b) Structure with voids in the TSV.

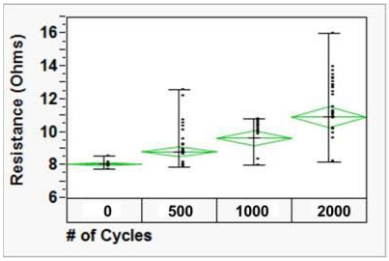


Fig. 5. Variability plot of the change in RDC with the number of thermal cycles.

temperature of 143 °C was applied, which has been reported to be about the stress-free temperature of Cu TSV [10], [11]. All materials were modeled as elastic isotropic materials, and the used values are taken from [10]. The TaN barrier, Ru seed layers were not included in the model due to their relatively insignificant thickness of about 30 nm.

For the electrical analysis, a 3-D electrical model was built using COMSOL software.[1] In this paper, parametric analysis of the influence of void/cracks found along the conducting path of the structure on the change in the R_{dc} was performed. Four different damage types were studied: 1) M1 thickness reduction due to oxidation; 2) voids inside TSV; 3) cracks at TSV-bottom metallization joint; and 4) Cracks at both TSV-M1 joint and TSV-bottom metallization joint. Sidewall cracks at TSV-TaN interface were not modeled, since R_{dc} is only influenced by changes in conducting paths. For the ease and efficiency of computation, the 3-D electrical model study was done in two steps. First, the entire 60 TSV daisy chain was modeled for the defect-free condition, to determine the total resistance of the structure, which was found to be 8.4 Ω. Thereafter, a representative unit cell (comprised of a single TSV, top and bottom Ta/TaN bilayers, Si, SiO_2 liner, the connecting M1, and bottom metallization) was modeled Fig. 4. The unit cell was used for modeling the experimental observations (i.e., effect of defects and their location) and the resistance results were then arithmetically scaled to that of the full daisy chain structure by multiplying its value by a factor of 36.7. The scaling factor was obtained by normalizing the calculated defect-free resistance for the entire 60 TSV daisy chain (8.4 Ω), to that of the defect-free representative unit cell.

For the electrical modeling, we used the following resistivity values for Cu, Si, and SiO_2, 1.80e-8 Ωm, 18 Ωm, and 1.0e12 Ωm, respectively. Based on internal SEMATECH studies, the combined contact resistance of the Ta/TaN bilayer at both ends of a single TSV is 35 mΩ.[1] This yields an equivalent resistivity of 3.4e-5 Ωm, which was used in the model. The applied current was 10 mA. The equations used for calculating the effective cross-sectional area are presented in the appendix.

III. Results

A. DC Electrical Resistance Results

Statistical analysis of the R_{dc} as a function of thermal cycling is presented in Fig. 5. Ideally, the total resistance (R_{total}) of the structure should consist of the summation of the resistance of the TSVs (R_{TSV}), top and bottom Ta/TaN adhesion and barrier layers ($R_{Ta/TaN}$), top metallization (R_{Top_Metal}), bottom metallization (R_{Bot_Metal}), and pads (R_{pad}), as shown in

$$R_{total} = \sum R_{TSV} + \sum R_{Ta/TaN} + \sum R_{M1} + \sum R_{Bot\_Metal} + \sum R_{pad}. \quad (1)$$

The data show that the mean resistance of the TSV daisy chain increases monotonically with the number of thermal cycles. In the as-received condition, the mean resistance of the TSV daisy chain is about 8 Ω. Upon thermal cycling, the mean resistance of the structure increased with the number of thermal cycles. It continuously increased by about 6%, 13%, and 38% after 500, 1000, and 2000 thermal cycles, respectively.

To understand the probable causes for the increase in resistance with thermal cycling, physical failure analyses of the TSV daisy chains were performed.

B. FIB Results

1) TSV Top Region: Fig. 6 shows the cross-sectional SEM images of retired samples from four different test conditions. Cracks were observed at the sidewall, precisely at the Cu TSV-adhesion/barrier interface in the as-received sample Fig. 6(a). While most of these sidewall cracks were pinholes-like, the longest crack was about 350 nm. After 2000 cycles, the cracks were visibly much larger. Within 6 μm of the top of the TSV, a large crack length of about 420 nm was observed Fig. 6(d). However, a much larger crack of about 1000 nm was observed at about 13 μm from the top of the TSV Fig. 6(e). For all the other test conditions, the length of sidewall cracks propagation were limited to within ~8 μm from the top of the TSV.

A statistical analysis of the sidewall crack length at the TSV-adhesion/barrier interface with respect to the number of thermal cycles is presented in Fig. 7. The crack length for the different test conditions fall within the same error margin, however, their mean crack length shows some variation. The mean crack length was constant, about 120 nm, until 500 cycles. Thereafter, the mean crack length increased to ~150 and 200 nm after 1000 and 2000 cycles, respectively.

Another damage type observed at the top region of the TSV was the roughening and propagation of voids at the top metal line (M1), leading to the reduction in the M1 thickness due to its oxidation. The as-received sample Fig. 6(a) shows a smooth

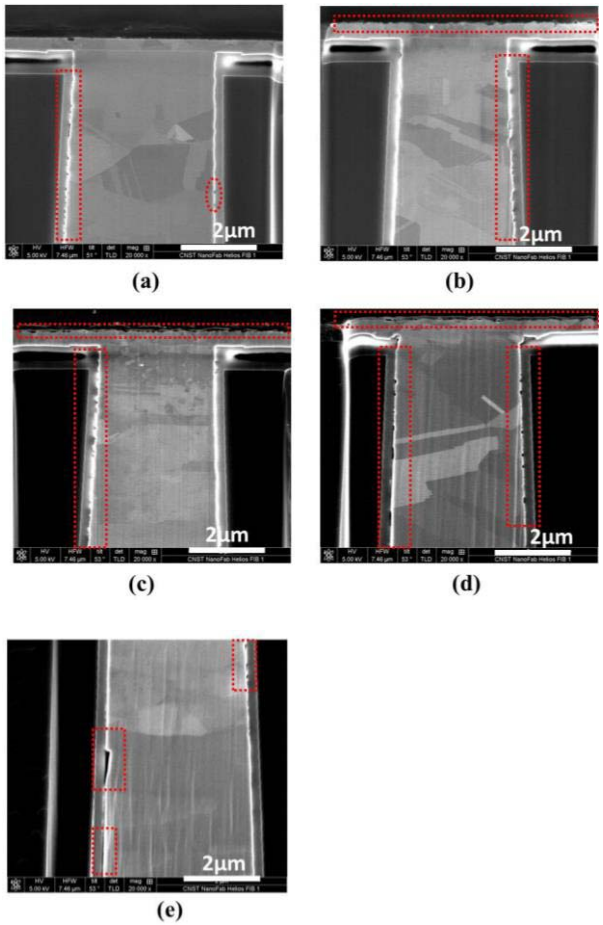


Fig. 6. SEM cross-sectional images of the top region. (a) As-received, (b) 500 thermal cycles, (c) 1000 thermal cycles, and (d) and (e) 2000 thermal cycles. The highlighted regions show the location of the cracks. Note that (e) is the lower top region of the TSV shown in (d).

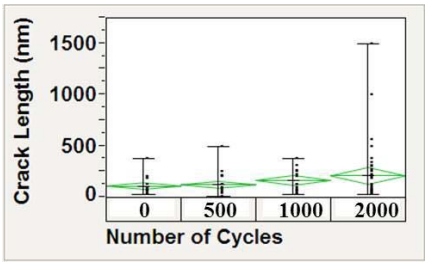


Fig. 7. Statistical analysis of the effect of thermal cycling on the growth of sidewall crack at the Cu TSV-adhesion/barrier interface.

flat metal line with no voids, however, after 500 thermal cycles Fig. 6(b), the top of the M1 begins to roughen and show some voids. At 1000 and 2000 thermal cycles, large cracks were observed to have propagated through the observed length of the M1.

Propagation of cracks along the M1-TSV interface Fig. 8 was also identified as another damage type, having a crack length of ∼350 nm. This was observed only in the duplicate sample that underwent 1000 cycles.

An apparent interaction between two different damage types was also observed, in which the cracks propagating along the

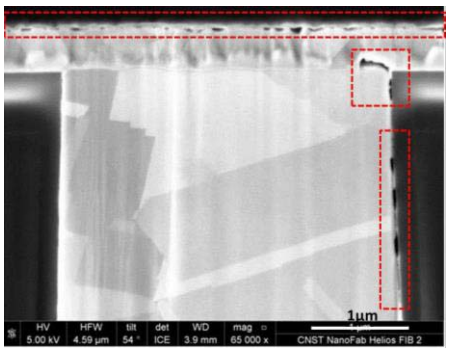


Fig. 8. SEM cross-sectional image of the top region of the duplicate sample, after 1000 thermal cycles. The highlighted regions show the location of the cracks.

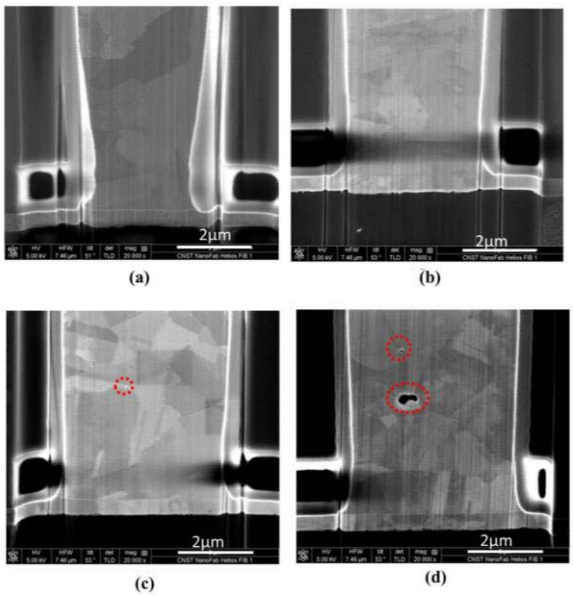
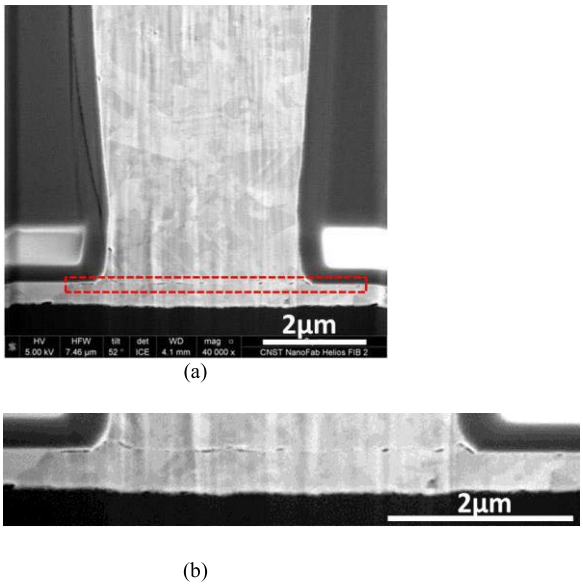


Fig. 9. SEM cross-sectional images of the bottom region. (a) As-received, (b) 500 thermal cycles, (c) 1000 thermal cycles, and (d) 2000 thermal cycles. The highlighted regions show the location of the voids.

M1-TSV interface linked up with the TSV-adhesion/barrier interface sidewall cracks, at the edge of the TSV, as shown in Fig. 8.

2) TSV Bottom Region: Representative cross-sectional SEM images for the different thermal-history test conditions are shown in Figs. 9 and 10. In this region, no sidewall crack was observed at the TSV-adhesion/barrier interface. However, few voids were observed appearing at the grain boundaries of the TSV as shown in Fig. 9. The characteristics of the voids show no discernible trend with thermal cycling. The largest void in the TSV was ∼500 nm in width.

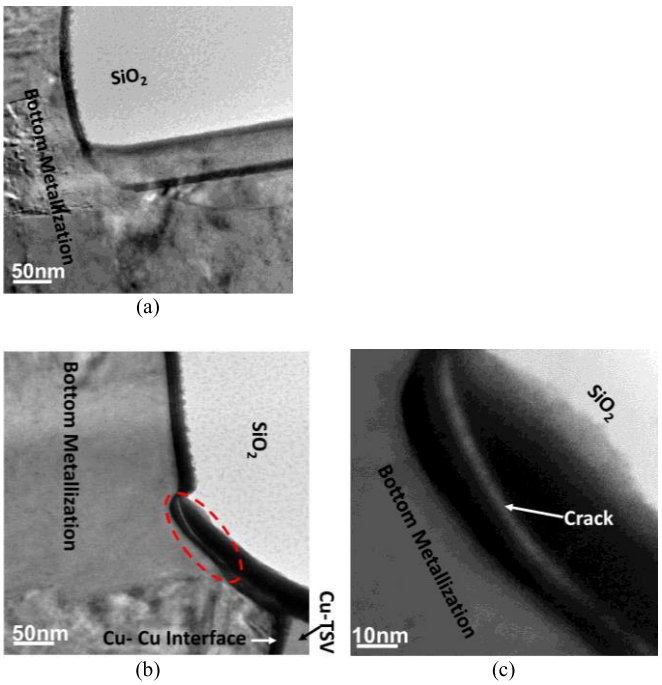
Another damage type observed at the in the bottom region was the propagation of cracks along the Cu TSV-bottom metallization interface, as shown in Fig. 10. This leads to the decrease in the effective contact area between the TSV and the bottom metallization. This is also true for the cracks observed at the TSV-M1 interface shown in Fig. 8. This damage type was observed in one of the two samples (duplicate sample) that underwent 500 cycles.



(a)

(b)

Fig. 10. (a) FIB-SEM cross-sectional image of the bottom region of the TSV of the duplicate sample after 500 thermal cycles, showing crack propagation at TSV-bottom metallization interface. (b) Magnification of the highlighted area in (a).



(a)

(b) (c)

Fig. 11. TEM image of the bottom Cu metal line-damascene SiO_2 interface. (a) As-received sample, (b) and (c) 2000 cycles. Note that (c) is the magnification of the highlighted area in (b).

3) TSV Central Region: Few void pockets were observed in the TSV microstructure, similar to those observed at TSV bottom region shown in Fig. 9, however, no clear thermal cycling dependence was observed, as voids were observed for all test conditions. No other damage types were observed.

C. TEM Results

For the TEM analysis only the as-received and the 2000 thermal cycled samples were examined. The schematic of the analyzed area within the TSV is shown in Fig. 2. In Fig. 11 the images of the junction between the bottom metallization and the damascene SiO_2 (boxed region of Fig. 2), for the as-received Fig. 11(a) and 2000 cycled Fig. 11(b) and (c) samples are shown. The junctions in both cases lack crystallinity. For the as-received sample Fig. 11(a), this junction is contiguous. On the other hand, this interface is qualitatively different for the 2000 cycled sample Fig. 11(b) and (c). Here, a long white band appears within the junction.

D. FEM Results

1) Thermo-Mechanical Analysis: Fig. 12(a) is a profile plot of the different stress components at the Cu-TSV-SiO_2 liner interface. For the principal stresses, a bow-like stress profile is observed with the minimum stresses occurring at the ends of the TSV, which increases monotonically and then saturates to a maximum value at depth between 10 μm and 40 μm into the TSV. While the radial and the circumferential stresses are approximately equal with a maximum stress of $\sim$150 MPa, the maximum axial stress was observed to be about twice their value. On the other hand, the stress-profile trend for the shear stress component is observed to be different. The absolute maximum shear stress of 130 MPa is observed to be localized at the two ends of the TSV, while a negligible uniform shear stress is observed at the central region of the structure. The Von Mises stress, which is an equivalent stress has similar profile as the shear stress, maximum stress of $\sim$200 MPa is observed at the ends of the TSV.

A plot of the stresses at the TSV-bottom metallization interface is shown in Fig. 12(b). From this graph it is observed that the absolute maximum stresses occur at or close to the edge of the TSV diameter, and decreases away from the TSV edge. At this region, the Von Mises stress is found to be as large as 250 MPa. Similar trend was also found at the top region of the TSV.

2) Electric Analysis: Fig. 13 shows the simulated change in dc electrical resistance (R_{dc}) with respect to the effective cross-sectional area or contact area for different damage types. The calculated resistance of the daisy chain without defects is 8.4 Ω; however, this value increased with the introduction of defects. Voids in the TSV do not seem to contribute much to the increasing calculated resistance. However, crack propagation along the TSV-bottom metallization joint, and at both ends of the TSV, effectively reduce the contact area, resulting in a nonlinear increase in the calculated resistance, and especially above 70% reduction in the effective contact area.

The modeling work also showed that M1 thickness reduction/loss due to its oxidation also strongly contributes to the increase in the resistance of the structure.

IV. Discussion

The simulated value of the resistance of the idealized defect-free TSV daisy chain of 8.4 Ω is close to the measured mean value of 8.0 Ω for the as-received state, as it falls with the

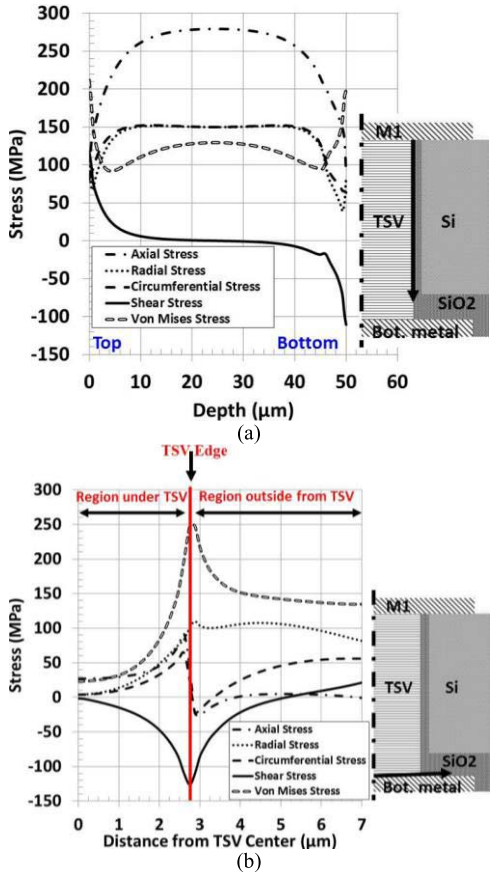


Fig. 12. Profile plot of the interfacial stresses at 30 °C (a) at the TSV-SiO_2 interface and (b) TSV-bottom metallization interface. In the schematic drawing of the modeled TSV structure, the arrow shows the area where the stress components were extracted.

error margin. Upon thermal cycling, the measured R_{dc} data showed a monotonic increase in resistance with the number of thermal cycles Fig. 5. This is attributed to the formation and growth of defects, in the structure.

The damage observed in the M1 layer Figs. 6 and 8 upon thermal cycling is due to its oxidation, as the thermal cycling process was done in air. This leads to the reduction in the thickness of the M1 layer with thermal cycling. From the simulation study Fig. 13, it can be concluded that a significant part of this increase in the measured resistance with thermal cycling can be attributed to M1 oxidation. This damage type can be mitigated by the passivation of the M1 layer.

On the other hand, as suggested by Fig. 7, the origin of the sidewall cracks at the TSV-adhesion/barrier interface may be process related, since these cracks were also observed prior to any additional thermal cycling Fig. 6(a). Above 500 cycles the mean crack length increased with thermal cycling. This suggests that thermal cycling promotes the growth of the preexisting sidewall cracks. This may be due to the high-stress localization at top region. In Fig. 12(a), both the shear stress and the Von Mises stress-profiles show the occurrence of high-stress concentration at the ends of the TSV. Thus, the localized stresses aid the propagation of preexisting sidewall cracks upon thermal cycling. These stresses occur due to the large coefficient of thermal expansion (CTE) mismatch between Cu (16.7 ppm/°C) and the surrounding SiO_2 (0.5 ppm/°C) isolation liner, as well as the matrix Si (2.3 ppm/°C) [10], [12]. Thus, the preexisting cracks at the sidewall may be acting as nucleation sites for crack propagation upon thermal cycling. Similar damage type has also been observed by [6].

Sidewall crack formation and propagation along the TSV-adhesion/barrier interface presents two serious reliability concerns. First, it could result in current leakage through the conductive Si substrate [13]. Second, it could result in Cu diffusion into the Si substrate, which is known to be detrimental to the yield and performance of front-end-of-line (FEOL) devices, due to Cu contamination [14], [15]. The TaN liner in the TSV structure acts as a barrier for Cu diffusion into Si, and as an adhesion enhancing layer [10]. Therefore, the breakdown of the Cu-adhesion/barrier interface could lead to Cu diffusion into Si which has detrimental consequences.

Voids formed in the central and the bottom regions of the TSV may have been initiated during processing and not by thermal cycling, as no clear thermal cycling dependence was observed. Since void formation is a diffusion-controlled process [16], the thermal history described in Section II is expected to result in the diffusion of atoms along the grain boundaries, leading to void formation. Based on all the analyzed FIB-SEM images of voids in TSV, the maximum anticipated change in the effective cross-sectional area of the TSV is about 2%, which should result in a minimal (<1%) change in the R_{dc} of the TSV daisy chain structure. Thus, it can be concluded that voids in TSVs have negligible impact on the increase in resistance with thermal cycling.

In Fig. 10, the propagation of cracks across the entire diameter of the TSV, at the TSV-bottom metallization interface, is attributable to thermal cycling. This is consistent with the localization of stresses at this region. Fig. 12(b) shows that the absolute maximum stress values for all stress components occurred at or close to the TSV edge, with the Von Mises stress having the highest stress value of 250 MPa. Thus, the highly localized stresses are anticipated to aid the propagation of cracks along the TSV-bottom metallization interface. These cracks initiate at the edge of the TSV where the maximum absolute stresses occurs, and then propagate inward, toward the center of the TSV. The propagation of cracks in the TSV top region along the TSV-M1 interface Fig. 8 can be explained in the same way. The fact that the TSV-M1 crack propagation is observed only at the edge of the TSV diameter Fig. 8, confirms that this damage type originates at the point of highest shear stress localization, which is at the edge of the TSV. These cracks lead to a decrease in the effective contact area of the joint. The reduced contact area at the TSV-M1 and/or TSV-bottom metallization interfaces are expected to contribute significantly to the increase in the total resistance of the structure, as shown in Fig. 13. This is consistent with the observations in Fig. 5, as its contribution to the change in resistance is anticipated to scale with the number of thermal cycles. The dramatic increase in resistance above 70% change in the contact area is due to the increased current crowding at the TSV-metallization junctions with decreasing effective contact area. At the bottom metallization-damascene SiO_2 interface of the 2000 cycled sample Fig. 11(b) and (c), a long

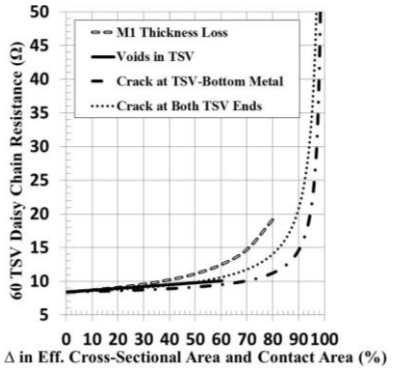


Fig. 13. Electrical modeling of the effect of the change in the effective cross-sectional area or contact area on the resistance of the TSV daisy chain.

white band was observed in the TEM images. We interpret this contrast change as a reduction in thickness, consistent with the presence of cracks, seen in the FIB/SEM images. The observed cracks are a consequence of thermal cycling.

Since R_{dc} measurement captures changes only in the electrical conducting paths, only the damage types that occur in the electrical conducting paths can be attributed to the observed increase in the TSV daisy chain resistance with thermal cycling Fig. 5. The main contributors are: 1) TSV-M1 interface cracks; 2) M1 oxidation; and 3) TSV-bottom metallization interface cracks. In contrast, the RF-based measurements in our previous report represented changes in the entire structure, not just the electrical conducting paths [8].

V. Conclusion

In this paper, the impact of thermal cycling on the reliability performance of TSVs were studied. By TEM and FIB-SEM-based analyzes, different damage types were identified. Subsequently, FEM-based thermo-mechanical and electrical analyzes were performed to understand stress distribution and R_{dc} resistance change in the structure, respectively.

The R_{dc} of the TSV daisy chain was observed to increase with thermal cycling, which is attributed to the presence of defects. Based on FIB-SEM and TEM analyses, six different damage types were observed in the TSV daisy chain; sidewall cracks, TSV voids, M1 oxidation, TSV-M1 interface cracks, TSV-bottom metallization crack, and cracks at the bottom metallization-damascene SiO_2 interface.

From electrical modeling analysis of the defects in the electrical conducting paths of the structure, it was found that the main cause for the increase in resistance (R_{dc}) with thermal cycling were due to the initiation and the growth of cracks at the M1-TSV interface, TSV- bottom metallization interface and the oxidation of the M1 metal line.

By thermo-mechanical modeling, the defect sites were correlated with the distribution of stress in the TSV daisy chain.

Appendix

In this appendix, we provide the equations and assumptions that were used to determine the effective cross-sectional area of void containing TSV that were plotted in Fig. 13. The TSV voids were all assumed to be cuboids. The voids in the TSV were assumed to have equal length (L_{void}) and width (W_{void}), while there depth (H_{void}) varied. Five voids of the same dimensions were assumed to be in a single TSV, hence, the volume of the voids (V_{void}) is a summation of all the five voids. By knowing the volume of a nonvoided TSV (V_{TSV}), the effective volume of the TSV in the presence of voids were determined, and hence the effective cross-sectional area ($A_{\mathrm{eff\_TSV}}$)

$$L_{\mathrm{void}} = W_{\mathrm{void}} \tag{2}$$

$$V_{\mathrm{void}} = \sum H_{\mathrm{void}} L_{\mathrm{void}}^2 \tag{3}$$

$$A_{\mathrm{TSV}} = \pi r_{\mathrm{TSV}}^2 \tag{4}$$

$$V_{\mathrm{TSV}} = h_{\mathrm{TSV}} \pi r_{\mathrm{TSV}}^2 \tag{5}$$

$$V_{\mathrm{eff\_TSV}} = V_{\mathrm{TSV}} - V_{\mathrm{void}} \tag{6}$$

$$A_{\mathrm{eff\_TSV}} = V_{\mathrm{eff\_TSV}} / H_{\mathrm{TSV}}. \tag{7}$$

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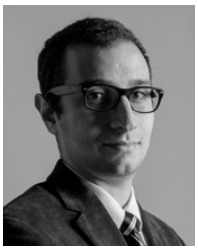

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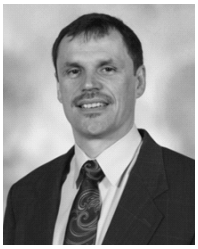

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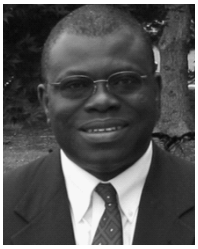

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