# EVALUATING METHODS OF SHIPPING THIN SILICON WAFERS FOR 3D STACKED APPLICATIONS

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**ABSTRACT**
An experiment was performed to develop a method for choosing appropriate packaging for shipping 300 mm silicon wafers thinned to 100 µm or less for three-dimensional stacked integrated circuits (3DS-ICs). 3DS-ICs hold the promise of improved performance and/or lower power consumption for a given function by combining multiple chips into a 3D structure. However wafers thinned to 100 µm or less, which may be sourced from fabrication facilities anywhere in the world, must be collected in a single location for integration into 3D stacks. The methods evaluated were based on the procedure specified in ISO 2248:1985, entitled "Packaging – Complete, filled transport packages – Vertical impact test by dropping." Four types of wafer packaging systems were tested. Wafers 50 µm and 100 µm thick and drop heights of 800 mm and 1200 mm were selected. A few wafers fractured during some of the tests, mainly those wafers with significant edge defects.

Key words: Drop tests, finite element modeling, temporary wafer bonding, three-dimensional stacked integrated circuits (3DS-IC), wafer bonding, wafer shipping.

**INTRODUCTION**
Three-dimensional stacked integrated circuits (3DS-ICs) hold the promise of improved performance and/or lower power consumption for a given function. Since multiple chips are combined into a 3D structure, different functions can be integrated that cannot typically be fabricated using a single process; for example, a combination of memory, logic, RF, optoelectronics, and/or MEMS could be merged into a single device stack. These wafers are typically thinned to less than 100 µm. The thinning process involves the following steps (certain processes reverse steps 1 and 2):

1. Temporarily bonding the device wafer face-down to a carrier wafer
2. Removing the contoured edge using an edge-trim process
3. Mechanical grinding, followed by chemical mechanical polishing, of the back surface to the desired thickness
4. (Optional) TSV reveal and patterning of redistribution layer (RDL)
5. Applying the back surface of the device wafer to dicing tape on a standard metal or plastic dicing frame
6. Debonding the carrier wafer from the device wafer

Steps 1 and 5 are typically done on exactly complementary tools, at a single location, necessitating that the thinned

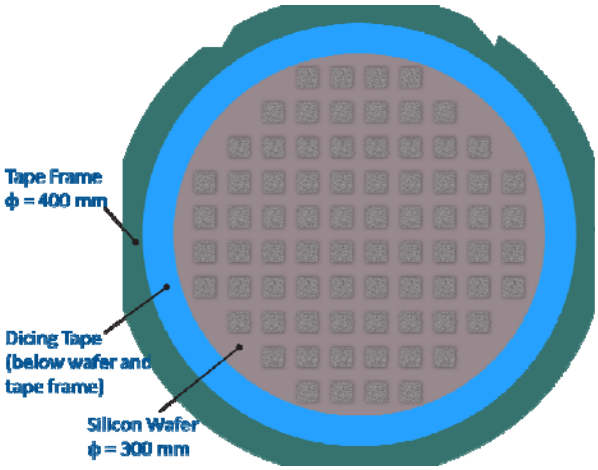



**Figure 1.** 300 mm wafer mounted on tape frame using dicing tape. The tape frame is a 400 mm diameter ring with flats and notches. The locations and dimensions of these feature are defined exactly in SEMI G74 and G87 and enable automated handling. The dicing tape is first attached to the back surface of the tape frame with the adhesive side of the tape facing the front. The wafer is subsequently attached to the adhesive side of the tape.

wafers be shipped on tape rather than shipped as bonded wafers before debonding. These thin and fragile wafers, originating from different processes in factories anywhere in the world, must be delivered to a single site for integration into 3D stacks. The means of shipping these thinned wafers becomes an enabling technology for high-volume manufacturing of 3DS-ICs.

The dimensions of silicon wafers first became standardized in the 1970s when the first edition of SEMI M1, entitled "Specifications for Polished Single Crystal Silicon Wafers" [1], was published. Through numerous revisions, the diameters have expanded from 2" (50.8 mm)[1] to 450 mm. Since single crystal silicon is a brittle material [2], to minimize breakage during processing and transport, the standard for wafer thickness has increased in lockstep with increases in diameter from 0.011" (279 µm) for 1" wafers to 925 µm for 450 mm wafers. The development of 3DS-IC technologies reverses this process, necessitating extremely thin, large diameter wafers.

SEMI's Thin Wafer Handling Task Force of the 3DS-IC Committee is developing a document, "Guide for Multi-Wafer Transport and Storage Containers for Thin Wafers," to help address issues with shipping thin wafers. To support the development of this guide, a series of experiments using thinned wafers and different classes of shipping containers is being performed. The wafers were thinned to 50 µm or 100 µm and the shipping configurations include those that hold multiple wafers horizontally or vertically; also tested were tray or clamshell configurations that can be densely stacked. In this paper, we present results from these experiments following the procedure specified in ISO 2248:1985 "Packaging – Complete, filled transport packages – Vertical impact test by dropping" [3]. In addition, results from finite-element modeling of important elements of existing wafer shipping systems are also included.

[1] Standard dimensions for 2" and 3" diameter wafers follow U.S. customary units; standard dimensions for 100 mm and larger diameter wafers follow SI units

## SHIPPING SYSTEM DESCRIPTION

### Thin Wafers on Tape Frames

According to the process described earlier, wafers are mounted on one of two types of tape frames: metal or plastic. Metal frames must conform to SEMI G74 [4]; plastic frames must conform to SEMI G87 [5]. Figure 1 shows a wafer on a tape frame. Two of the shipping boxes support only the tape frame; the remaining two types support the wafer from the tape surface as well as the tape frame.

### Wafer Shipper Types

Several types of commercially available wafer shipping boxes were suggested by their manufacturers to the Thin Wafer Handling Task Force for use with thin wafers. This experiment did not consider any prototype shipping boxes designed specifically for thin 300 mm silicon wafers. Four types of shippers were tested.

*Multi-Wafer Horizontal Shipping Boxes*

One type of horizontal multi-wafer shipping box was used in this experiment: the coin-stack shipping box. This box, shown in Figure 2, can hold up to 13 wafers on tape frames.

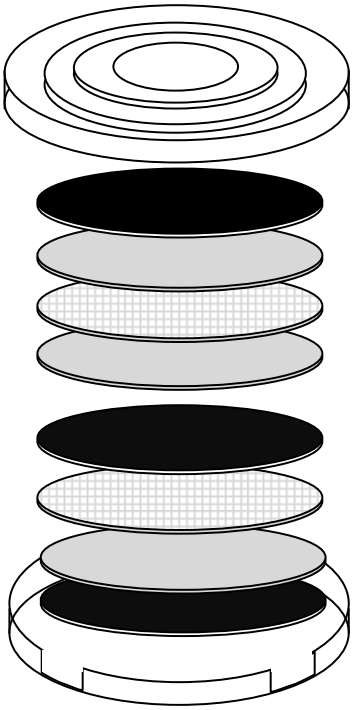


**Figure 2.** Horizontal coin-stack multiple wafer shipping box

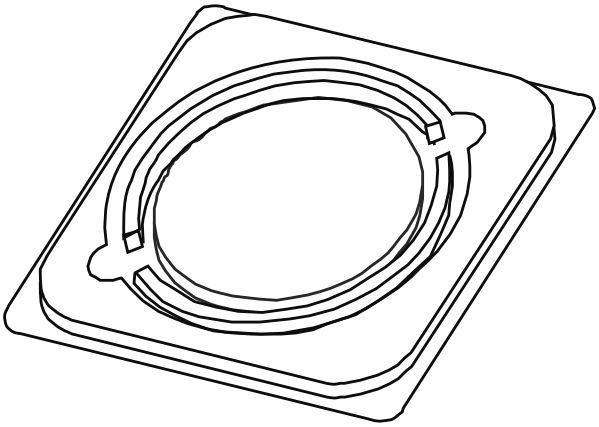


**Figure 3.** Horizontal stackable tray shipping box

It is the subject of a prospective SEMI standard, which was recently balloted as SEMI document 5295.

*Horizontal Stackable Shipping Box*
Two types of horizontal, stackable shipping boxes were included: trays and clamshells. Each is designed so that the wafer, which is on tape on the frame, is placed on a support surface and retained by a second component of the shipping box. Each of these shipping boxes is designed for a conformal fit into a 432 mm (17") x 432 mm (17") cardboard box, which represents the entirety of the secondary packaging materials.

Stackable trays are designed for wafers on a tape frame to be placed tape side down in the tray. The tape frame is held in place by putting a second tray on top of the first. Additional wafers and trays can be added to the stack. A total of n + 1 trays can be used to ship n wafers; a drawing of one of these trays is shown in Figure 3.

The clamshell box holds an individual wafer on its frame and supports the frame rigidly; it also supports the wafer indirectly through the tape. A schematic of a clamshell box such as was used in these experiments is shown in Figure 4.

*Vertical Shipping Box*
One type of vertical shipping box was used. It has slots for 13 tape frames; these slots are specifically fabricated to hold either metal tape frame (1.5 mm thick) or plastic tape frames (2.5 mm thick). This system is shown in Figure 5.

**Secondary Packaging**
Secondary packaging refers to the materials that protect the shipping box. They typically include an outer cardboard box and inner liner materials that hold the shipping box in place and dampen part of the force of any impact. When the shipping box manufacturer provided secondary packaging materials or recommended packaging materials, these were used. Otherwise, the drop test was performed using secondary packaging materials chosen according to common shipping practices.

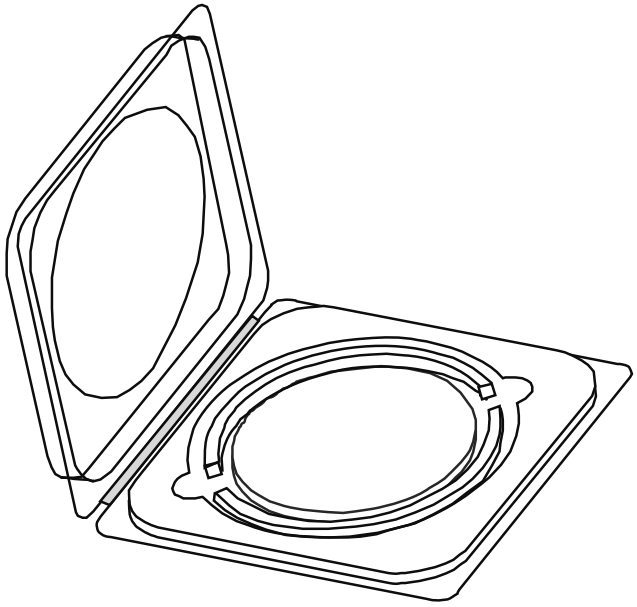


**Figure 4.** Horizontal clamshell stackable shipping box

**MEASURMENT PROCEDURE**
**Wafer Processing**
Two hundred and fifty unpatterned wafers were processed in multiple lots. Several temporary bonding process flows were used, the details of which are beyond the scope of this paper. After processing, 83 wafers mounted on dicing tape on tape frames underwent the drop tests. Of these, 47 were 100 µm thick and the remaining 37 were 50 µm thick. The 100 µm thick wafers could be further split into two groups based on the quality of the edge trim. Thirty-eight wafers had visibly poor edge quality, as shown in Figure 6a. The remaining 9, plus all of the 50 µm thick wafers, had much smoother edge quality, as shown in Figure 6b.

**Packaging procedure**
The wafers were placed in the primary package(s). For shipping boxes that could accommodate multiple wafers, all slots were filled with either wafers on tape frames or tape frames with tape but no wafer. Table 1 shows the different packaging configurations used in the experiment.

**Sensors**
Commercial-grade, single-use shock threshold sensors measured how much impact was delivered to the primary packaging. Sensors, with trigger values from 10 g to 75 g, were attached to the exterior of the primary package. These shock sensors, shown schematically in Figure 7, irreversibly change color, typically to red, when exposed to acceleration exceeding a target value in the axis, or axes, of sensitivity. The tube-style sensors used are sensitive to accelerations perpendicular to their long axis. One or more sensors were attached to the primary package during each drop test, oriented such that the sensitive axes of the sensors were aligned to the drop axis. The g-values were chosen to narrow on the expected impact value, e.g., so that at least one sensor would trigger and at least one would not.

| DROP SET | Shipping Box | Wafer Thickness | Tape Frame |
|---|---|---|---|
| 1 | Vertical, multi | 50 | Metal |
| 2 | Vertical, multi | 100 | Metal |
| 3 | Coin Stack | 50 | Metal |
| 4 | Coin Stack | 100 | Metal |
| 5 | Coin Stack | 50 | Plastic |
| 6 | Coin Stack | 100 | Plastic |
| 7 | Tray | 50 | Metal |
| 8 | Tray | 100 | Metal |
| 9 | Tray | 50 | Plastic |
| 10 | Tray | 100 | Plastic |
| 11 | Clamshell | 50 | Metal |
| 12 | Clamshell | 100 | Metal |
| 13 | Clamshell | 50 | Plastic |
| 14 | Clamshell | 100 | Plastic |
| | | ***thickness in µm** | |

**Table 1.** Design of Experiment Matrix

**Drop test**

The attitude of the drop is defined in IS) 2248:1985 [3] as the orientation of the package on impact. A rectangular box has a total of six unique faces, twelve edges and eight corners. However, since both the silicon wafers and the packaging systems exhibit certain degrees of rotational symmetry, several orientations were not tested. ISO 2248:1985 does not define a preferred drop height, but leaves this up to the user. For this experiment, two drop heights were chosen: 800 mm and 1200 mm. These roughly correspond to an unprotected impact force of 100 g (100 times earth gravity) and 150 g, respectively.

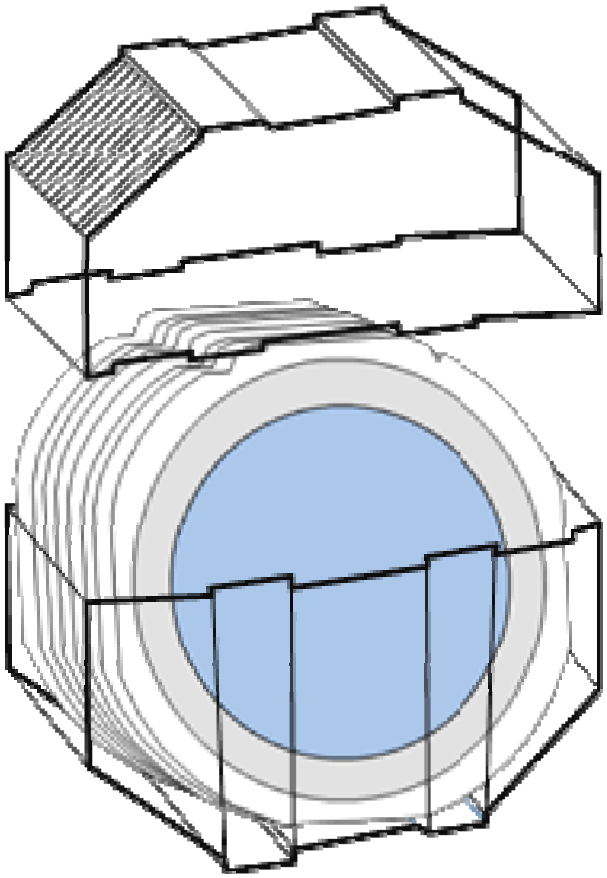


**Figure 5.** Vertical multiple wafer shipping box

A video recording was made of each drop to verify that the correct height and attitude were used. After each drop, the package was carefully opened and the contents inspected for damage to the inner packaging, shipping box, or wafers. In addition, if any or all of the shock sensors were triggered, this information was recorded and the sensors were replaced.

**Data recording**

A data sheet was developed to record the data required by ISO 2248:1985 plus any additional data relevant to the particular experiment, such as wafer descriptions and locations of shock sensors.

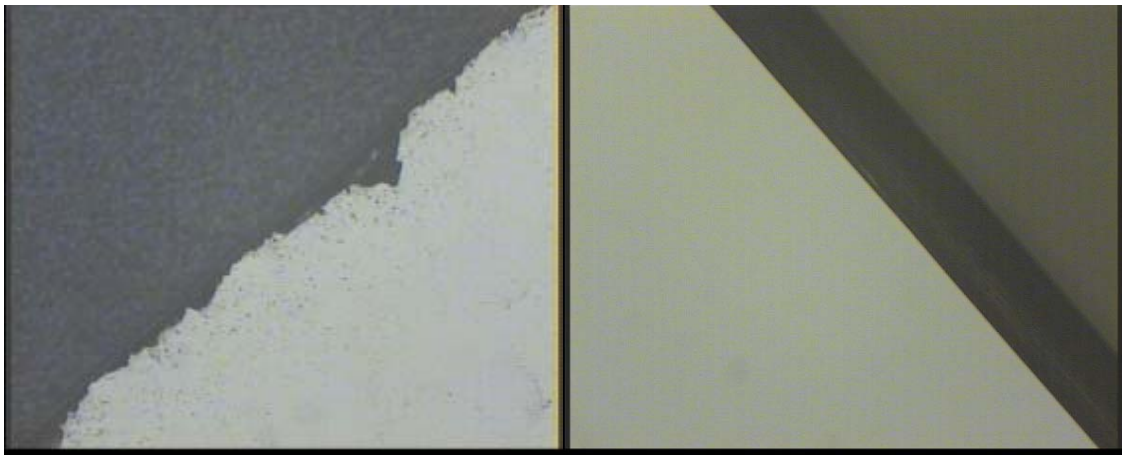
**MEASURMENT RESULTS**

The drop tests were performed at two separate times based on wafer availability; the first tests used only the poorer quality 100 µm thick wafers; the second tests included all types of both 100 µm and 50 µm wafers. During the second tests, both types of 100 µm wafers were included side-by-side to provide evidence of whether edge quality affects the fragility of similar wafers.

Overall, few wafers were broken during the drop tests. Further, none of the shipping boxes failed completely in any drop, *i.e.*, no single drop test cracked all the wafers. In the tests in which multiple wafers failed, those wafers were generally not adjacent to or even near one another, as might be expected if the forces impacting the wafers were higher in one region of the shipping box than another, e.g., if the delivered force were higher nearer the point of impact between the secondary packaging and the drop surface.

Key observations include the following:

1) Wafers with poor edge conditions were more likely to break than those with smooth edges.



**(a)** **(b)**

**Figure 6.** Edge quality of typical wafer from Lot 1 (a) and Lot 2b (b) after debonding.

2) Breaks appeared to originate from defects at the edges; see Figure 8a for a crack initiating from a large edge defect on a 100 µm wafer.
3) The drop from 1200 mm represents a severe case for shipped wafers. Visible damage to the shipping systems was observed as follows for 1200 mm drops:
    a. In one drop in which a 50 µm wafer broke the force was such that a triangular piece of the wafer delaminated from the tape in a central region of the wafer (Figure 8b).
    b. In another drop, one of the shipping boxes cracked.
    c. In multiple cases, internal secondary packaging exhibited significant deformation on impact.

Secondary packaging appeared to play a significant role in the results. That is, the shipping boxes are stiff and the tape rings with the attached wafers are held firmly in place by all configurations; in some configurations the wafer is also held firmly in place against a surface. This means that the primary packaging provided only minimal cushioning, while the secondary packaging provided the majority.

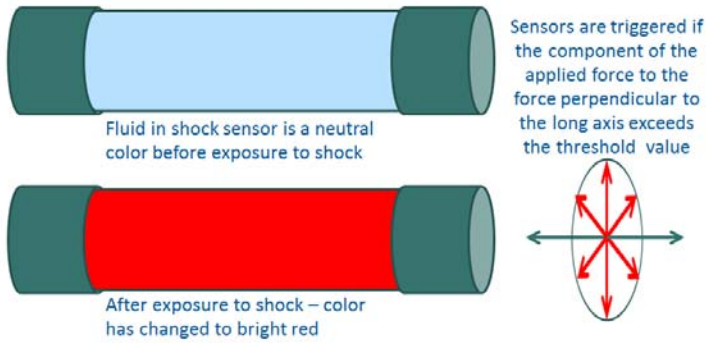


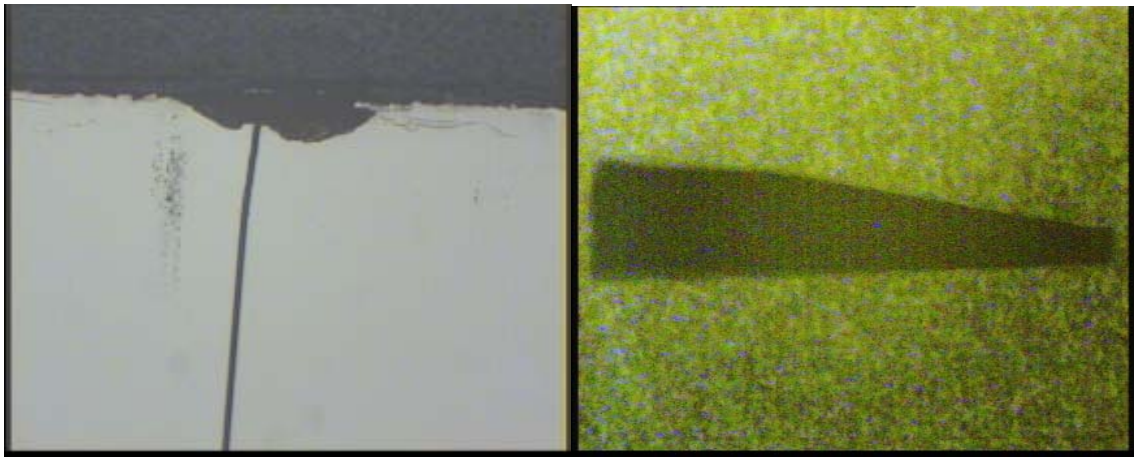

**Figure 7.** Diagram of function of shock sensor

## FINITE ELEMENT ANALYSIS OF THIN WAFERS ON TAPE FRAME

Cook [2] gave a "design stress" of 130 MPa for well-polished, full thickness wafers. However, no technique for measuring stress during a drop test of thin silicon wafers has been reported. Therefore, finite element analysis (FEA) was used to estimate the stress. The wafer-tape-metal frame system, with its standardized dimensions and known material properties, was modeled exactly. A typical maximum acceleration of 75 g was estimated from the shock threshold sensors, considering both those that did trigger and those that did not. This value should be taken as only a rough estimate of the shock applied to the wafer-tape-frame systems. Because no time history of the deceleration of the frames was available, an "ideal cushioning" assumption was made: a constant deceleration of 75 g was applied for a time period sufficient to bring the frame to a stop. With these assumptions, the calculated maximum principal stress at the wafer center was less than half of Cook's design stress of 130 MPa. The assumptions used in the calculation prevent a more precise result. However, because none of the wafers failed in the center, a stress value well below 130 MPa is consistent with expectations. The FEA produced stresses near the wafer edge that varied considerably, but with a maximum value about half the value in the center of the wafer. This low stress value can be reconciled with the experimental results by assuming that the edge defects, as shown in Figure 6a, lower the critical stress near the wafer edge to a level well below Cook's value. Some support for this interpretation can be found in the experimental results on the second lot of wafers, in which few wafer failures occurred. The failures that did occur were associated with damage to the packaging systems.

## CONCLUSIONS

We have shown a process for evaluating methods of shipping thinned 300 mm wafers. Several



**(a)** **(b)**

**Figure 8.** Break example from Lot 1, extending from a region of poor edge quality (left) and a break on a Lot 2b wafer, where the force delivered to the wafer was enough to detach a triangular piece of the wafer from the dicing tape (right).

different classes of tape frame wafer shippers were suggested for use in this application; all gave acceptable results.

The fragility of the wafers should be considered when choosing the shipping configuration. It was clear from the results that the likelihood of breakage for any specific drop was increased with poorer quality edges.

The results suggest that perhaps the key differentiating factor among the shipping systems tested is the performance of the secondary packaging.

Estimated stress values at the wafer centers and edges in these drop tests, calculated by FEA of the wafer-tape-frame system with the use of boundary conditions roughly estimated to correspond to the present set of tests, may be interpreted as showing that the "design stress" level for these thinned wafers is significantly reduced by defects at the wafer edges. For wafers with severe edge defects, the level is well below the literature value [2] of 130 MPa for well-polished, full thickness wafers.

Based on the results, all of the options evaluated handled both wafer thicknesses adequately. Ultimately the shipping method needs to be qualified by each user. The standard that will result from D5175 is intended to provide a guideline for an experimental procedure that can be used to make this decision.

**ACKNOWLEGEMENTS**

The authors would like to thank Raghu Chaware of Xilinx and Janet Cassard of NIST for discussions and Dr. Stephanie Hooker, Chief of the NIST Materials Reliability Division, for technical support.

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