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On the Contribution of Bulk Defects on Charge Pumping Current

Jason T. Ryan, *Member, IEEE*, Richard G. Southwick, III, *Member, IEEE*, Jason P. Campbell, *Member, IEEE*, Kin P. Cheung, *Senior Member, IEEE*, and John S. Suehle, *Fellow, IEEE*

***Abstract*—Frequency-dependent charge pumping (CP) (FD-CP) has emerged as a popular technique for studying the spatial and energetic distribution of defect centers in advanced high-k gate stacks. However, conflicting interpretations of the CP frequency–defect depth relationship has led to controversial and inconsistent findings between various groups. A key assumption is that most, if not all, bulk defect trapping/detrapping contributes to the CP current. In this paper, we show, experimentally using two independent measurements, that there is a large discrepancy between the total amount of bulk defect trapping/detrapping that occurs and the actual CP contribution due to these defects. We argue that the CP current due to bulk defects depends heavily upon the specific device geometry/technology, the minority-carrier lifetime, and FD-CP's general inability to function as a defect profiling tool.**

***Index Terms*—Bulk defects, charge pumping (CP), charge trapping, high-k dielectrics.**

I. Introduction

CHARGE PUMPING (CP) is perhaps the most powerful and universally utilized tool available for the quantitative assessment of interface defects in metal–oxide–semiconductor field-effect transistors (MOSFETs). Since its conception, many CP-based methodologies have been developed with the goal of extracting defect information [1]–[3]. This is particularly true for the study of high-k-based gate stacks since they tend to suffer from increased interface defect densities and nonnegligible densities of bulk defects in the interfacial layer and/or bulk dielectric [4]–[12]. These additional defects frequently result in complicated and controversial CP measurements since bulk defect trapping and/or detrapping can contribute to the measured CP current (I_{CP}) [4]–[12]. In fact, many studies have embraced the bulk defect I_{CP} contribution and have attempted to use CP as a tool to spatially profile bulk defects by establishing a defect-depth-to-CP-frequency relationship [4]–[8], [10]–[12]. The details and validity of these frequency-dependent CP (FD-CP) measurements are an ongoing debate [9]–[11]. An important aspect of establishing the defect depth–frequency relationship is that the measured increase in I_{CP} due to bulk defects is equal to the participating bulk defects. A less quantitative requirement is that the increase in I_{CP} is proportional to the participating bulk traps. It is difficult to ensure that these requirements are met.

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The authors are with the Semiconductor and Dimensional Metrology Division, National Institute of Standards and Technology, Gaithersburg, MD 20899 USA (e-mail: jason.ryan@nist.gov; richard.southwick@nist.gov; jason.campbell@nist.gov; kin.cheung@nist.gov; john.suehle@nist.gov).

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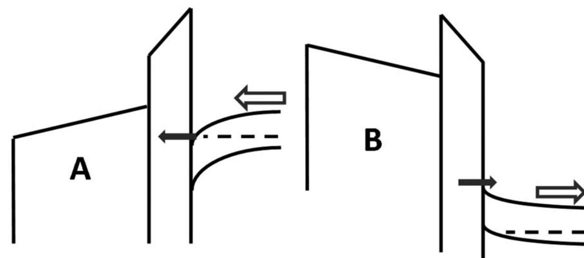

Fig. 1. Schematic illustration of direct (a) trapping and (b) detrapping without the mediation of an interface defect.

In the classic view of CP, bulk defects participate through a two-step interface-defect-mediated process where substrate charge must first be captured at an interface defect before tunneling into a bulk defect [3]. A recent work by Zhang *et al.* [9] has argued that, due to geometric and energetic constraints, bulk defects are unlikely to participate in CP through this mechanism (particularly in highly scaled production-quality devices). Recently, a second mechanism has been considered when the density of bulk defects is relatively high (as is the case for high-k gate stacks). In this mechanism, schematically shown in Fig. 1, charges can directly tunnel into (trapping) and out of (detrapping) bulk defects without the mediation of an interface state. The trapping component charges come from the inversion layer. When these charges detrap (during accumulation), they can contribute to I_{CP} via recombination in the substrate. If all the detrapped charges are converted to I_{CP}, then one can rely on this to extract a depth profile of the defects near the substrate conduction band edge. If only part of the detrapping charges recombine and are converted into I_{CP}, one can still get a proportional defect depth profile as long as the conversion fraction is constant.

In this paper, we use two independent measurement techniques to quantify the component of measured I_{CP} due to bulk defect participation. We find a stark contrast between the total charge trapping/detrapping that occurs compared to the total charge trapping/detrapping that is converted into I_{CP}. Such a finding suggests that FD-CP is incapable of providing defect depth profile information in most cases.

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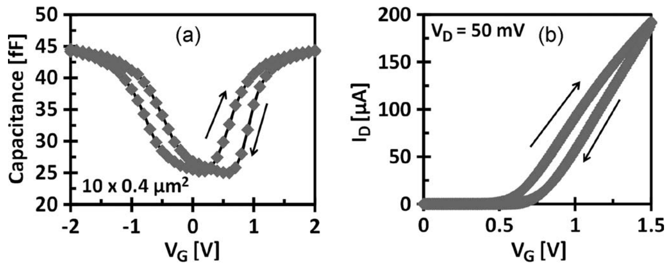

Fig. 2. "Slow sweep" (a) C–V and (b) I_D–V_G indicating large amounts of bulk dielectric charge trapping.

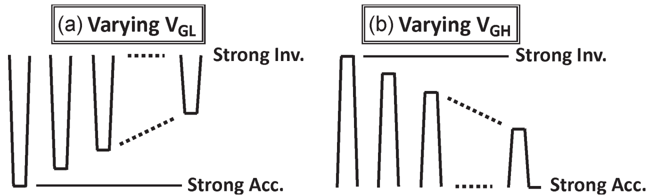

Fig. 3. Schematic representations of the CP pulse conditions. (a) Varying $V_{\rm GL}$ allows probing of the lower half of the bandgap. (b) Varying $V_{\rm GH}$ allows probing of the upper half of the bandgap.

II. Experimental Details

The devices used are 10 μm $\times$ 0.25 μm n-channel MOSFETs with gate stacks consisting of a 1-nm SiO_2 interfacial layer (2-nm thermal oxide etched back to 1 nm), 7-nm atomic-layer-deposited HfO_2, and a TiN metal gate. "Slow sweep" capacitance versus voltage (C–V) and drain current versus gate voltage (I_D–V_G) measurements (Fig. 2) clearly display significant hysteresis, indicating significant amounts of bulk dielectric electron trapping. CP measurements were made following the interface defect spectroscopy methodology reported recently [13], [14]. The technique is similar to variable-height CP [2], [15] but with the added requirement of using CP frequencies low enough to ensure sufficient interface defect fill times. Simple square wave V_G pulses are applied with the source/drain grounded, while the substrate current ($I_{\rm CP}$) is measured.

The upper half of the bandgap is measured by fixing the low-voltage portion of the CP pulse ($V_{\rm GL}$) at strong accumulation ($V_{\rm GL} = -1.5$ V in these samples) while sequentially stepping the high-voltage portion of the CP pulse ($V_{\rm GH}$) from strong inversion deep into depletion. The lower half of the bandgap is measured by fixing $V_{\rm GH}$ at strong inversion ($V_{\rm GH} = +1.5$ V in these samples) while sequentially stepping $V_{\rm GL}$ from strong accumulation deep into depletion. Fig. 3 schematically shows the pulse conditions for fixed-$V_{\rm GH}$ and fixed-$V_{\rm GL}$ cases, while Fig. 4 shows the measured results for a CP frequency of 2 kHz. By varying the pulse height in this fashion, we obtain $I_{\rm CP}$ as a function of probed energy window (determined by the Fermi-level positions during $V_{\rm GH}/V_{\rm GL}$) in the bandgap [13], [14]. Since $I_{\rm CP}$ is directly proportional to interface defect density (in the absence of bulk defects), this approach allows the extraction of interface defect density of states versus bandgap energy [13], [14]. $I_{\rm CP}$ only saturates when biasing between strong accumulation and strong inversion. Saturation is not seen in Fig. 4, likely due to unsaturated bulk contributions.

To push the measurement window toward the band edges, pulse rise (t_r) and fall (t_f) times were both held at 2.3 ns for all

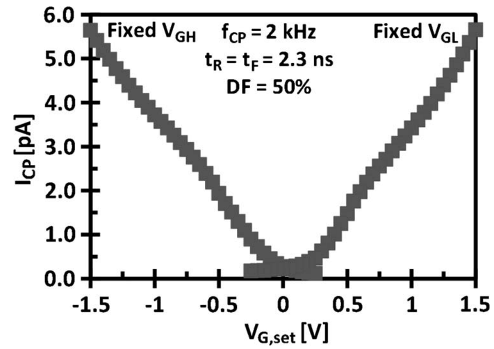

Fig. 4. Measured $I_{\rm CP}$ versus V_G for the case of (left-hand curve) fixed $V_{\rm GH}$ and (right-hand curve) fixed $V_{\rm GL}$. It is reasonable to assume that the data are heavily influenced by the participation of bulk dielectric defects.

measurements. With our device geometries and rise/fall times, CP geometric effects are negligible. For each bias condition, FD-CP is performed at 1, 2, 3, and 4 kHz. Such low CP frequencies are necessitated by the fact that some of our bias conditions (for example, when half of the pulse is pushed into depletion) result in extremely low densities of charge carriers available to fill the interface defects and complete the CP cycle, as previously reported [13], [14].

The second experimental technique used is ultrafast I_D measurements. This is accomplished with a custom-built amplifier circuit mounted directly on the end of a standard wafer probe micromanipulator. By keeping the signal path between the device under test and the fast amplifier circuit as short as possible ($\sim$1 cm), we are able to obtain full I_D–V_G curves in less than 100 ns with high accuracy. V_G waveform integrity is maintained with a custom-built coaxial probe tip (50 Ω terminated within 0.5 cm of the gate contact). Drain bias voltage "droop" is eliminated with bypass capacitors.

III. Results and Discussion

Our device clearly suffers from significant amounts of bulk defect trapping (Fig. 2). Thus, it is reasonable to assume, particularly with our low CP frequencies, that the data shown in Fig. 4 contain large amounts of bulk defect CP contributions. Bulk defects can influence the CP measurement in two ways. First, detrapped charges can contribute to $I_{\rm CP}$ via recombination in the substrate (detrapped charge contribution). Second, trapped charge causes the effective V_G experienced by the channel ($V_{G,\rm eff}$) to differ from the applied V_G ($V_{G,\rm set}$). Experimentally quantifying both of these effects is possible, and the next two sections discuss the procedures.

A. Detrapped-Charge Contribution

As previously mentioned, direct tunneling of substrate charge in bulk defects without interface defect mediation is the only mechanism considered. Recently, a simulation-based methodology to account for this contribution to $I_{\rm CP}$ has been reported [8]. Although it is not specifically discussed, this work seems to provide a simulation-based pathway toward the quantification of the bulk defect contribution [8].

However, like all simulations, this approach [8] relies on assumptions. For example, minority-carrier lifetime must be

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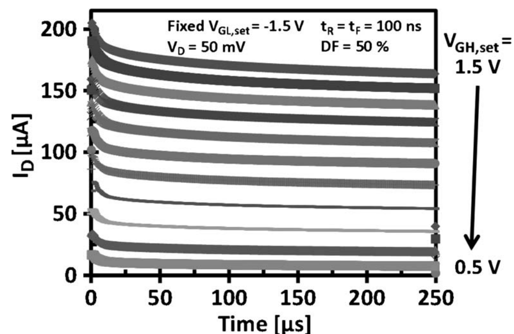

Fig. 5. I_D-versus-time curves intended to mimic the fixed-$V_{\rm GL}$ CP case (right-hand curve of Fig. 4). Only the inversion half cycle is shown.

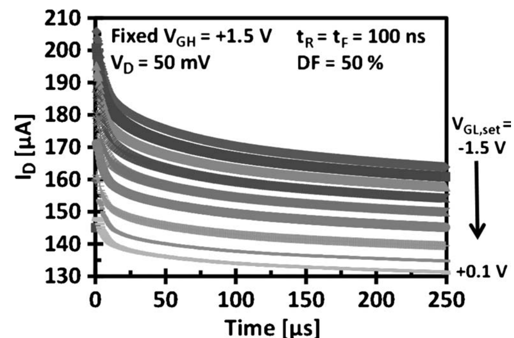

Fig. 6. I_D-versus-time curves intended to mimic the fixed-$V_{\rm GH}$ CP case (left-hand curve of Fig. 4). Only the inversion half cycle is shown.

assumed to calculate the recombination efficiency. Unfortunately, bulk minority-carrier lifetimes are very difficult to accurately measure [16], [17]. While reported minority-carrier lifetimes for silicon can vary wildly, the most common values are in microseconds [16], [17]. However, it has been shown that, due to surface recombination effects, bulk minority-carrier lifetime measurements always yield an *underestimate* [16]. The fact that some studies of production-quality silicon report lifetimes up to tens of milliseconds suggests that the commonly reported values can be quite erroneous for modern silicon MOSFETs [16], [17]. In view of this issue and other difficulties, we choose to take an experimental approach to understand the bulk trapping component in CP measurements.

First, we will quantify how much total charge trapping/detrapping occurs during our CP measurements. This requires a series of ultrafast I_D-versus-time traces taken under conditions that mimic our CP conditions in Fig. 4, measuring I_D while applying the same V_G pulse train to the gate. Fig. 5 mimics the CP case of fixing $V_{\rm GL}$ at strong accumulation while sequentially varying $V_{\rm GH}$ (right-hand curve of Fig. 4), and Fig. 6 mimics the CP case of fixing $V_{\rm GH}$ at strong accumulation while sequentially varying $V_{\rm GL}$ (left-hand curve of Fig. 4). Both Figs. 5 and 6 only show the inversion half cycle ($V_{\rm GH}$) of the pulse train. Notice the significant I_D degradation in both cases due to charge trapping. It is important to note that these measurements are done with repetitive pulses and therefore represent steady state, which means that detrapping during accumulation exactly balances trapping during inversion. Thus, by quantifying the trapping behavior, we automatically obtain the detrapping behavior.

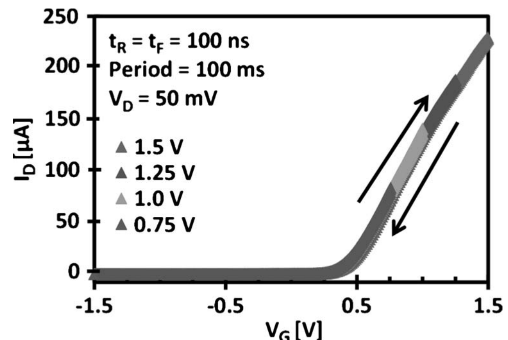

Fig. 7. “Trapping-free” I_D–V_G curves for various values of peak V_G made within 100 ns, too fast for significant bulk defect participation.

To quantify the trapping, a simple method is used to translate the I_D degradation (ΔI_D) to threshold voltage shift ($\Delta V_{\rm th}$) (or gate overdrive degradation). To accomplish that, we need to know the ideal (free of charge trapping effects) I_D–V_G relationship. We obtain this calibration curve by measuring an I_D–V_G curve on a time scale too fast (100 ns) for the bulk defects to respond. This “trapping-free” curve is shown in Fig. 7, and the lack of hysteresis is evidence that it is void of any significant bulk defect effects. Shown in Fig. 7 are various values of peak $V_{\rm GH}$ amplitude (+0.75–+1.5 V) with a fixed $V_{\rm GL} = -1.5$ V. To ensure complete detrapping, a low duty cycle is utilized.

After we translate ΔI_D to $\Delta V_{\rm th}$, we need to link $\Delta V_{\rm th}$ to charge trapping. Following [18, eq. (3)] and rearranging into the form of $Q = CV$, we have

$$N_{\rm trap} \cdot q = \frac{\varepsilon_0 \cdot k}{x} \cdot \Delta V_{\rm th} \quad (1)$$

where $N_{\rm trap}$ is the number of bulk defects, q is the electronic charge, ε_0 is the permittivity of free space, k is the dielectric constant, and x is the distance of the bulk defects away from the gate electrode. Dividing through by the time allowed for detrapping results in an average detrapping current.

However, to do so requires knowledge of the trap distribution. This, of course, is unknown. Since bulk trapping is most likely to exist in the 7-nm high-k layer, we assume that the majority of the bulk trapping component lies between 1 (interfacial layer thickness) and 8 nm from the silicon interface. To simplify, we assume that all trapped charges form a sheet of charge at some distance x from the interface. This distance is roughly the distance reachable by the tunneling front at the CP frequency. With this charge centroid location and the dielectric thickness, we can quantitatively link the I_D degradation to how much charge trapping (and, thus, detrapping) has occurred [18].

Consider first the case of CP between strong accumulation and strong inversion in Fig. 4, plotted separately in Fig. 8 (also included is the relative $\Delta V_{\rm th}$ shift). Using the earlier analysis, we obtain an average trapping/detrapping current on the order of 100 pA–1 nA for a CP frequency of 2 kHz, depending on our choice of charge centroid location (x) and the k values of both the SiO_x interfacial layer [19] and bulk HfO_2. Even if we take the conservative low end estimate, this value is still much larger than the measured $I_{\rm CP}$ value for the same bias conditions (about 5.5 pA in Fig. 4). Since $I_{\rm CP}$ is the sum of interface and

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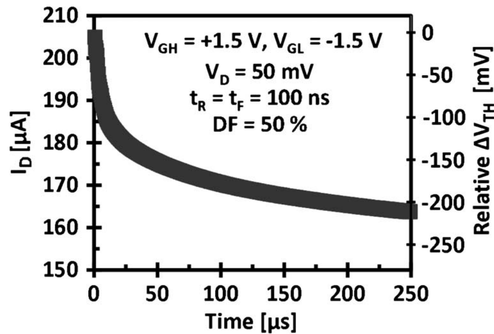

Fig. 8. I_D-versus-time trace and associated relative ΔV_{th}, for the case of mimicking CP between strong accumulation and strong inversion. The average current associated with this trapping-induced I_D degradation is on the order of 100 pA—1 nA.

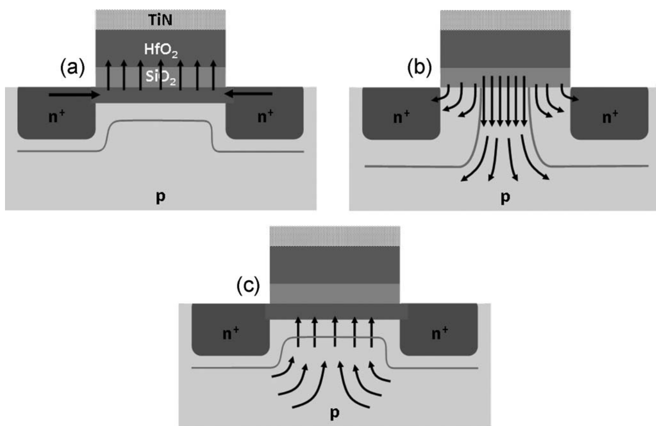

Fig. 9. Simplified drawings illustrating (a) charge capture (trapping) from the source/drain in the bulk dielectric during inversion, (b) "long" channel accumulation where significant charge enters the substrate (detrapping) as minority carriers, and (c) inversion which results in the back diffusion of unrecombined electrons.

bulk defect contributions, the bulk defect contribution must be less than 5.5 pA. This is an important result of this work. It experimentally shows that, at least in this specific case, a small fraction of the detrapping charges from bulk defects contribute to I_{CP}. Note again that, with the device geometries and pulse rise/fall times used, CP geometric effect is negligible. This low efficiency is a bad sign for the utility of FD-CP as a tool for bulk defect profiling.

How can one explain the extremely low efficiency? In the simulation paper mentioned earlier [8], two modes of charge detrapping contribute to I_{CP}. One mode is a relaxed trap in a "deep" region that contributes directly through the capture of a hole during the accumulation half cycle. This mechanism is often invoked to explain the phenomenon of random telegraph noise in I_D [20]. If this is true, the fact that some RTN can have very long time constants ($\sim$10 s), much longer than the half-cycle time allowed for all practical CP frequencies ($< 500\ \mu$s), suggests that "deep" defects with long time constants do not participate in the CP process. In other words, most of the charge trapped during inversion detraps into the substrate as minority carriers during accumulation.

Fig. 9 schematically shows the bulk charge detrapping in real space. When the MOSFET is biased into inversion [Fig. 9(a)], inversion-layer electrons directly tunnel into bulk defects. Since inversion charges come from the source/drain, this process does not contribute to I_{CP}. When the device is quickly pulsed into accumulation [Fig. 9(b)], detrapping occurs, and the emitted electrons enter the substrate as minority carriers. Two possibilities can occur. First, detrapped electrons may enter the source/drain depletion regions where they experience a horizontal electric field and are immediately swept into the source/drain and do not contribute to I_{CP}. Second, detrapped electrons may enter the substrate in the field-free region and are free to diffuse into the substrate as minority carriers. Some of these electrons can recombine with holes (majority carrier) and contribute to I_{CP}. If the MOSFET has a large field-free region (long-channel device), most emitted charges become minority carriers and freely diffuse in the substrate and eventually may recombine. If the MOSFET has a small field-free region (short-channel device), most emitted charges are immediately swept into the source/drain. Thus, one factor affecting the conversion efficiency is device channel length. Note that CP frequency should have no effect on this factor.

For the fraction of emitted charges that are diffusing in the substrate as minority carriers, the conversion efficiency to I_{CP} depends on the minority-carrier lifetime. As discussed earlier, while a specific lifetime value is difficult to justify, evidence suggests that modern production-quality silicon substrates have a minority-carrier lifetime on the order of milliseconds or more [16], [17]. As a result, most of the diffusing minority carriers remain unrecombined during the time scale of our CP measurements (half cycle of 125 μs for a CP frequency of 4 kHz). When the device is biased back into inversion [Fig. 9(c)], unrecombined charges simply back diffuse toward the depletion region around the channel and enter the inversion layer, leading to a low conversion efficiency. The conversion efficiency is clearly a function of CP frequency—longer time for recombination allows more recombination. The combination of a small percentage of emitted electrons entering the substrate as freely diffusing minority carriers and low recombination efficiency explains why the overall efficiency of converting detrapping charge to I_{CP} is small.

In the absence of bulk defect contributions (interface defects only), I_{CP} increases linearly with CP frequency. Bulk defect contribution to I_{CP}, on the other hand, decreases with higher CP frequency. Thus, any bulk defect contribution, no matter how inefficient, will be revealed as a nonlinearity in an I_{CP}-versus-frequency measurement, as shown with the representative measured data of Fig. 10 (dotted lines drawn arbitrarily as a guide). As a side note, these simple intuitive statements are the basis for defect depth profiling via FD-CP.

Fig. 10(a) is for the case of CP between strong inversion ($V_{\mathrm{GH}} = 1.5$ V) and strong accumulation ($V_{\mathrm{GL}} = -1.5$ V), while Fig. 10(b) is for the case of CP between strong inversion and deep depletion ($V_{\mathrm{GL}} = 0.25$ V). Both sets of data clearly display a nonlinearity. Before we can attribute the nonlinearity to bulk contributions, we must first rule out the possibility that the nonlinearity is caused by an interface defect filling time issue.

As previously mentioned, the time it takes for all interface defects within the allowed recombination energy window to fill with charge carriers is inversely proportional to the number of

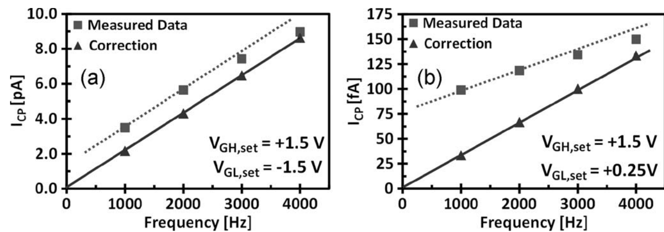

Fig. 10. FD-CP for the case of CP between (a) strong inversion and strong accumulation and (b) strong inversion and deep depletion (dotted lines drawn arbitrarily). Also shown are the correction curves discussed in the text. The difference between the two curves is the bulk defect contribution to I_{CP}.

carriers available to fill the defects. When one-half of the CP pulse is varied deep into depletion, the carrier density during depletion can become quite small. If ample time is not given, defects expected to participate in the CP process no longer contribute to I_{CP}, resulting in a detrimental loss in charge per cycle. Note that this effect will make I_{CP} appear to decrease with higher CP frequency and can be confused with the effect of bulk defect contribution. This is a potential cause of the nonlinearity in Fig. 10(b). However, when biasing between strong inversion and strong accumulation, the available carrier density is sufficiently high enough to support CP frequencies of many megahertz, yet a nonlinearity is still observed for this case [Fig. 10(a)], clearly indicating that the nonlinearity is not due to interface defect filling time issues.

Now that we can reasonably assume that the nonlinearity is due to bulk defect participation, we use the FD-CP data to determine the I_{CP} contribution due to detrapping charge. Assuming that the minority-carrier lifetime is long compared to the CP half cycle, there are two factors that affect the net recombination, namely, minority-carrier concentration and the time available for recombination. Referring to Fig. 8 (and, similarly, for all bias conditions in Figs. 5 and 6), on the time scale of our measurements, the majority of trapping occurs within approximately the first 100 μs of the inversion gate pulse. Beyond that time, I_D is saturating for the rest of the CP half cycle. We can expect the same for the detrapping process because the two are balanced. When recombination is consuming little of the minority-carrier concentration, it is a good approximation to take the concentration as constant and independent of the CP frequency (at least for long minority-carrier lifetimes and our low CP frequencies). If the amount of charges available for recombination is constant, the recombination rate must also be constant. Consequently, the time allowed for recombination determines the total amount of recombination. Thus, CP at 1 kHz will have four times the amount of recombination as CP at 4 kHz simply because four times the amount of time for recombination is allowed.

We are now in the position to construct correction curves and determine the bulk defect contribution by implementing three criteria: 1) I_{CP} scales linearly with frequency (absence of bulk defects); 2) I_{CP} must cross the origin (zero I_{CP} and 0 Hz). Gate leakage is negligible at our CP conditions, and careful calibration resulted in negligible measurement offset; and 3) the ratio of bulk defect contributions to I_{CP} at 1 and 4 kHz is four to one. Using these criteria and the procedure shown in Fig. 11,

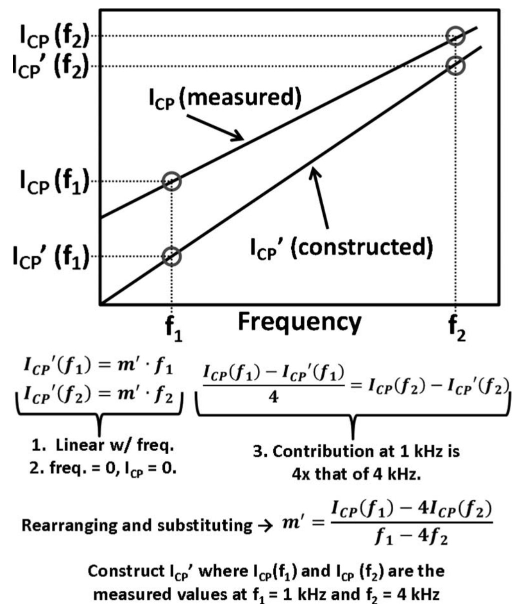

Fig. 11. Procedure to construct the correction curves of Fig. 10.

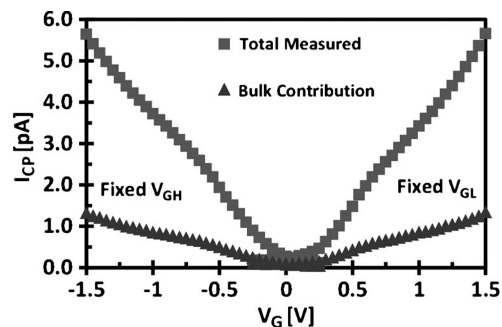

Fig. 12. Measured I_{CP} versus V_G compared to the I_{CP} contribution due to bulk defect participation.

one unique solution exists, and the correction curves of Fig. 10 are constructed.

The difference between the measured data and the correction curve, for each value of CP frequency, is the I_{CP} contribution due to bulk defect participation. Repeating the procedure for all bias conditions utilized in Fig. 4 allows us to quantify the amount of bulk defect participation over the entire range of our measurement. This is shown in Fig. 12 which compares the measured total I_{CP} and the contribution from bulk defect participation. It should be noted that arbitrarily varying the four-to-one ratio over a reasonable range has little effect on the correction value, supporting our assumption of a roughly constant recombination rate. The extracted bulk defect contribution represents roughly 1%–0.1% (depending on our previous assumptions) of the total detrapped charge.

It is important to note that the bulk contribution we quantified represents only a small fraction of all detrapping that occurs and is thus not an accurate or quantitative representation of all bulk defects present in the dielectric. Simply put, the value we extract should not be used to develop bulk defect spatial profiles, bulk defect densities across process splits, or other quantitative bulk defect properties.

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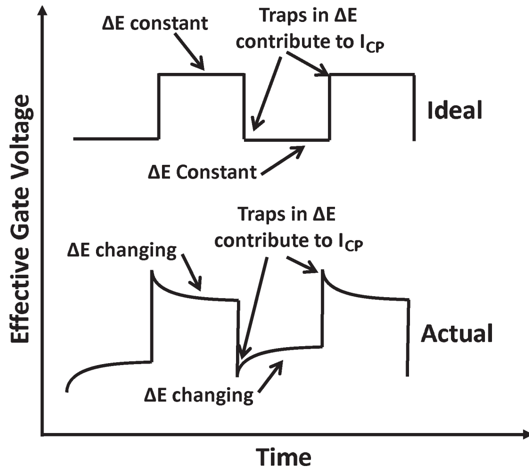

Fig. 13. Schematic drawing of (top) an ideal CP V_G pulse train and (bottom) a more realistic CP V_G pulse train which takes into account the effective V_G variations due to significant charge trapping. The extraction points for determining $V_{G,\mathrm{eff}}$ are at the very end of V_{GH} and very end of V_{GL}.

B. Effective Gate-Voltage Variations

We next consider the effect trapping/detrapping has on the effective gate voltage experienced by the channel. This effect results in a distortion of the V_G axis (x-axis) of Figs. 4 and 11. In order to completely understand the role of bulk defect participation on CP measurements, it must be quantified.

Very similar to determining the total charge trapped/detrapped during the half CP cycle, we equate an I_D value from Fig. 5 or Fig. 6 to an equivalent I_D value on the trapping-free I_D–V_G curve of Fig. 7. Then, we extract the V_G necessary to produce this current; this V_G value is the $V_{G,\mathrm{eff}}$ experienced by the channel at some particular time during the CP cycle and allows us to simply determine the actual Fermi-level position for a given $V_{G,\mathrm{set}}$. One question remains, however; at what time during the CP cycle do we extract $V_{G,\mathrm{eff}}$?

Consider first the ideal V_G pulse train of Fig. 13 for the case of performing CP on a production-quality Si/SiO_2 device with negligible bulk traps ($V_{G,\mathrm{set}} = V_{G,\mathrm{eff}}$). Interface defects start to fill with electrons when the device is pulsed into inversion (n-channel MOSFET). At strong inversion, this occurs very quickly, and by the end of the V_{GH} pulse, all interface defects up to the Fermi-level position set by V_{GH} are filled. When quickly pulsed into accumulation, holes flood in and recombine with the interface trapped electrons which reside above the new Fermi-level position defined by V_{GL} (only defects whose energies lie between the Fermi-level positions defined by V_{GH} and V_{GL}, ΔE, are permitted to participate). The process continues when the device is quickly pulsed back into inversion, resulting in a net I_{CP}.

We know from the previous section that $V_{G,\mathrm{set}}$ does not equal $V_{G,\mathrm{eff}}$; $V_{G,\mathrm{eff}}$ is continuously changing with time, resulting in a V_G pulse that looks more like the second schematic diagram of Fig. 13. As far as CP is concerned, only the Fermi level at the end of the inversion half cycle counts. When pulsed into accumulation, the Fermi-level shift will be driven by the full applied ΔV_G at first. As holes are flooding in and recombining with interface trapped electrons, the effective V_G is changing

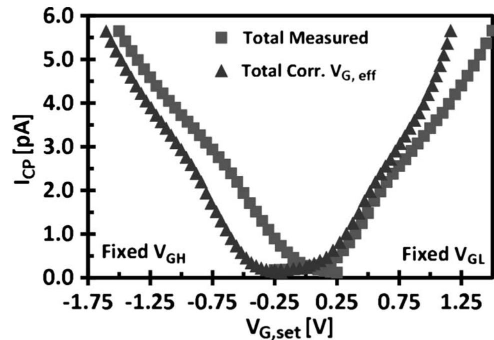

Fig. 14. Measured I_{CP} versus V_G compared to I_{CP} after accounting for the effective V_G variations.

due to charge detrapping from bulk defects, leading to a Fermi level that is shifting back up. This will result in an effectively smaller allowed bandgap energy recombination window (ΔE). Thus, only the traps within the allowed smaller energy window, determined at the end of the V_{GH} pulse and the end of the V_{GL} pulse, contribute to I_{CP}. Using Figs. 5–7 and the aforementioned procedure, we obtained the curve shown in Fig. 14 which quantifies the variations in V_G.

IV. Conclusion

Using two independent methods, we have found that the total amount of trapping/detrapping that occurs (measured with ultrafast I_D–V_G) is significantly larger than the amount of trapping/detrapping that is actually converted into I_{CP}. Consideration of source/drain depletion overlaps as well as minority-carrier lifetimes provides a reasonable explanation for the low conversion efficiency. Using a long-channel device can improve the percentage of detrapped charges entering the substrate as minority carriers. However, the efficiency of converting them into I_{CP} will remain low due to the long minority-carrier lifetime compared to the half-cycle CP frequency. The way to increase the conversion efficiency is to use long-channel devices with short minority-carrier lifetimes (for example, defect-rich silicon carbide substrates). For the devices in our study, the minority-carrier lifetime is much longer than the bulk charge detrapping time and the CP half cycle, leading to a complex dynamic. Coupled with extremely low conversion efficiency, there is not much hope of recovering the defect depth profile using the FD-CP method.

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Jason T. Ryan (S'04–M'10) received the Ph.D. degree from The Pennsylvania State University, University Park, in 2010.

Since 2010, he has been with the National Institute of Standards and Technology, Gaithersburg, MD.

Richard G. Southwick, III (S'04–M'11) received the Ph.D. degree from Boise State University, Boise, ID, in 2010.

He is currently with the National Institute of Standards and Technology, Gaithersburg, MD.

Jason P. Campbell (M'07) received the Ph.D. degree from The Pennsylvania State University, University Park, in 2007.

Since 2007, he has been with the National Institute of Standards and Technology, Gaithersburg, MD.

Kin P. Cheung (SM'02) received the Ph.D. degree from New York University, New York, in 1983.

He is currently a Project Leader with the National Institute of Standards and Technology, Gaithersburg, MD.

John S. Suehle (F'12) received the Ph.D. degree from the University of Maryland, College Park, in 1988.

Since 1982, he has been with the National Institute of Standards and Technology, Gaithersburg, MD.