

Measurement Science for “More-Than-Moore” Technology Reliability Assessments

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In this paper, we will present an overview of metrology issues and some of the techniques currently under development in our group at NIST, aimed at understanding some of the potential performance limiting issues in such highly integrated systems. We will discuss our attempts to identify and characterize the various types of defects and relate them to where and why they form, without interrupting the responsible phenomena.

I Introduction

Traditionally, the semiconductor industry has obtained incremental value in time by geometric scaling (i.e., shrinking physical dimensions), and occasionally introducing new materials. These tweaks used to be sufficient for improving computation performance (through faster clock frequencies, and memory capacity). As CMOS devices reach their fundamental physical limits, the aggressive scaling characteristic of the Moore's law will no longer be sufficient for the desired performance improvements. This realization has led to the paradigm of functional diversification (also known as More-Than-Moore), to attain the equivalent performance that would otherwise have been attainable by scaling (equivalent scaling).

The More-Than-Moore approach allows for non-digital functionalities to be integrated with digital systems on the same chip or package. As envisioned, integrated systems of the future will perform diverse functions, such as high-accuracy sensing of real-time signals, energy harvesting, and on-chip chemical/biological testing, etc., in addition to high-performance computation, high-density storage and high-bandwidth communication. These emerging hybrid devices involve the design and integration of multiple device technologies and diverse components in a single heterogeneous system that is high-performance, energy-efficient and reliable [1]. Enabling such diverse functionality with the prerequisite attributes in a single system requires a radical shift in the principles of system design and integration. These new approaches to increased performance also require new materials and integration schemes, with higher interconnect densities and increase thermal loads, etc. Furthermore, new packaging technologies are required when diverse devices such as bio-chips, integrated optics, embedded active and passive devices, MEMS, printable circuits (semiconductor, light emitter, RF, etc.) are integrated into a monolithic device.

Such heterogeneously integrated systems are becoming ubiquitous; Articles of trade based on heterogeneously integrated schemes are rapidly being introduced into commerce, e.g., 3D integrated MEMS and CMOS image sensors (from STMicroelectronics), silicon wafer level packaging of HB-LED modules are commercially available. They are currently common in the application fields of automotive and aerospace, health, and security. These mission critical applications require an extremely high level of reliability. As with most nano-systems, the nanoelectronic components of these heterogeneously integrated systems are characterized by large surface-to-volume ratios, with most of the materials of construction located at interfaces. Given that the behavioral properties of interfacial materials are both qualitatively and quantitatively different from those in the bulk, it is expected that the performance-limiting phenomena in nanoelectronic systems will be quite different from those in microelectronics systems. This situation is further complicated by the introduction of new materials and integration schemes in the fabrication of such nanoelectronic systems.

Our primary objective is to identify measurement techniques tools and methodologies to improve the reliability of complex heterogeneously integrated devices. We systematically investigate the new failure mechanisms in such devices, in the hope of developing low energy and time efficient methods for effective detection and screening of lifetime limiting defects. The specific topical areas of interests include mechanical properties of interfaces, electromagnetic compatibility, signal integrity, modeling of reliability effects. The fundamental assumption of our work is that it is probable that the traditional models and techniques for studying reliability in integrated circuits may not be appropriate for nanoelectronics and nanosystems. For example, electromigration in interconnects has been extensively studied and used to predict interconnect life expectancy. In the interest of time, high current densities (on the order of MA/cm²) and temperatures (in the 100⁰C to 300⁰C range) are normally used in stress interconnects to project performance life expectations. Unfortunately, these conditions are so far removed from the typical normal operating conditions of most nanoelectronic devices that the results obtained, and predictions based on them, are almost certainly irrelevant to normal use conditions. Also, the conventional techniques are frequently inadequate in detecting the early onset of failures. Furthermore, the activation energy extracted from the temperature dependence of lifetimes under these “extreme” stress conditions may not be relevant to the actual kinetics of the underlying phenomena responsible for the observed electromigration failures.

In our current work, we believe that with judicious selection and control of the experimental stress conditions, cross correlation with other techniques and application of nontraditional reliability metrology techniques it should be possible to resolve many of the problems that limit the metrological value the traditional techniques.

In this paper, we present an overview of a number metrology issues and some of the new techniques and models currently under development in our group at NIST aimed at addressing these issues. We have used a case study of the evolution of silicon oxide isolated silicon filled TSV interconnects to illustrate and discuss our attempts to identify and characterize types of performance-limiting defects in three-dimensional (3-D) nanoelectronic devices, with special focus on 3-D interconnects, and relate the defects to where and why they form. In this illustration, we deploy a number of complimentary non-destructive tools and techniques for identifying such performance-limiting defects, without interfering the responsible mechanistic phenomena.

II Experimental Results and Discussion

In experiments described in this paper, microwave / radio-frequency (RF) radiation was used to study the evolution of nano-electronic device performance under stress. In these studies, frequencies up to 20 GHz were used to probe devices, at ambient temperatures and after stress. By inspection of the scattering parameters (S-parameters), one can obtain qualitative assessments of device design, integration and material chemistry evolution issues. With modeling, one can also quantitatively extract changes in the electrical characteristics of the devices with stress. We have shown elsewhere that RF reflectance losses (S_{11} parameter) are sensitive to changes in device structure long before such changes are detectable by any microscopy technique, including AFM [2]. Figure 1, shows the changes in broadband radio-frequency signal transmission loss in a low resistivity silicon substrate of a silicon-filled through-silicon via (TSV) test structure, as a function of thermal-stress cycling. The samples were repeatedly cycled between 30⁰C and 150⁰C in ambient air. The signal insertions loss increased with increasing number of cycles, indicating heat-induced changes in test structure.

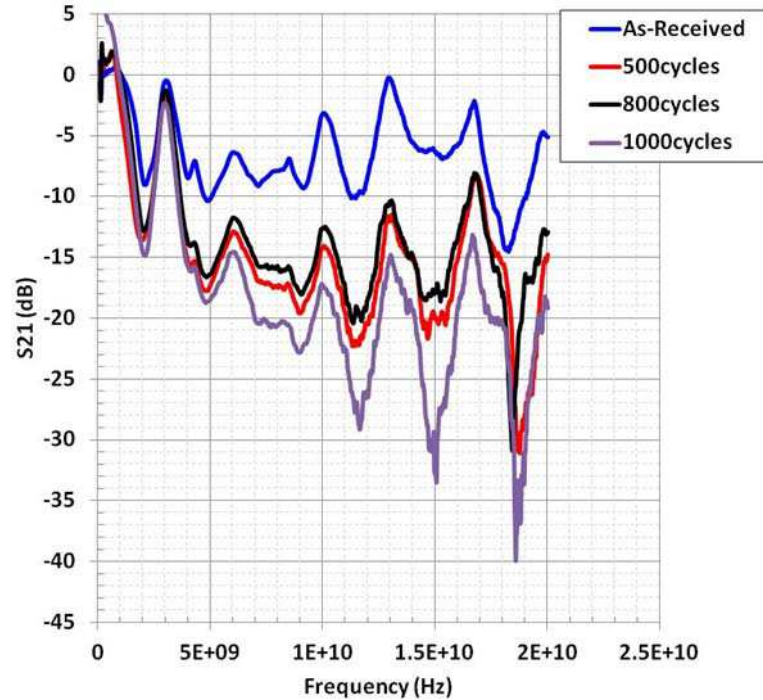


Figure 1: Changes in broadband radio-frequency signals insertion loss in a silicon-filled TSV test structure, as a function of thermal-stress cycling.

The observed changes with thermal cycling were extensively investigated with a battery of techniques. The topographical changes in the test structures were evaluated by AFM. Figure 2 shows the AFM images of the test structure after varying number of thermal cycles. Before thermal cycling (Figure 2a), it can be observed from the AFM image that the oxide (SiO_x) isolation liner appears uniform without any voids and grooves. However, after 1000 thermal cycles (Figure 2b), a very visible seam was observed at the center of the SiO_x isolation liner. The seam appears to grow with further thermal cycling and after 1600 thermal cycles (Figure 2c) additional visible voids were observed around the seam location. The changes in the seam dimensions and profile with thermal cycling were measured by AFM, and summarized in Figure 3. From this graph it is found that the void area increased with increasing number of thermal cycles. This is consistent with Lei Shan et al. who have shown that voids/holes results in signal losses which scale with the size of the voids/holes. In addition, the increased losses with thermal cycling can be caused by compositional changes in the SiO_x isolation liner [3].

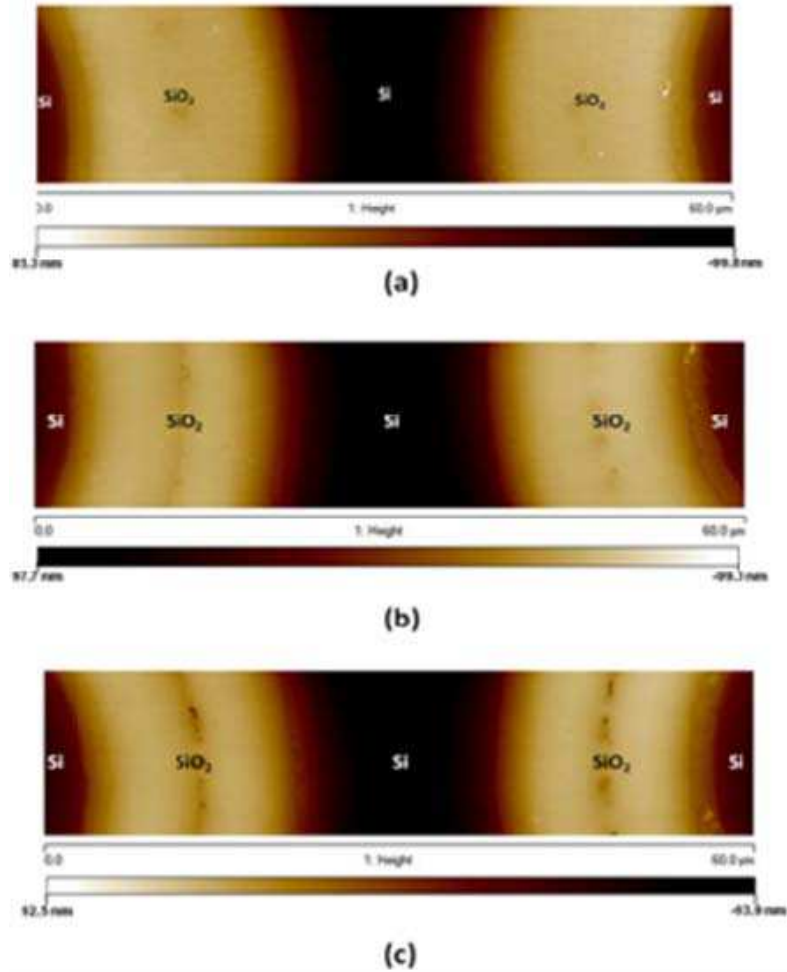


Figure 2: AFM topography image showing the morphological evolution of the SiO_x isolation liner with thermal cycling. (a) As-received state (b) after 1000 thermal cycles (c) after 1600 thermal cycles

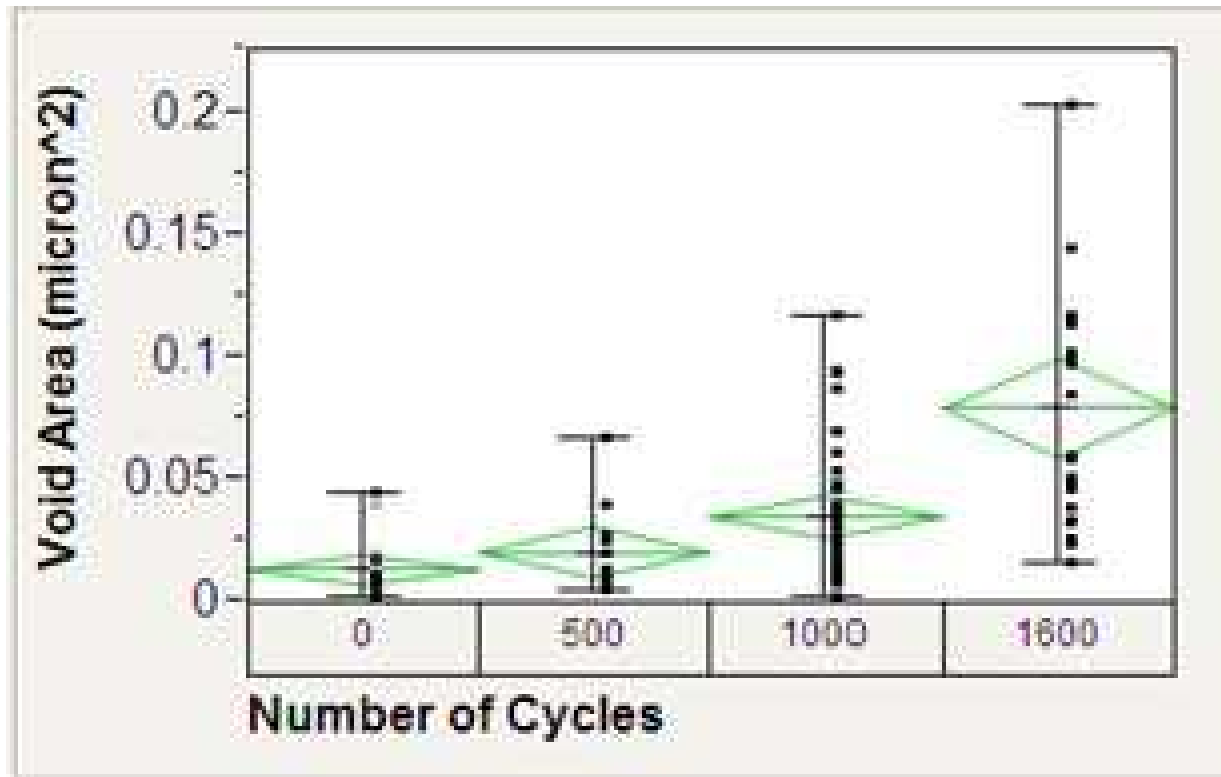


Figure 3: Plot of the void area in SiO_x isolation layer as a function of the number of thermal cycles.

To further understand the changes in the liner oxide, we used a variety of scanning probe techniques to measure the changes in the electrical properties of the isolation around the Si-TSVs. There are a variety of techniques that can measure the localized capacitance between a Scanning Probe Microscope (SPM) tip and a sample. Some of these techniques include intermittent contact scanning capacitance (IC-SCM), scanning microwave microscopy (SMWM) and various implementations of scanning Kelvin force (SKFM) and Kelvin probe microscopy. Figure 4 is a profile scan that compares the evolution of surface potentials on the oxide liner as a function of thermal cycles (on the same samples used for the AFM data in Figure 2). Figure 5 shows a detailed surface potential image for the three different test conditions. These measurements were made with scanning Kelvin force microscopy (SKFM). A shortcoming of these techniques is that they provide qualitative, rather than quantitative, capacitance measurements. Thus, the data in Figure 4 and Figure 5 clearly show the evolution in the electrical characteristics of the liner oxide with thermal cycling in open laboratory ambient. From figure 5C, it appears the liner is comprised of multiple layers of oxide with possible different composition or residual trapped charge.

The forces detectable by the scanning probes can be classified into three main categories: (1) Coulomb forces which have electrostatic origin and covers forces arising from the interaction between charges, permanent dipoles and higher order moments. (2) Polarization forces which

cause dipole moments in atoms or molecules, which are induced by electric fields of charges and of permanent or induced dipoles. (3) Bonding forces, which have a quantum mechanical nature and lead to charge transfer processes as involved in covalent bonding [5]. Furthermore magnetic forces, friction forces, capillary forces, etc. can, in principle occur in scanning probe measurements. By detecting electrostatic forces, contact potentials can be determined in the SKFM mode. In a normal capacitor, the contact potential (CP) results from the alignment of the Fermi levels of tip and sample having different work functions. However, the samples evaluated in this work do not fit the capacitor model; thus, the observed surface potential observed in Figure 4 could be due to either polarization or bonding forces. In order to further understand the changing surface potential with thermal cycling, further analysis will be needed. We plan to use surface FTIR (in the ATR mode) to measure the concentration of bridging Si-O-Si at the approximate center of the liner rings, as a function of temperature and number of cycles.

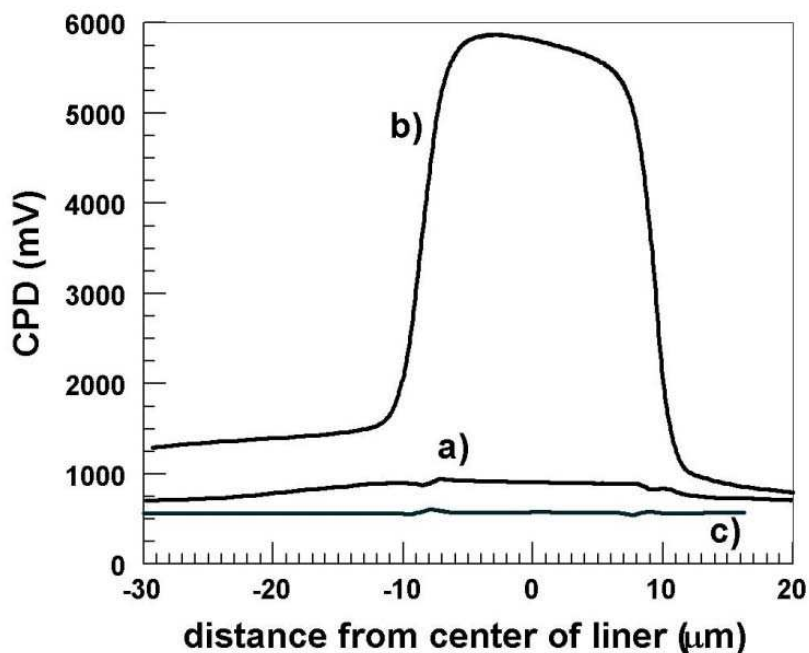
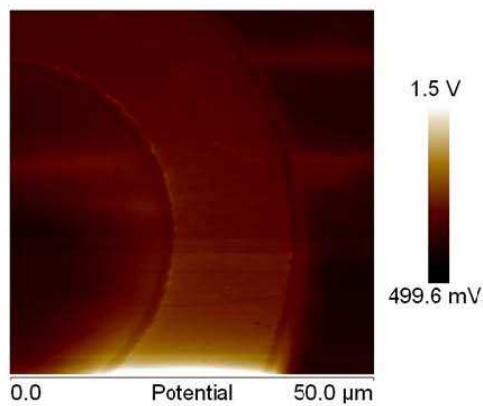
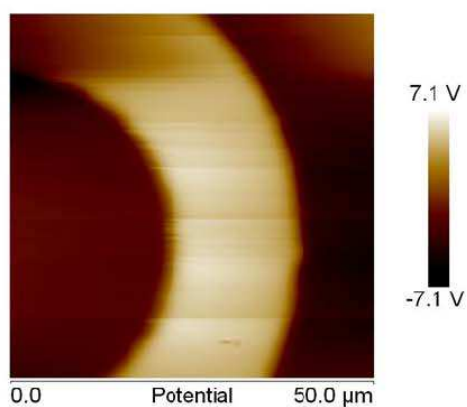


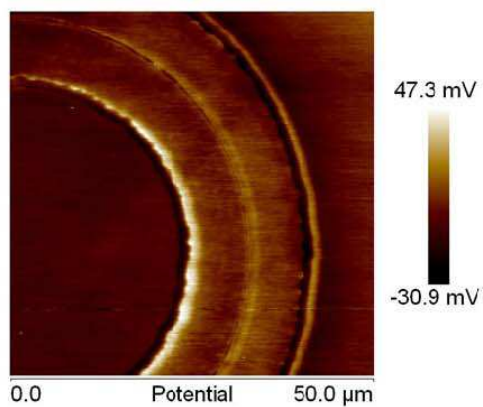
Figure 4: Line scans of surface potential measured with SKFM across the TSV and SiO_x liner showing the evolution of the SiO_x isolation liner with thermal cycling. (a) As-received state (b) after 1000 thermal cycles (c) after 1600 thermal cycles.



(a)



(b)



(c)

Figure 5: SKF images showing the surface potentials evolution of the SiO_x isolation liner with thermal cycling. (a) As-received state (b) after 1000 thermal cycles (c) after 1600 thermal cycles

III Summary

In summary, we are working on various measurement techniques to study, understand and model potential performance limiting phenomena in heterogeneously integrated nanoelectronic systems. The work so far has demonstrated the utility of radio-frequency probes in monitoring systems with large surface to bulk ratios. Kelvin Force probe measurements, although largely qualitative, have also been demonstrated to detect changes in dielectric films in integrated systems.

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