Electro-Thermal Simulation and Design of a 60 A, 4.5 kV Half-Bridge Si IGBT/SiC JBS Hybrid Power Module*

Tam H. Duong, Allen R. Hefner
National Institute of Standards and Technology
Gaithersburg, MD 20899 USA

Karl D. Hobart
Naval Research Laboratory
Washington, D.C. 20375 USA

***Abstract*—This paper presents the results from a parametric simulation study that was conducted to optimize the design of a high-current 4.5 kV half-bridge Si-IGBT/SiC-JBS hybrid module for medium voltage hard-switched power conversion as well as to compare the performance of the hybrid module to the all-Si configuration. The simulations are performed for a circuit that emulates hard-switched conditions similar to a full wave inverter and utilizes validated electro-thermal models for the 4.5 kV Si IGBT, Si PiN diode, and SiC JBS diode and a validated thermal model for the module package. Simulations for various circuit and module parameters including the size and number of SiC JBS diode chips, gate resistances and switching frequencies are used to design the module to be used for demonstration in a Naval power converter application.**

Keywords: Silicon carbide (SiC); medium-voltage; Junction Barrier Schottky (JBS); hybrid half-bridge module; power systems.

I. INTRODUCTION

Medium-voltage (4.5 kV– 6.5 kV) IGBT modules have many applications ranging from medium-voltage and high-power motor drives to HVDC and flexible AC transmission system (FACTS) converters. The anti-parallel diodes in these modules are the major limiting factor in performance due to losses and current stress that result from their poor reverse recovery characteristics. This has become a critical problem for Naval applications which require medium voltage power systems to be built on relatively small platforms due to the large increase in electrical power demanded by e.g., hybrid- or all-electric propulsion, high power radar and new weapons systems. The 4.5 kV SiC JBS diodes developed in [1, 2] and the 4.5 kV Si-IGBT/SiC-JBS hybrid modules being developed in this work are motivated by this critical need. It is expected that the use of these hybrid modules for the Naval platform will enable reduced size, weight, and cooling requirements and will result in improved operational capabilities and significant fuel savings.

The purpose of this paper is to perform a parametric simulation study to optimize the design of a high-current 4.5 kV half-bridge Si-IGBT/SiC-JBS hybrid module for medium voltage hard-switched power conversion as well as to compare the performance of the hybrid module to the all-Si configuration. The simulations are performed for a circuit that emulates hard-switched conditions similar to a full wave inverter and utilizes validated electro-thermal models for the 4.5 kV Si IGBT, Si PiN diode, and SiC JBS diode and a validated thermal model for the module package. Simulations for various circuit and module parameters including the size and number of SiC JBS diode chips, gate resistances and switching frequencies are used to design the module to be used for demonstration in a Naval power converter application.

II. ELECTRO-THERMAL SIMULATION METHODOLOGY

Fig. 1(a) is a schematic of the circuit used for the electro-thermal simulations and Fig. 1(b) is the topology of the 60 A, 4.5 kV Si IGBT/SiC JBS half-bridge power module electro-thermal model. To mimic the device voltage, current and heating stress conditions of a full wave PWM inverter in a circuit that enables rapid simulation, the boost converter shown in Fig. 1(a) is chosen to operate with a 50% duty cycle with a one-quarter 50 Hz sine-wave on and one-quarter off where the circuit response time is chosen so that the current rises similar to that of the 50 Hz sine-wave. In the half-bridge power module model, the junction temperature node of each power semiconductor device is connected directly to the thermal node Junction of the chip thermal model connected between nodes Junction and Header; while the module package is connected between nodes Header and Spreader. The Spreader is connected directly to the Tnode (ambient temperature) for the simulations in this work but could alternatively be connected to a heatsink or cooling system thermal model.

* Contribution of NIST, not subject to copyright. The devices discussed in this paper provided by NRL. NIST does not recommend or endorse the devices as the best available for the purpose.

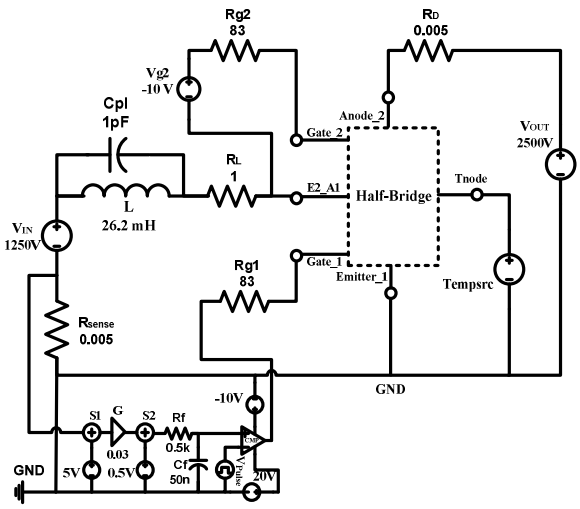

Fig. 1(a): The basic 2500 V boost converter used for the 60 A, 4.5 kV half-bridge Si IGBT/SiC JBS power module simulation.

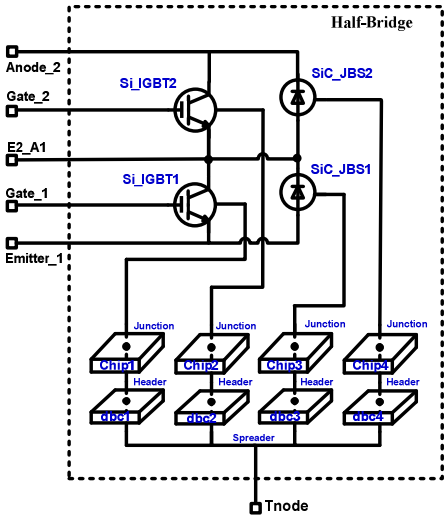

Fig. 1(b): Circuit topology of the 60 A, 4.5 kV half-bridge Si IGBT/SiC JBS power module.

III. Model Development and Validation

A. Model Development

The 60 A, 4.5 kV half-bridge Si IGBT/SiC JBS power module in the schematic Fig. 1(b) is modeled using the previously developed models for Si IGBTs in [3], for Si PiN and SiC JBS diodes in [4], and for the module package in [5], where model parameters for the specific components were extracted using recently developed parameter extraction tools.

B. Model Validation

Model validation results are shown in Figs. 2-7 for the 4.5 kV SiC JBS and Si PiN diode models, and in Figs. 8-11 for the 4.5 kV Si IGBT model.

Figs. 2 and 3 show I-V characteristics of the 4.5 kV, 60 A SiC JBS and Si PiN diodes at three different temperatures of 25 °C, 75 °C, and 125 °C, respectively. The results indicate that the SiC JBS diode begins to conduct at approximately 1.2 V as determined by the Schottky barrier height, versus 0.6 V for the Si PiN diode as determined by the built-in potential of the P-i-N junction. The results also indicate that both devices have similar performance; however the SiC JBS has a positive temperature coefficient resulting in a better current sharing for paralleled SiC diodes.

Figs. 4 and 5 show the capacitance-voltage characteristics for 4.5 kV, 60 A SiC JBS and Si PiN diodes at 25 °C, respectively. The results indicate that the junction capacitance of the SiC JBS diode is approximately eight times larger than that same current-rated Si PiN diode. Although the capacitance is larger, it still produces far less reverse recovery charge than the Si PiN, as shown below, and the capacitance is better behaved in that there is no possibility of an abrupt (snappy) change in capacitance as there is with the PiN diode under certain conditions.

Figs. 6 and 7 show the reverse recovery characteristics for the 4.5 kV, 60 A SiC JBS and Si PiN diodes with the forward current of 30 A, switching voltage of 2.25 kV at three different values of reverse di/dt (40 A/µs, 80 A/µs, and 170 A/µs) at 25 °C, and with a low external driver capacitance.

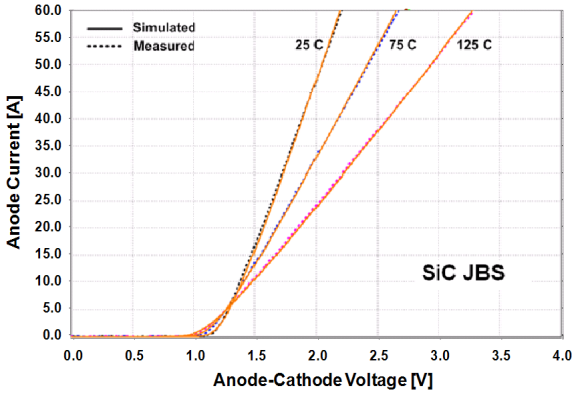

Fig. 2: Comparison of measured (dashed) and simulated (solid) forward conduction characteristics at 25 °C, 75 °C, and 125 °C for a 4.5 kV, 60 A SiC JBS diode.

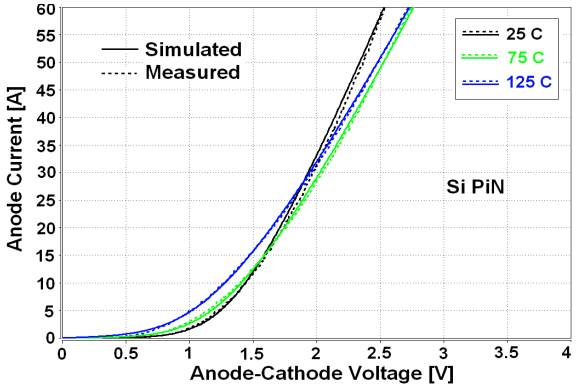

Fig. 3: Measured (dashed) and simulated (solid) forward characteristics for a 4.5 kV, 60 A Si PiN diode.

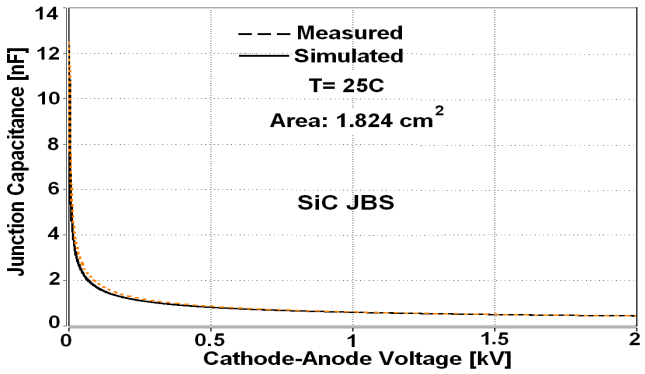

Fig. 4: Measured (dashed) and simulated (solid) junction capacitance for a 4.5 kV, 60 A SiC JBS diode at 25 °C.

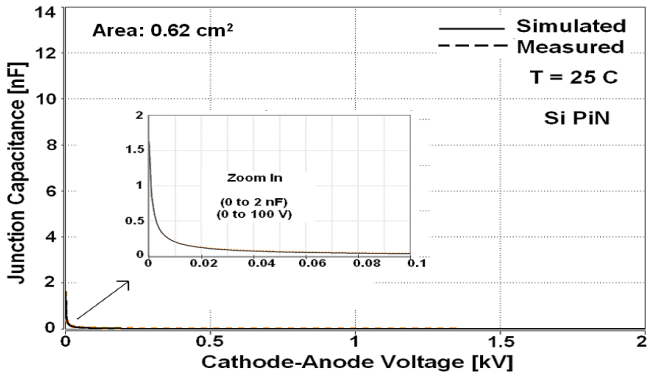

Fig. 5: Measured (dashed) and simulated (solid) junction capacitance for a 4.5 kV, 60 A Si PiN diode at 25 °C.

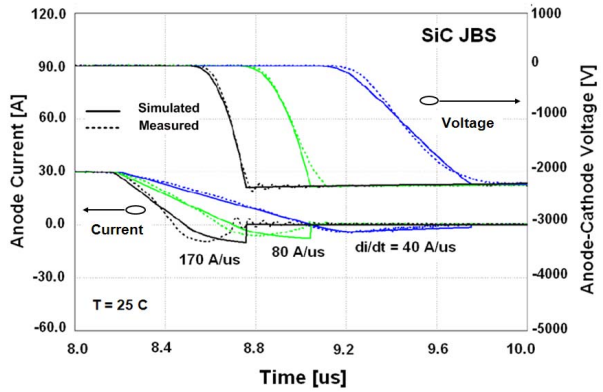

Fig. 6: Comparison of measured (dashed) and simulated (solid) reverse recovery characteristics for a 4.5 kV, 60 A SiC JBS diode at 25 °C.

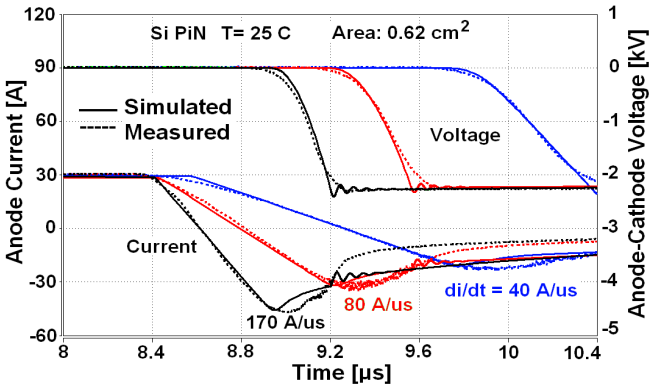

Fig. 7: Measured (dashed) and simulated (solid) reverse recovery at different dI/dt for a 4.5 kV, 60 A Si PiN diode at 25 °C.

Figs. 8 and 9 show the 4.5 kV, 60 A Si IGBT model (solid) compared with measured (dashed) results of output characteristics at 25 °C and 125 °C, respectively. Fig. 10 shows the simulated and measured clamped inductive load turn-off gate-emitter voltage (top) and IGBT collector current and collector-emitter voltage (bottom) waveforms for different clamped voltages (e.g. 1 kV, 2 kV, and 3 kV), switching current of 30 A, gate resistor of 50 Ω, and IGBT temperature of 25 °C. Fig. 11 shows the 4.5 kV, 60 A Si IGBT simulated and measured clamped inductive load turn-off gate-emitter voltage (top) and IGBT collector current and collector-emitter voltage (bottom) waveforms of for different gate resistors (e.g. 25 Ω and 50 Ω), a switching current of 30 A, clamp voltage of 2.5 kV, and IGBT temperature of 25 °C.

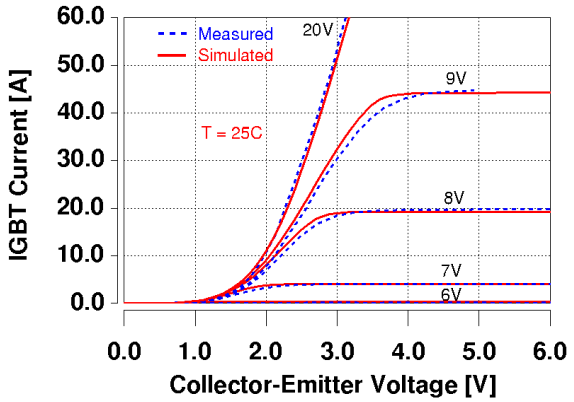

Fig. 8: Measured (dashed) and simulated (solid) output characteristics at 25 °C (a) for a 4.5 kV, 60 A Si IGBT.

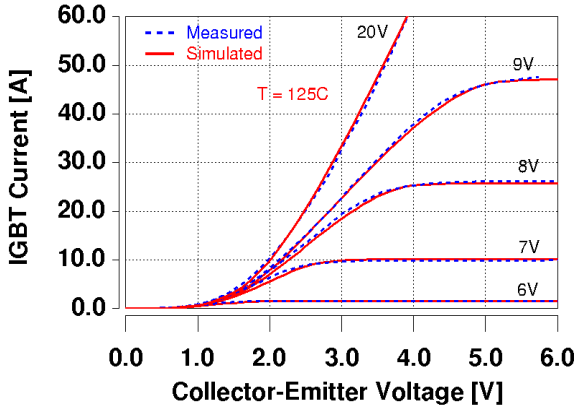

Fig. 9: Measured (dashed) and simulated (solid) output characteristics at 125 °C (a) for a 4.5 kV, 60 A Si IGBT.

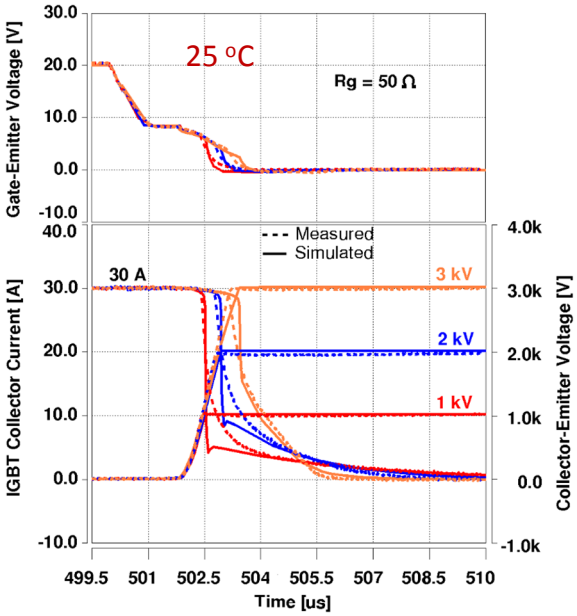

Fig. 10: Clamped voltage dependence of 4.5 kV, 60 A Si IGBT inductive load turn-off measured (dashed) and simulated (solid) switching waveforms at gate resistor of 50 Ω, switching current of 30 A, and at 25 ºC.

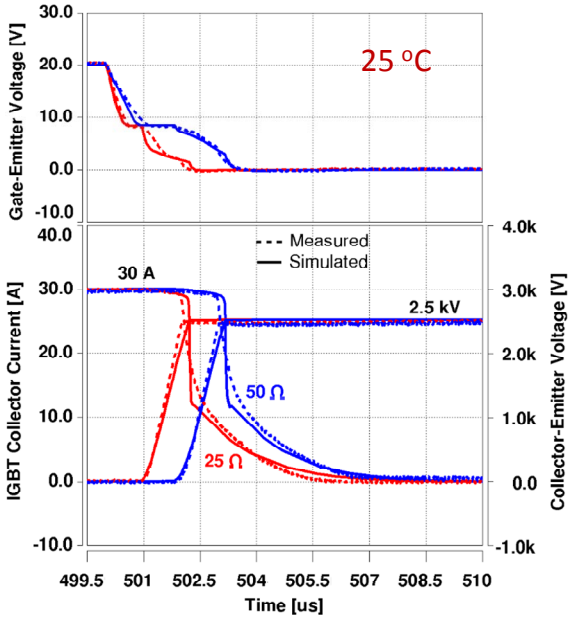

Fig. 11: Gate resistor dependence of 4.5 kV, 60 A Si IGBT inductive load turn-off measured (dashed) and simulated (solid) switching waveforms at clamped voltage of 2.5 kV, switching current of 30 A, and at 25 ºC.

IV. Electro-Thermal Analysis of The Half-Bridge SiC MOSFET/JBS Power Module

To avoid running the full electro-thermal simulation for the time required to reach steady-state temperature, a temperature initial condition iteration strategy similar to that defined in [6] is used. This is accomplished using a thermal power source at the thermal terminal of each semiconductor device to set the initial temperature distributions. These initial power source values are iterated until the average dissipated power for each semiconductor device obtained at the end of several 50 Hz cycles of a full electro-thermal simulation matches the initial conditions.

A. Electrical Operation and Thermal Response

As an example, Fig. 12 shows the temperature waveforms at the chip surface TJ (Junction) and chip-package TH (Header) for (a) Si_IGBT1 and (b) SiC_JBS2 as shown in Fig. 1(b) for a full electro-thermal simulation of the circuit in Fig. 1(a) with switching frequency of 1 kHz, gate resistances of 20.75 Ω, ambient temperature of 25 °C, and JBS diode area of 0.456 cm^2. Notice that the chip surface-temperature waveform of Si_IGBT1 spikes at a 1 kHz rate during the 50 Hz quarter sine-wave phase that the device is switching (e.g., 0 ms to 5 ms) due to the switching energy losses in the Si IGBT that results from charging the capacitance of the other devices in the module at turn on and due to the tail current losses during turn off. Also, notice that the junction temperatures of both the Si_IGBT1 and SiC_JBS2 are cooling after the peak in inductor current (5 ms) and during the phase in which the device is off (e.g., 5 ms to10 ms).

From the temperature waveforms of Fig. 12 (a), it is evident that the thermal response of the Chip1 determines the Si IGBT temperature variations during the device 1 kHz switching cycle (from 60 °C to 73 °C) because the temperature at the package header TH does not change during the 1-kHz cycle. The thermal response of the Chip1 and module package (dbc1) determines the device temperature variations during the 50 Hz sinusoidal current variations (from 46 °C to 73 °C) because the temperature at the package case (Spreader or Tnode in Fig. 1(b)) does not change.

Fig. 13 shows the simulated temperature waveforms at TJ and TH for Si_IGBT1 and SiC_JBS2 during the start-up of the converter shown in Fig. 1(a). For the start-up simulation, the initial condition for the temperature throughout the thermal network is 25 °C. The Chip1 and module package (dbc1) temperature waveforms asymptotically approach the same steady state values of temperature obtained in the iteration method of Fig. 12 after about 500 ms.

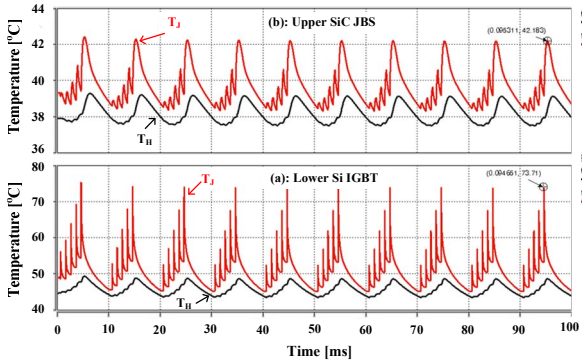

Fig. 12: Temperature waveforms at the *Chip1* surface T_J (*Junction*) and chip-package interface T_H (*Header*) for the lower Si-IGBT and the upper SiC-JBS diode as shown in Fig. 1(b).

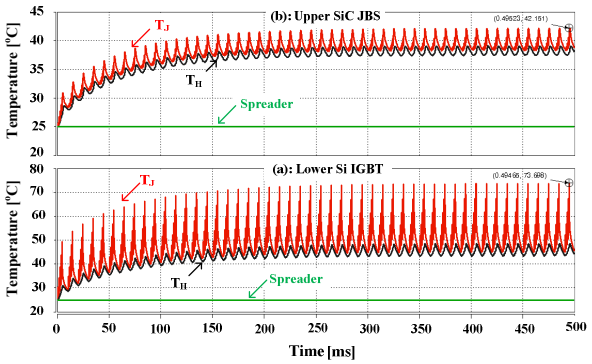

Fig. 13: Simulated thermal response at startup for the average power dissipated in the Si_IGBT1 (a) and SiC_JBS2 (b) indicating the temperature at the junction (T_J) and chip-package interface (T_H).

B. Power Dissipation and Switching Energy of Si IGBTs and SiC JBS/Si PiN Diodes

Fig. 14 shows simulated waveforms of the (a) collector-to-emitter voltage (V_{CE}), (b) collector current (I_C), (c) instantaneous dissipated power (P_{INS}), and (d) cumulative dissipated energy (E_{CUM}) for the active lower Si IGBT during two 1 kHz switching cycles of the simulation in Fig. 12 (i.e., the time interval between 92.25 ms to 94.25 ms). The instantaneous power dissipated as heat (provided at the thermal node) is not equal to the product of terminal current and voltage waveforms because the internal capacitance currents do not produce heat. Fig. 14 was chosen so that the details of both the turn-on and turn-off waveforms are viewed on the same graph.

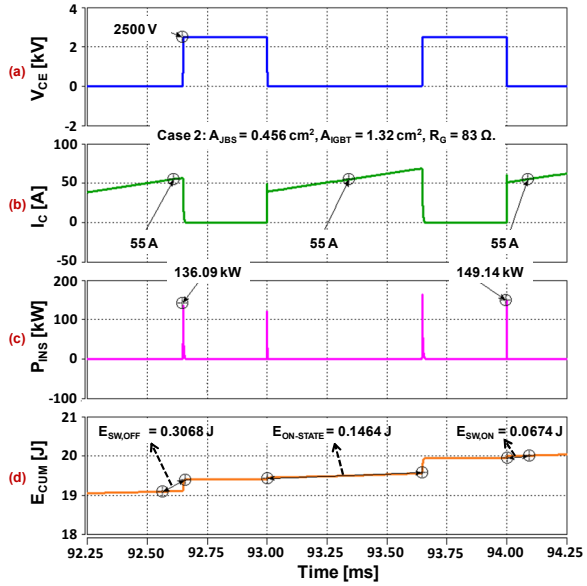

Fig. 14: Two switching cycles from the 1 kHz simulation (a) collector-to-emitter voltage (V_{CE}), (b) collector current (I_C), (c) instantaneous dissipated power (P_{INS}), and (d) cumulative dissipated energy (E_{CUM}) for the active lower Si IGBT (Si_IGBT1) in the 60 A, 4.5 kV half-bridge Si IGBT/SiC JBS power module previously shown in Fig. 1(b).

Before Si_IGBT1 is turned on, the inductor current is flowing through SiC_JBS2. When Si_IGBT1 is switched on (t = 94 ms shown in Fig. 14), the inductor current is transferred from SiC_JBS2 to Si_IGBT1. In addition to the inductor current, Si_IGBT1 also conducts capacitive currents resulting from charging the output capacitances of the other Si IGBTs and JBS diodes within the module. This results in a collector current spike at turn-on (see Fig. 14(b)) that is larger than the on-state current (55 A) and results in a turn-on switching energy indicated in Fig. 14(d) of $E_{SW,ON}$ = 67.4 mJ/cycle. Note that the current spike is a lot higher in the case of Si PiN.

During the reverse recovery of diode SiC_JBS2, the collector-emitter voltage of Si_IGBT1 drops and approaches the Si IGBT on-state voltage. Once the IGBT is fully on, the instantaneous power dissipation is determined by the product of the on-state voltage and drain current. During this on-state phase of the switching cycle (e.g., the time interval between 93 ms to 93.65 ms), the instantaneous power dissipation is small compared to the value of the power spikes during switching events, but the time duration of the on-state phase of the switching cycle is much longer than the switching times. Therefore, the energy-loss waveform rises with a constant slope (determined by the inductor current and the Si IGBT on-state voltage) during the on-state phase of the switching cycle.

When the gate of Si_IGBT1 is turned off (t = 92.65 ms in Fig. 14), V_{CE} rises to maintain the constant current in the load inductor. During the voltage rise, the load current charges the output capacitances of all of the devices within the module. Once V_{CE} reaches the supply voltage of 2500 V, the collector-emitter voltage is clamped at the supply voltage by the anti-parallel diode on Si_IGBT2. Because the IGBT channel is turned off slowly before the voltage begins to rise, the turn-off switching energy indicated in Fig. 14(d) ($E_{SW,OFF}$ = 306.8 mJ) is larger by more than a factor of 4 than the turn-on switching energy.

V. Results of Module Optimization Parametric Study

Table 1 summarizes the results of the parametric module parameter simulation study performed to optimize the module and circuit parameters for best performance in medium voltage hard-switched Naval power conversion. The table shows the total dissipated power (P), and the individual Si IGBT and SiC-JBS/Si-PiN diode dissipated powers (P_{IGBT} and $P_{JBS/PiN}$). The components of loss are also indicated for each device; that is, on-state loss ($E_{ON-STATE}$ for Si IGBT and E_{COND} for SiC-JBS/Si-PiN diode), turn-on loss ($E_{SW,ON}$), and turn-off loss ($E_{SW,OFF}$). Finally, the peak temperatures ($T_{PEAK,\ IGBT}$ for Si IGBT and $T_{PEAK,JBS/PiN}$ for SiC-JBS/Si-PiN diode) are given for each device. Each case in the table is for a different set of module parameters; that is, the total diode chip areas (A_{IGBT} for Si IGBT and $A_{JBS/PiN}$ for SiC-JBS/Si-PiN diode), gate resistance (R_G), and switching frequency (f_{SW}).

The results in Table 1 indicate that the performance of the 4.5 kV half-bridge Si-IGBT/SiC-JBS hybrid module can

be optimized for thermal performance by varying power module parameters such as the number of SiC JBS diode chips (JBS area) and that the SiC JBS diode results in lower losses and cooler temperatures for both the diode and IGBT.

Fig. 15 shows the comparisons of IGBT turn-on current spike waveforms for both SiC JBS (e.g, Case 2, 4, and 6) and Si PiN (e.g. Case 7) as anti-parallel diodes. It indicates that the turn-on current spike in the IGBT is also reduced substantially by using the SiC JBS diode, enabling the use of a lower gate resistance and higher switching frequency. Fig. 16 shows the IGBT turn-on current spike at different values of gate resistor and SiC JBS die area. Fig. 16 depicts that at the same value of the gate resistor, the larger the SiC JBS die area, the larger is the turn-on current spike in the IGBT. Fig. 16 also indicates that for the same SiC JBS die area, the smaller the value of the gate resistor, the larger is the turn-on current spike in the IGBT. Fig. 17 shows the junction temperature waveforms for the lower Si IGBT (a) and the upper SiC JBS (b) for Case 1 at three different switching frequencies (i.e., 1 kHz, 2 kHz, and 3 kHz). The results indicate that the junction temperature of the Si IGBT increase with frequency while it almost remains the same for SiC JBS. Note that the junction temperature waveform of the Si IGBT is not stable at 3 kHz due to thermal runaway.

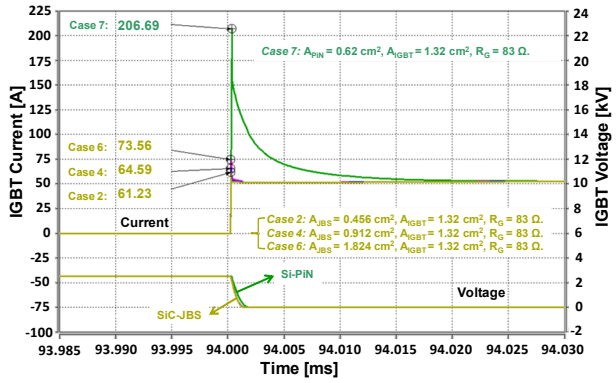

Fig. 15: Simulated turn-on current spike waveforms for the Si_IGBT1 at R_G=20.75 Ω (e.g. Cases 1, 3, and 5) and at R_G=83 Ω (e.g. Case 2, 4, and 6).

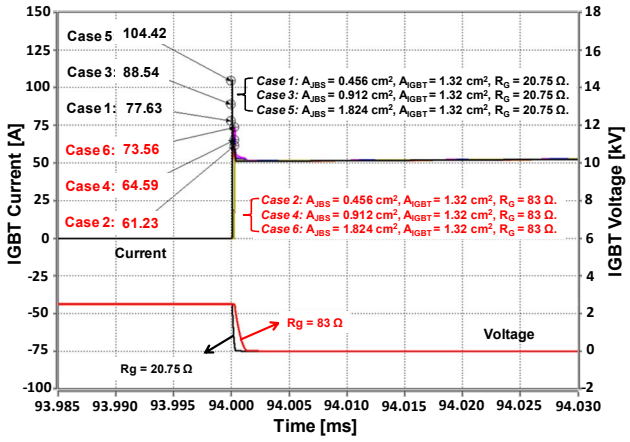

Fig. 16: Simulated turn-on current spike waveforms for the Si_IGBT1 at R_G=20.75 Ω (e.g. Cases 1, 3, and 5) and at R_G=83 Ω (e.g. Case 2, 4, and 6).

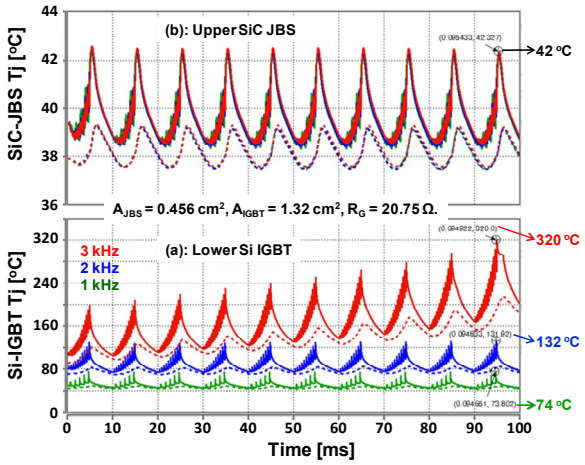

Fig. 17: Frequency dependence junction temperature waveforms for the Si_IGBT (a) and SiC_JBS2 (b) at R_G=20.75 Ω (e.g. Case 1).

VI. CONCLUSION

A parametric simulation study is presented to optimize the design of a high-current 4.5 kV half-bridge Si-IGBT/SiC-JBS hybrid module for medium voltage hard-switched power conversion as well as to compare the performance of the hybrid module to the all-Si configuration. The simulations are performed using the experimentally validated electrical model for the 4.5 kV Si IGBT and SiC JBS diode, and the developed and validated thermal model for the module package. The simulations are performed for a circuit that emulates hard switch conditions similar to a full wave inverter with a quarter sine-wave current cycle, while only requiring the use of one 4.5 kV IGBT switch and one 4.5 kV JBS diode. The results indicate that the performance of the module can be optimized by varying power module parameters such as the number of Si IGBT and SiC JBS diode chips, gate resistance, and switching frequency.

REFERENCES

[1] Tam Duong, Allen Hefner, Karl Hobart, Sei-Hyung Ryu, David Grider, David Berning, Jose M. Ortiz-Rodriguez, Eugene Imhoff, Jerry Sherbondy, "Comparison of 4.5 kV SiC JBS and Si PiN Diodes for 4.5 kV Si IGBT Anti-parallel Diode Applications," Proceedings of the 2011 IEEE Applied Power Electronics Conference (APEC), March 6 - 10, 2010, Fort Worth, Texas. pp. 1057-1063.

[2] K. D. Hobart, E. A. Imhoff, F. J. Kub, A. R. Hefner Jr., T. H. Duong, J. M. Ortiz-Rodriguez, S.-H. Ryu, D. Grider, S. Leslie, J. Sherbondy, and B. Ray, "Performance of Hybrid 4.5kV SiC JBS Freewheeling Diode and Si IGBT," Proceedings of the 2011 International Conference on Silicon Carbide and Related Materials (ICSCRM), September 11-16, 2011, Cleveland, OH.

[3] Allen R. Hefner, Jr., "A Dynamic Electro-Thermal Model for the IGBT," in the IEEE Trans. on Industry Applications, vol. 30, no. 2, pp. 394-405, 1994.

[4] T. R. McNutt, A. Hefner, Jr., H. Mantooth, J. Duliere, D. Berning, and R. Singh, "Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator," IEEE Trans. Power Electron., vol. 19, no. 3, pp. 573-581, 2004.

[5] J. M. Ortiz-Rodríguez, M. Hernández-Mora, T. Duong, S. G. Leslie, and A. R. Hefner," Thermal Network Component Models for 10 kV SiC Power Module Packages," Proceedings of the 2008 IEEE Power

Electronics Specialists Conference (PESC), June 15-19, 2008, Island of Rhodes, Greece, pp. 4770-4775.

[6] T. H. Duong, J. M. Ortiz-Rodríguez, R. N. Raju, and A. R. Hefner, "Electro-Thermal Simulation of a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module," in the Proc., Power Electronics Specialist Conference, Rhodes, GR, June 15-19, 2008, pp. 1592 – 1597.

Table 1: Power and Energy Calculations for 4.5 kV Si IGBT/SiC JBS Module

Case #	*Total*	Si IGBT					Anti-parallel Diode				
	P [W]	P_{IGBT} [W]	$E_{ON-STATE}$ [J]	$E_{SW,ON}$ [J]	$E_{SW,OFF}$ [J]	$T_{PEAK,IGBT}$ [^{o} C]	$P_{JBS/PiN}$ [W]	E_{COND} [J]	$E_{SW,ON}$ [J]	$E_{SW,OFF}$ [J]	$T_{PEAK,JBS/PiN}$ [^{o} C]
1	244.32	193.43	0.1092	0.0279	0.2977	73.71	50.890	0.0140	0.0758	558.78u	42.18
2	257.24	206.02	0.1464	0.0674	0.3068	76.25	51.219	0.0171	0.0797	152.80u	42.27
3	227.16	193.72	0.1234	0.0309	0.2924	73.82	33.438	0.0124	0.0499	165.32u	31.13
4	239.97	206.33	0.1419	0.0651	0.3084	76.31	33.635	0.0114	0.0493	997.78u	31.16
5	218.82	194.33	0.1147	0.0259	0.2998	73.90	24.494	0.0087	0.0346	926.68u	27.42
6	231.59	206.97	0.1423	0.0584	0.3063	76.37	24.623	0.0090	0.0354	307.88u	27.43
7	502.29	270.76	0.1129	0.2134	0.3381	89.11	231.53	0.0105	0.0414	0.6212	34.90
8	540.10	489.09	0.0514	0.0251	0.4582	131.98	51.01	0.0127	0.0275	760.55u	42.27

Case 1: $A_{JBS} = 0.456\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 20.75\ \Omega$, fsw = 1 kHz, SiC JBS Diode
Case 2: $A_{JBS} = 0.456\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 83\ \Omega$, fsw = 1 kHz, SiC JBS Diode
Case 3: $A_{JBS} = 0.912\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 20.75\ \Omega$, fsw = 1 kHz, SiC JBS Diode
Case 4: $A_{JBS} = 0.912\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 83\ \Omega$, fsw = 1 kHz, SiC JBS Diode
Case 5: $A_{JBS} = 1.824\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 20.75\ \Omega$, fsw = 1 kHz, SiC JBS Diode
Case 6: $A_{JBS} = 1.824\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 83\ \Omega$, fsw = 1 kHz, SiC JBS Diode
Case 7: $A_{Si\text{-}PiN} = 0.620\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 83\ \Omega$, fsw = 1 kHz, Si PiN Diode
Case 8: $A_{JBS} = 0.456\ cm^2$, $A_{IGBT} = 1.32\ cm^2$, $R_G = 20.75\ \Omega$, fsw = 2 kHz, SiC JBS Diode