Fabrication and Electrical Characterization of Fully CMOS-Compatible Si Single-Electron Devices

P. J. Koppinen, M. D. Stewart, Jr., and Neil M. Zimmerman

***Abstract*—We present electrical data of silicon single-electron devices fabricated with CMOS techniques and protocols. The easily tuned devices show clean Coulomb diamonds at $T = 30$ mK and a charge offset drift of $0.01e$ over eight days. In addition, the devices exhibit robust transistor characteristics, including uniformity within about ± 0.25 V in the threshold voltage, gate resistances greater than 10 GΩ, and immunity to dielectric breakdown in electric fields as high as 4 MV/cm. These results highlight the benefits in device performance of a silicon-foundry-compatible process for single-electron device fabrication.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS), Coulomb blockade, quantum dot, silicon-on-insulator (SOI), single-electron transistor, single-electron tunneling (SET).**

I. Introduction and Motivation

SINGLE-ELECTRON tunneling (SET) devices [1] are promising candidates for a wide variety of nanoelectronics applications, such as sensitive electrometers [2], thermometers [3], electron pumps and turnstiles for current standards [4], [5], and quantum bits for quantum information processing [6]–[8]. In recent years, silicon has drawn a lot of attention as a candidate for practical SET devices for several reasons. These advantages include compatibility with complementary metal–oxide–semiconductor (CMOS) processing, good electrostatic control of the tunnel barriers [9], greater device stability as demonstrated by a lack of charge offset drift [10]–[12], and a relative lack of nuclear spins, an important source of decoherence in spin-based quantum information applications [13].

However, to become truly viable in any of these applications, devices must be fabricated which overcome the device-to-device variations and low yield associated with the processing typical of small-scale research programs. At the single device level, the gate voltage variation from one device to another may not be an important parameter; however, uniform device operation becomes crucial when trying to operate several SET devices simultaneously, e.g., in the large-scale integration of SET devices. The choice of device architecture can also impact the integrability of devices. For example, gate-to-gate variations in an architecture where more than one gate [7], [14] controls a single tunnel barrier can make finding the desired operating point a laborious iterative process.

In this paper, we demonstrate robust behavior and good uniformity of easily tuned fully CMOS[1] single-electron devices, which contain only silicon, thermally grown silicon dioxide (SiO_2), and phosphorous-doped polycrystalline silicon (poly-Si) in the active device region. The motivation for a fully CMOS approach to fabrication is twofold: 1) to minimize the number of impurities and defects near the active device region and 2) to avoid the instabilities associated with metallic oxides and, in particular, aluminum oxide. In this way, we avail ourselves of the best opportunity to fabricate uniform robust devices. In the following, we will discuss and demonstrate the robustness of our devices with respect to basic metal–oxide–semiconductor field-effect transistor (FET) (MOSFET) characteristics and SET device operation. In particular, we show that these devices exhibit only small variations of the threshold voltage from device to device, dielectrics which are robust against breakdown, and charge offset stability on the order of $0.01e$ over a period of several days.

II. Operating Principle of the Device and Fabrication

Our devices each contain a lightly boron-doped (p-type) mesa-etched single-crystal Si nanowire, n^+-type source and drain, and two layers of gates; see Fig. 1(a). The topmost gate layer, which we call the upper gate (UG), covers the entire device between the heavily doped source and drain. Applying a positive voltage to the UG inverts the underlying Si nanowire and provides conduction. The second gate layer, which we call the lower gates, consists of three finger gates which wrap around the Si nanowire. These are denoted as LGS (closest to the source), LGC (center gate), and LGD (closest to the drain); see Fig. 1(b).[2] The LG fingers are primarily used to locally deplete the electron gas and, therefore, to create electrostatically controlled tunnel barriers (LGS and LGD), or to modulate the electrostatic potential of a quantum dot (LGC).

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[1] We use "fully CMOS" as a shorthand to indicate that our techniques and protocols are compatible with CMOS processing and avoid metals and dopants near the QDs as in silicon foundries; we do not intend this phrase to imply that our process flow can be implemented without modification in any specific CMOS node.

[2] We note that, as discussed later, yield issues drove us to use long gates and large dots for this first fabrication run. These large dot sizes also precluded the possibility of achieving the few electron regime.

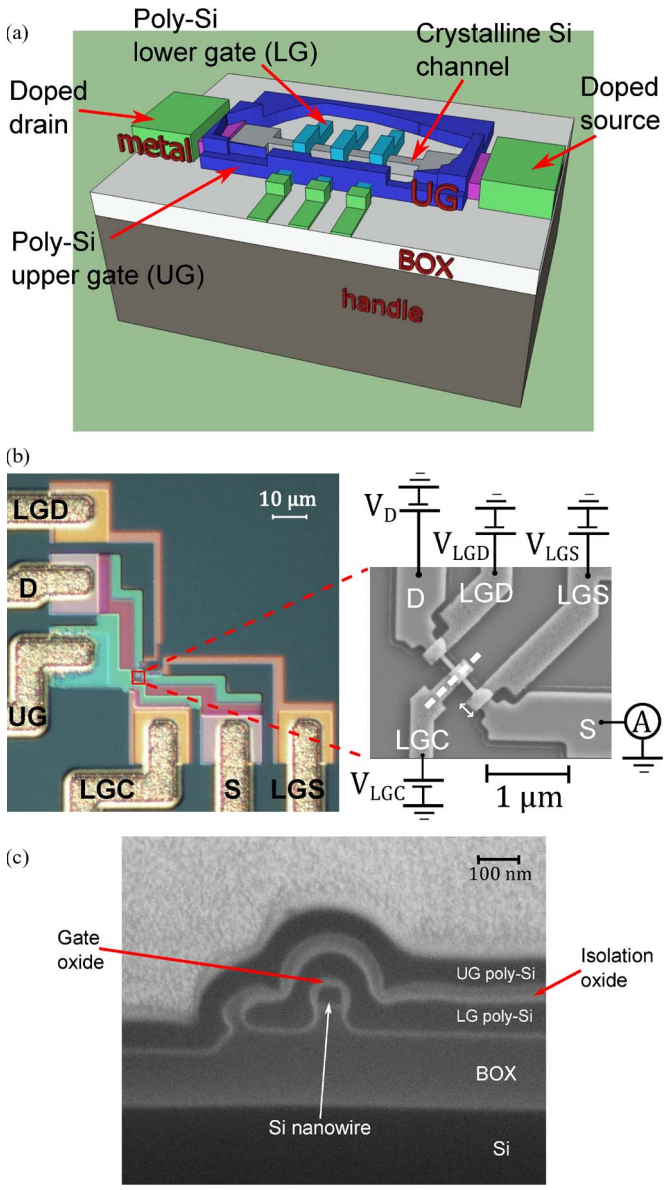

Fig. 1. (a) Schematic view of a sample. Device operation is described in the text. (b) (Left) Optical micrograph of a sample. (Right) SEM micrograph (before UG deposition) of the active device area, and schematics of an electrical measurement circuit (does not show V_{UG}). Lower gates LGS, LGC, and LGD are poly-Si, and the conducting channel (S/D) is single-crystal Si. Channel and lower gates sit on top of the buried silicon oxide (BOX). The white arrow next to the finger gate indicates the gate length. (c) Cross-sectional SEM image of a device along the dashed white line in (b). The darker areas are Si, the gray areas are SiO_2, and the bright layer on top is a protective layer of Pt deposited prior to the FIB cut.

The devices are fabricated on a 150 mm silicon-on-insulator (SOI) wafer, with a doping density of about 10^{15} cm^{-3}, an initial SOI thickness of 100 nm, and a buried oxide (BOX) thickness of 200 nm. To minimize the interface trap density at the gate oxide interface of the nanowire [15], [16], we fabricate the SOI nanowires at a 45° angle with respect to the flat ($\langle 110 \rangle$) of the wafer in order to obtain a $\langle 100 \rangle$ crystallographic equivalent orientation on each facet of the nanowire.

As previously mentioned, we fabricate these devices with a fully CMOS process flow developed at the Center for Nanoscale Science and Technology nanofabrication user facility at the National Institute of Standards and Technology.

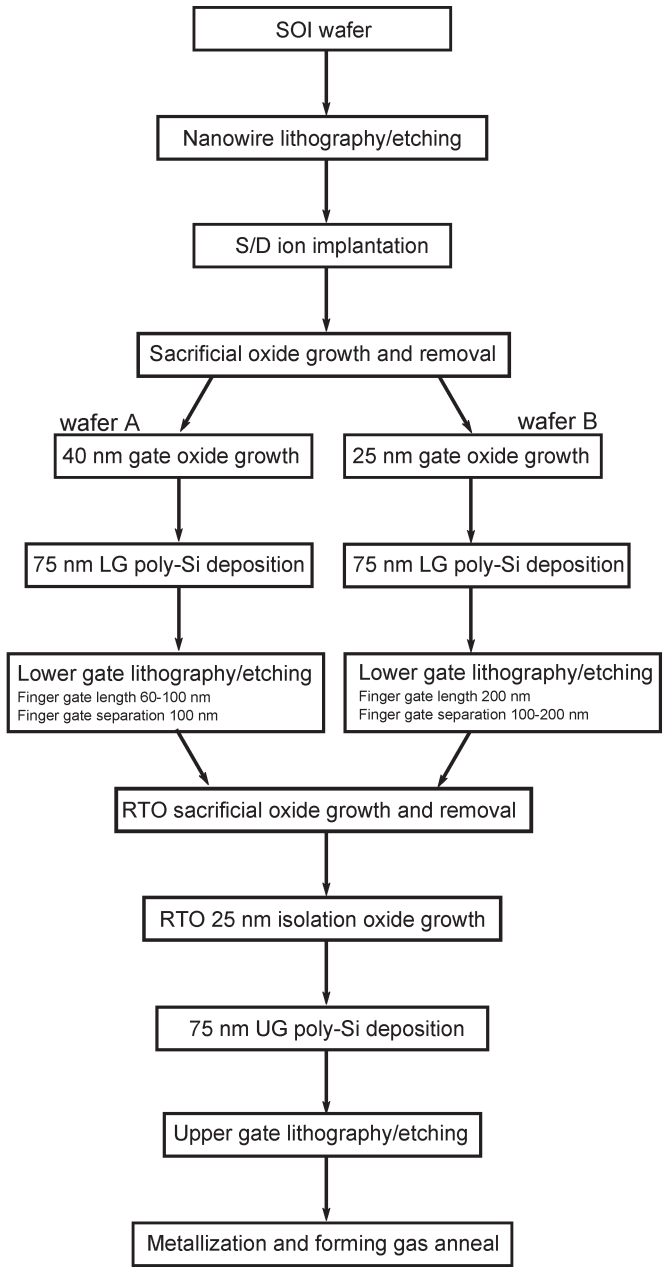

Fig. 2. Flowchart of the condensed fabrication process described in the text.

The fabrication process is shown in Fig. 2. To put our work in context, our processing differs from others [14], [17]–[19] in that we avoid metal gates and their associated lower quality metal oxides in favor of Si, poly-Si, and high-quality thermal SiO_2. Moreover, unlike other fully CMOS efforts [20], we also avoid deliberately placing dopants near the Si quantum dots. The nanowire, lower gate, and upper gate lithography and etching were performed with negative tone electron beam lithography using hydrogen silsesquioxane as a resist and dry etching in Cl_2 chemistry. Our etch recipe was to first condition the chamber by performing a 15 min clean on a dummy Si wafer and then perform our etch with 50 sccm of Cl_2, 20 sccm of O_2, 50 W RF power, 5 mtorr pressure, and zero ICP power. Source and drain areas located about 10 μm away from the active device area were implanted with phosphorous at 30 keV with a dose of 10^{15} cm^{-2}. We grew sacrificial oxide on both the

TABLE I
SUMMARY OF THE WAFER CHARACTERISTICS

Test	Wafer A result	# tested	Wafer B result	# tested
Threshold voltage value and uniformity at 300 K	[-0.4 V, -0.1 V]	8	[-0.1 V, 0.3 V]	4
Threshold voltage value and uniformity at 2.2 K	[0.2 V, 0.4 V]	3	[0.5 V, 1 V]	4
LG Turn–off voltage value and uniformity at 300 K	–	–	[-1.5 V, -1 V]	4
LG Turn–off voltage value and uniformity at 2.2 K	–	–	[-1 V, -0.5 V]	4
On/off ratio [5]	10^3	8	10^4	4
Subthreshold slope (300 K)	–	–	80 mV/decade	4
UG–channel leakage [1]	>10 GΩ at $\pm$ 0.25 MV/cm	7/8[4]	>10 GΩ at $\pm$ 4 MV/cm	4/4[4]
UG breakdown [2]	no breakdown at $\pm$ 2.5 MV/cm	2/2[4]	2 breakdown at $\pm$ 4 MV/cm	2/4[4]
LG–UG leakage	>10 GΩ at $\pm$ 0.4 MV/cm	24/24[4]	>10 GΩ at $\pm$ 4 MV/cm	46/49[4]
LG breakdown [3]	no breakdown at $\pm$ 4 MV/cm	6/6[4]	no breakdown at $\pm$ 4 MV/cm	46/49[4]
Functional nanowires	8	8	4	34
Functional LG fingers	0	24	12	12

Notes: [1] One sample on wafer A showed leakage resistance of 100 MΩ to the channel.
[2] Breakdown generated threshold voltage shift after the voltage excursion.
[3] Breakdown generated leakage path.
[4] number tested that showed the result/total number tested.
[5] The on/off ratio was measured with drain bias of 1 mV at room temperature. It was the same at low temperature and is a lower bound.
Electric field strengths are calculated with the initial oxide thicknesses.

nanowire and the lower gate layer in order to remove possible etch damage produced during the dry etch. Both the sacrificial oxide and the gate oxide on the nanowire were grown in a tube furnace at 850 °C and 950 °C, respectively, with a 20 min anneal in N_2 at the oxidation temperature to reduce the charge density in the oxide. The sacrificial oxide was removed with a short 100 : 1 HF dip. The lower gate and upper gate layers were 75 nm thick *in situ* phosphorous-doped poly-Si deposited by low-pressure chemical vapor deposition (LPCVD) at 625 °C. Both gate layers were degenerately doped to ensure electrical conduction at low temperatures with a typical resistivity of 10–30 mΩ · cm (determined from two terminal measurements at 2.2 K). The sacrificial oxide on the lower gate and the isolation oxide between the lower gate and the upper gate were grown with rapid thermal oxidation (RTO) at 1000 °C. The final steps of the process were metallization of ohmic contacts with sputter-deposited Al–1% Si and a forming gas anneal at 425 °C for 30 min. Except for the addition of sacrificial oxidation and stripping, the basic processing is the same as that in [12] but differs in several details. We note that the devices presented here possess superior performance to those in [12].

To date, we have fabricated devices on two 150 mm wafers which we call A and B[3]; see Fig. 2. The main differences between the wafers are the nominal gate oxide thickness and the finger gate lengths. The SOI nanowire width and length are 70 and 800 nm, respectively, for both wafers. Each wafer contained 48 dies: 36 with two devices as in Fig. 1 on each and 12 diagnostic dies located on the diagonals of the wafer. The diagnostic dies contained conventional FETs with a 70 nm wide SOI nanowire as a channel and test structures to measure the resistance of ohmic contacts and the resistivity of the poly-Si.

[3]Wafer A was called MS-3GD6 and B was called MS-3GD2 during the fabrication.

A cross-sectional SEM image produced by a focused ion beam (FIB) cut along the LGC finger [the white dashed line in Fig. 1(b)] of a finished device is shown in Fig. 1(c). The darker areas in the micrograph are Si, and the gray areas are SiO_2. The cross-sectional image shows that both poly-Si films of upper gate and lower gate layers conformally coat the layers underneath as is expected from LPCVD growth and that the oxides are continuous, as needed for electrical isolation.

III. RESULTS AND DISCUSSION

We characterized many devices and FETs from randomly chosen dies across both wafers at room temperature and at 2.2 K. In addition, one of the devices was cooled down and measured in a dilution refrigerator at 30 mK. The summary of the electrical characterization is presented in Table I.

Fig. 3(a) shows the turn-on characteristics of different devices (as in Fig. 1) on wafer A (40 nm gate oxide). The solid lines and dashed lines correspond to data taken at 300 K and 2.2 K, respectively. At room temperature, the threshold voltages, as obtained by linearly extrapolating the current to zero [21], were $V_T = -0.3$ V with a standard deviation of 0.1 V, and there was a threshold shift of about 0.6 V when the devices were cooled down. A simple estimate of the expected threshold voltage [22] which ignores the presence of any fixed oxide charge and which treats the devices as planar FETs yields $V_T = -0.1$ V at room temperature and $V_T = 0.4$ V at 2.2 K, which is in reasonable agreement with our measured values. Wafer B (25 nm gate oxide) showed uniform turn-on characteristics with $V_T \approx 0$ V at room temperature and a nearly equal shift in the threshold when cooled down. The diagnostic transistors on each wafer also showed similar turn-on behavior. A typical subthreshold slope for these devices was 80 mV/decade at room temperature (the ideal subthreshold

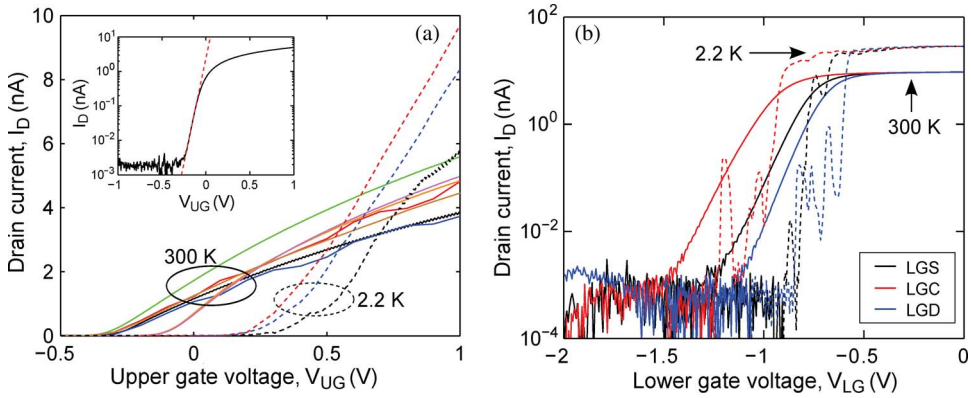

Fig. 3. (a) Turn-on characteristics of SET devices measured as MOSFETs with 1 mV bias applied to the drain. Solid lines represent room-temperature data for different devices, and dashed lines are three different devices measured at 2.2 K. (Inset) Turn-on characteristic of a single device in a semilogarithmic plot measured at room temperature with 1 mV drain bias. Devices show good uniformity in threshold voltages, and the inset shows subthreshold slope of 80 mV/decade (slope of red dashed line). (b) Turn-off characteristics of each individual lower gate of a device measured (solid lines) at room temperature and (dashed lines) at 2.2 K. Black represents LGS, red (gray, the leftmost curve at both temperatures) represents LGC, and blue (gray, the rightmost curve at both temperatures) represents LGD. Upper gate voltages $V_{\rm UG}$ were 1.3 and 2 V for the room-temperature data and 2.2 K data, respectively. The data were taken with 10 mV drain bias. All lower gates turn off conduction in the channel and show an on/off ratio of about 10^4.

slope is 60 mV/decade [22]) with an on/off ratio of 10^4; see the inset in Fig. 3(a). Typical turn-off characteristics for each of the finger gates (LGS, LGC, and LGD) measured at both room temperature and 2.2 K for wafer B are shown in Fig. 3(b). The room-temperature data were taken with an upper gate voltage $V_{\rm UG} = 1.3$ V, while the low-temperature data were taken with $V_{\rm UG} = 2$ V. The ranges for turn-off voltages, i.e., the lower gate voltage $V_{\rm LG}$ at 100 pA of drain current I_D, were from -1.5 to -1 V at room temperature and -1 to -0.5 V at 2.2 K for all measured lower gates for all devices.

We also tested the robustness of the gate oxide and the isolation oxide on wafer B. In these tests, the gate voltage was swept in steps up to ± 10 V while the source–drain and leakage currents were simultaneously measured to the other gates and to the channel. All leakage resistances between the channel and either layer of gates or between gates were > 10 GΩ up to gate voltages of ± 10 V. After each gate voltage excursion, the turn-on characteristics were remeasured in order to determine if there was a change in the threshold voltage or slope. Diagnostic FETs were immune to electric fields up to 4 MV/cm (± 10 V), showing no change in V_T nor generation of a leakage path (Fig. 4). Similar robustness measurements for SET devices showed no threshold shift up to 2.8 MV/cm (± 7 V) and only a small (0.05 and 0.2 V) threshold shift after a gate excursion of 4 MV/cm (± 10 V) in two out of four devices. No observable leakage path developed during the sweep. A typical literature value of the breakdown field of metal–oxide–semiconductor capacitors is about 10 MV/cm, before generating a leakage path [23]. We also performed robustness measurements of the isolation oxide between the lower gates and the upper gate on about 50 different lower gate fingers on different devices across the wafer. Only three fingers developed a breakdown path during the ± 10 V sweep.

Previously, we have discussed the robustness and uniformity of devices in terms of MOSFET performance, and in the following, we present device characteristics when operated in a single-electron device mode. First, we discuss ease of tuning. The right-hand side of Fig. 1(b) shows a schematic of a typical

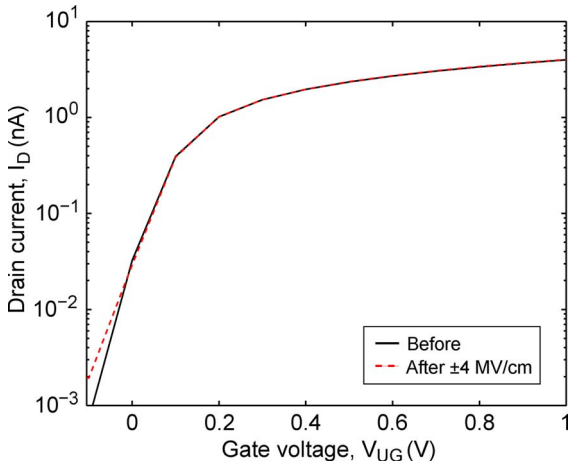

Fig. 4. Turn-on characteristics, i.e., drain current as a function of gate voltage of a MOSFET transistor with 25 nm gate oxide thickness. Data were taken with the drain voltage V_D of 1 mV. Solid (black) line is initial turn-on curve, and dashed (red or gray) line is turn-on curve after ± 10 V (4 MV/cm) excursion in the gate voltage. The identical curves indicate immunity to dielectric breakdown up to ± 4 MV/cm.

measurement circuit for a device. Tuning the device to display SET oscillations took very little time, on the order of minutes, because there was very little cross-capacitance between gates and each barrier was controlled by a single gate voltage. To tune a device into SET mode, we first applied a small bias voltage to the drain (on the order of 1 mV) and set the upper gate to a voltage (obtained from a short upper gate sweep, typically about 2 V) which gave about 1 nA of current. Next, a two dimensional sweep of $V_{\rm LGS}$ and $V_{\rm LGD}$ (with $V_{\rm LGC}$ well above the turn-off voltage) was performed to find the voltages where each of these gates began to turn off conduction. Typically, the barrier voltages were about -0.6 V. We note that barrier resistances responded symmetrically to $V_{\rm LGS}$ and $V_{\rm LGD}$. After fine-tuning $V_{\rm LGS}$ and $V_{\rm LGD}$, we measured SET oscillations by sweeping $V_{\rm LGC}$ with the other gate voltages fixed.

Coulomb oscillations of a device taken at 2.2 K are shown in Fig. 5. The oscillations were very regular with a period of

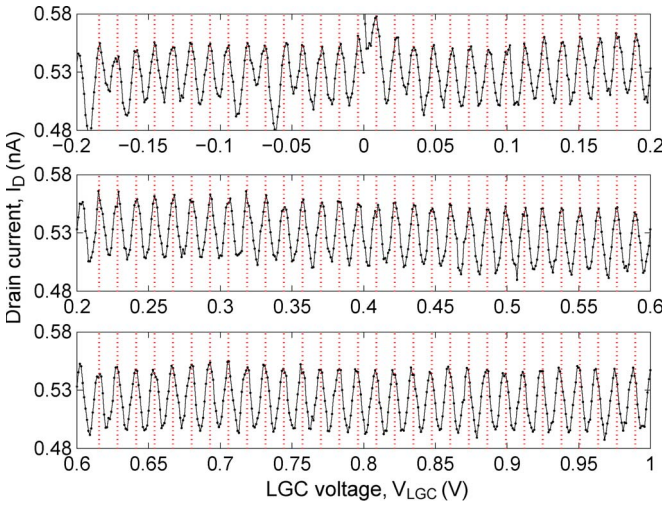

Fig. 5. SET oscillations of a device at 2.2 K; vertical dashed lines (red or gray) are separated by a period of 12.9 mV. The data show good uniformity of the gate capacitance over 90 periods.

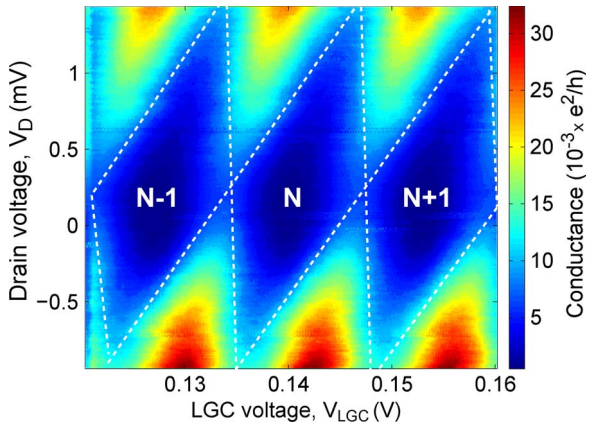

Fig. 6. Coulomb diamonds measured at 30 mK for a SET device; N is the electron number. Charging energy $E_C = 1.2$ meV, drain capacitance $C_D = 7$ aF, and total capacitance of the island $C_\Sigma = 70$ aF, extracted from the diamond data.

12.9 mV over an LGC gate voltage range of 1.2 V, corresponding to about 90 periods. The capacitance of LGC to the dot, extracted from the SET oscillation period, was about 12 aF. Coulomb diamond data recorded at 30 mK for the same device are shown in Fig. 6. The charging energy and lever arm α, which converts the gate voltage to the electrostatic potential of the island $U_{\rm dot} = \alpha V_{\rm LGC}$, extracted from the diamond data were 1.2 meV and 0.09, respectively. The capacitance between the dot and each of the other two lower gates (LGS and LGD) was measured relative to the LGC capacitance by following the position of a current peak when sweeping LGS (or LGD) and LGC (data not shown). The capacitance values for both LGS and LGD were about 5 aF, indicating that the dot was located in the center of the device. This, together with the agreement between the measured capacitance to LGC (12 aF) and that calculated from the geometry (14 aF), gives us confidence that the dot being modulated was an intentional dot formed through electrostatic control of LGS and LGD rather than through barriers formed by defects.

As a more strict test of the quality of our fabrication, we performed charge offset drift measurements on several devices. This measurement consisted of repeatedly measured Coulomb blockade oscillations at a fixed time interval over several days. Fig. 7(a) shows a typical collection of SET oscillations taken at 2.2 K and spanning the total duration of the charge offset drift measurement. To obtain charge offset drift values for each curve, a sinusoidal function of the form $I_{\rm drain} = I_0 \sin[2\pi(V_{\rm LGC}/\Delta V + Q_0/e)]$ was fit to the measured data. Here, I_0 is the amplitude of the oscillations, and ΔV is the oscillation period. The phase of the sinusoidal fit function Q_0 is a charge offset value for each curve. The result of this procedure is shown in Fig. 7(b). The devices exhibited very stable behavior with a drift in $|\Delta Q_0(t)| \approx 0.01e$ over eight days of measurement. Moreover, these results rival those of similar Si devices fabricated in other foundries [10]–[12]. In addition, after eight days of measurement, we thermally cycled the device to room temperature. Fig. 7 shows these data as well. While the thermal cycle resulted in a shift in the charge offset value of about $0.1e$, the level of drift observed was identical both before and after the thermal cycle. Finally, a measurement of I_D versus $V_{\rm LGC}$ voltage with the same LGS, LGD, and UG voltages after the thermal cycle reproduced not only the SET oscillations at the same value $V_{\rm LGC}$ with a charge offset of $0.1e$ but also the aperiodic features which become prominent when the gate begins to turn off conduction (the inset of Fig. 7).

While the previous results indicate that the cleanliness of our CMOS fabrication is quite good, many devices in this first device run failed electrically either by not turning on or through an inability to turn off conduction with the LG fingers. This drove our yield of fully functioning (in which we were able to measure intentional Coulomb blockade) devices down to 4/34 devices measured. We have been able to identify the gross fabrication failures, by cross-sectioning devices with FIB in conjunction with the electrical results. In brief, the failure modes are the result of overoxidation of the SOI nanowire and the LG fingers, as well as the overall amount of oxide removed in the processing. We believe that further development of our process flow will ameliorate these failures.

IV. Summary and Conclusions

In summary, we have demonstrated devices which show good uniformity in electrical characteristics from device to device within a wafer and between wafers. Moreover, the devices are quite robust against dielectric breakdown up to electric fields of 4 MV/cm. Finally, and most importantly, when operated as a single-electron device, these devices show very stable behavior. Taken together, these characteristics indicate a relatively clean and stable electrostatic environment throughout the fabrication process. We attribute these successes to the minimization of impurities and defects which result from our CMOS processing and material restrictions. To further improve the usefulness of these devices as current standards and quantum information devices, our next tasks include the following: 1) substantially increasing the yield and 2) making shorter finger gates so that we can use those gates both to generate barriers and as plunger gates.

While these results indicate that a fully CMOS process pays dividends in device performance, it also complicates the

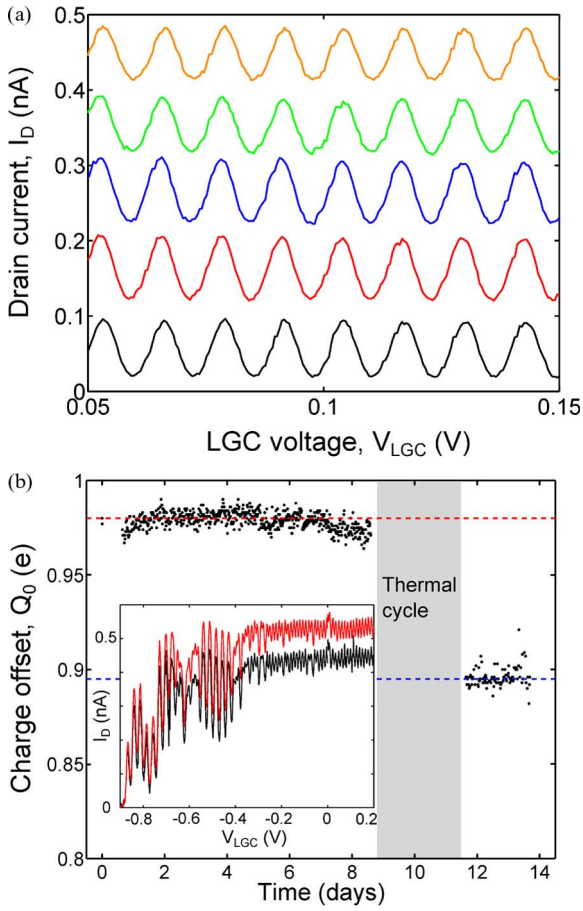

Fig. 7. (a) Example of single-electron oscillations taken at different times spanning the total duration of charge offset drift measurements; curves are offset vertically for clarity. (b) Charge offset drift derived from Coulomb oscillations; red and blue (gray) dashed horizontal lines are a guide for the eye. The gray area indicates the time interval of the thermal cycle. After the thermal cycle, the charge offset value Q_0 changed by $0.1e$ but remained as stable as before. (Inset) Drain current as a function of LGC voltage V_{LGC} (black line) before and (red or gray line) after the thermal cycle. The data in the inset before and after the thermal cycle are taken with the same gate voltages. All features in the data are reproduced after the thermal cycle.

fabrication. We believe that our results in terms of reliability, ease of tuning, and clean SET behavior all justify the cost of the increased complexity of fabrication.

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