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Metrology for Nanosystems and Nanoelectronics Reliability Assessments*

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Abstract — **The traditional models and techniques for studying reliability in integrated circuits may not be appropriate for nanoelectronics and nanosystems. In this paper, we present an overview of a number of materials and metrology techniques currently under development in our group at NIST. Among other topics, we will assess the techniques and models currently used for evaluating integrated circuit reliability, as well as present some new approaches.**

Index Terms* – *CBCM, charge based capacitance measurement, interconnects, metrology techniques, nanoelectronics, reliability, three-dimensional integrated circuits, through silicon vias, TSVs

I INTRODUCTION

Nanoelectronic systems, as with most nano-systems, are characterized by large surface-to-volume ratios; thus, most of the materials in such structures are located at surfaces and interfaces. Given that the behavioral properties of interfacial materials are both qualitatively and quantitatively different from those in the bulk, it is expected that the performance-limiting phenomena in nanoelectronic systems will be quite different from those in microelectronics systems. This situation is further complicated by the introduction of new materials and integration schemes in the fabrication of such nanoelectronic systems.

In fact, integrated electronic device lifetimes have declined almost monotonically with decreasing device dimensions. For example, the lifetimes of the current nominal 15 nm to 30 nm geometry devices are projected to be around 5 to 20 years with normal operation. However, when these devices are stressed, even with modest heat or voltage, the lifetimes drop precipitously into the few months range.

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In contrast, devices in the microelectronics (2 μm to 5 μm) regime had estimated lifetimes in the 1,000 to 5,000 year range. Thus, by extrapolation, the life expectancy of a 1.2 nm device is estimated to be on the order of a few years at best, but most possibly only months. Is this the end of the road of the electronics revolution? How realistic are these projections? Could they be based on the wrong models and metrology?

In this paper, we present an overview of a number of materials and metrology issues and some of the new techniques and models currently under development in our group at NIST aimed at addressing these issues.

Our work is motivated by the migration towards functional diversification of electronics, most of which is taking place in the nanoelectronics realm. Traditionally, the semiconductor industry has provided new value in time by scaling / shrinking physical dimensions, and occasionally introducing new materials. These tweaks used to be sufficient for improving computation performance (through faster clock frequencies, and memory capacity). As CMOS devices reach their fundamental physical limits, the aggressive scaling characteristic of the Moore's law, will no longer be sufficient for the desired performance improvements. This realization has led to the paradigm of functional diversification (also known as More-Than-Moore), to attain the equivalent performance that would otherwise have been attainable by scaling (equivalent scaling). The More-Than-Moore approach allows for non-digital functionalities to be integrated with digital systems on the same chip or package. As envisioned, integrated systems of the future will perform diverse functions, such as high-accuracy sensing of real-time signals, energy harvesting, and on-chip chemical/biological testing, etc., in addition to high-performance computation, high-density storage and high-bandwidth communication. These emerging hybrid devices involve the design and integration of multiple device technologies and diverse components in a single heterogeneous system that is high- performance, energy-efficient and reliable. Enabling such diverse functionality in a single system may require a radical shift in the principles of system design and integration. These new approaches to increase performance also require new materials and integration schemes, with higher interconnect densities and increase thermal loads, etc. Furthermore, new

packaging technologies are required when diverse devices such as bio-chips, integrated optics, embedded active and passive devices, MEMS, printable circuits (semiconductor, light emitter, RF, etc.) are integrated into a monolithic device. Such highly integrated devices will exhibit new and previously unknown performance limiting failure modes. We need to anticipate, understand and monitor such potential issues.

The fundamental assumption of our work is that it is probable that the traditional models and techniques for studying reliability in integrated circuits may not be appropriate for nanoelectronics and nanosystems. For example, electromigration in interconnects have been extensively studied and used to predict interconnect life expectancy. In the interest of time, high current densities (on the order of MA/cm^2) and temperatures (in the 100 ^{0}C to 300 ^{0}C range) are normally used in stress interconnects to project performance life expectations. Unfortunately, these conditions are so far removed from the typical normal operating conditions of most nanoelectronic devices that the results obtained, and predictions based on them, are almost certainly irrelevant to normal use conditions. Also, these conventional techniques are frequently inadequate in detecting the early onset of failures. Furthermore, the activation energy extracted from the temperature dependence of lifetimes under these "extreme" stress conditions may not be relevant to the actual kinetics of the underlying phenomena responsible for the observed electromigration failures. In our current work, we believe that with judicious selection and control of the experimental stress conditions and cross collaboration with other techniques it should be possible to resolve many of the problems that limit the metrological value the traditional techniques.

In this paper, we discuss our attempts to identify and characterize types of performance-limiting defects in three-dimensional (3-D) nanoelectronic devices, with special focus on 3-D interconnects, and relate the defects to where and why they form. In addition, we discuss non-destructive techniques for identifying such performance-limiting defects, without interrupting the responsible mechanistic phenomena. Finally, we will also discuss materials integration issues; e.g., impact of across wafer material properties variability on variation on the electrical properties of scaled integrated circuits.

II RF-BASED TECHNIQUES

An aspect of our work involves the use of microwave / radio-frequency (RF) radiation to study the evolution of nano-electronic device performance under stress. In these studies, we use frequencies up to 20 GHz to probe devices, at ambient temperatures and after stress. By inspection of the scattering parameters (S-parameters), one can obtain qualitative assessments of device design, integration and material chemistry evolution issues. With modeling, one can also quantitatively extract changes in the electrical characteristics of the devices with stress. Illustratively, we have shown elsewhere that RF reflectance losses (S11 and S22 parameters) are sensitive to changes in device structure long before such changes are detectable by any microscopy technique, including AFM [1].

Figure 1, shows the changes in broadband radio-frequency signal transmission loss in a low resistivity silicon substrate of a silicon-filled through-silicon via (TSV) test structure, as a function of thermal-stress cycling. In these experiments, the samples were repeatedly cycled between 30^{o}C and 150^{o}C in ambient air. The signal insertion losses increased with increasing number of cycles, indicating heat-induced changes in test structure.

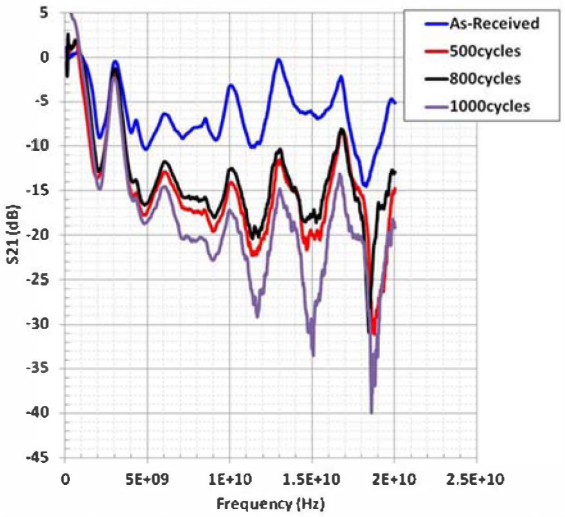

Figure 1: Changes in broadband radio-frequency signals insertion loss in a silicon-filled TSV test structure, as a function of thermal-stress cycling.

In order to ascertain the cause of the increased RF transmission losses with respect to the number of thermal cycles, further analysis is required. By the application of the AFM technique, topographical analysis of the test structures under different test conditions can be performed. Figure 2 shows the AFM images of the test structure after varying number of thermal cycles. Before thermal cycling (Figure 2a), it can be observed from the AFM image that the SiO_2 isolation liner appears uniform without any void and grooves. However, after 1000 thermal cycles (figure 2b), very visible seam is observed at the centre of the SiO2 isolation liner. After 1600 thermal cycles (figure 2c) very visible voids are observed to form at the seam location.

By performing a scan profile across the SiO_2 isolation liner, the void area was calculated as a function of the number of thermal cycles, as shown in Figure 3. From this graph it is found that the void area increased with increasing number of thermal cycles.

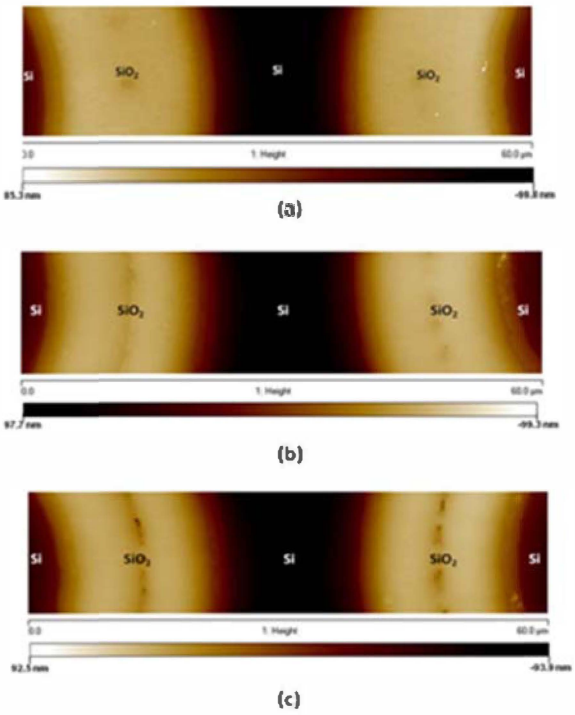

Figure 2: AFM topography image showing the morphological evolution of the SiO_2 isolation liner with thermal cycling. (a) As-received state (b) after 1000 thermal cycles (c) after 1600 thermal cycles.

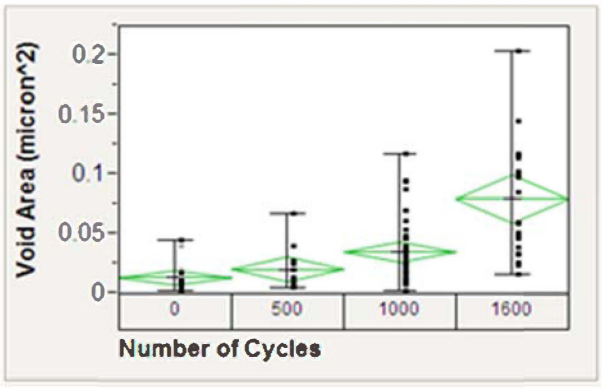

Figure 3: Plot of the void area in SiO_2 isolation layer as a function of the number of thermal cycles.

The RF signal losses in the test structure are attributed to signal scattering within the dielectric isolation layer by possible voids that formed and grew within the dielectric film during thermal stressing [1]. These voids appear to coalesce into a seam in the center of the dielectric field.

In another 3-D interconnect example, we are focusing on the development of Low Frequency Noise / Flicker noise (1/f) based techniques for monitoring electromigration experiments [2] in metal filled TSVs. Specifically, the weak dependence of Flicker noise on temperature is an intriguing question that needs to be addressed.

III SCANNING PROBE BASED TECHNIQUES

We are working on Scanning Probe Microscopy as a non-destructive real-time metrology technique. There are a variety of techniques that can measure the localized capacitance between a Scanning Probe Microscope (SPM) tip and a sample, including intermittent contact scanning capacitance (IC-SCM) or scanning microwave microscopy (SMWM) and various implementations of scanning Kelvin force (SKFM) and Kelvin probe microscopy. These techniques may prove useful, for example, in measuring the capacitance between adjacent metal lines or between through silicon vias (TSVs) and various metal lines, for both model and process validation. A shortcoming of these techniques is that they provide qualitative, rather than quantitative, capacitance measurements.

To address the limitations of these qualitative techniques, we are working on a charge based capacitance measurement (CBCM) technique that can be directly interfaced to a device through a scanning probe microscope tip. This goal is to be able to quantitatively measure small capacitances between adjacent metal structures without output to probe pads or any additional on-chip circuitry. The CBCM technique [3] technique has been demonstrated as a method to measure the capacitance between adjacent metal lines on integrated circuits when the CBCM is fabricated on the same chip as the devices under test. To move the CBCM circuitry to another chip requires connection through probe pads and bonding wires to the SPM tip. Towards this end, we have designed a test chip (Figure 4), with various implementations of a CBCM circuit. The chip contains CBCM circuits with different approaches to applying a bias to the capacitor under test and various on-chip approaches to compensate for the bonding pad capacitance. We are currently experimenting with methods of interfacing this chip to an SPM tip using varactor diodes to cancel the stray and pad capacitances and to isolate the tip-to-sample capacitance from the stray capacitances.

A second probe based effort seeks to image conductive structures beneath overlying dielectrics. Three probe based techniques have proven useful for this type of sub-surface imaging. Intermittent-contact scanning capacitance microscopy (IC-SCM) uses a vibrating tip to induce a differential capacitance (dC/dz) which can be detected by lock-in techniques [4]. IC-SCM is sensitive to adjacent conducting regions, which can be separated from the tip by many micrometers of low-k dielectric. Scanning Kelvin force microscopy (SKFM) also has the ability to sense

conductive structures in an insulating matrix with spatial resolution that can be increased through using high aspect ratio tips [5].

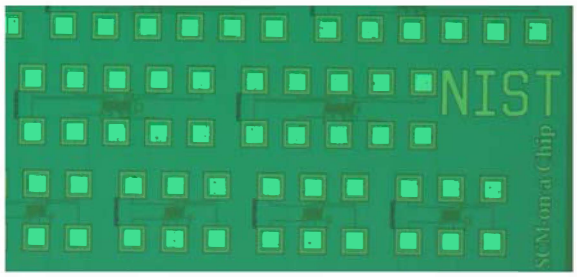

Figure 4: CBCM measurement circuits with various on-chip compensation capacitors.

We are also working with Scanning Microwave Microscopy (SMWM) [6]; this combines our interests in RF and Scanning Probe Microscopy. The technique could potentially detect both buried metal lines and voids in metallic structures through variations in the skin depth with incident microwave frequency. This technique opens up some interesting subsurface imaging possibilities. For example, can lines at different depths be biased at different frequencies and detected with SMWM, allowing detailed depth profiles to be determined? Likewise can the coupling of adjacent lines or lines at different depths be measured as a function of frequency using SMWM while avoiding specialized test structures and bonding pads?

III MATERIALS ISSUES

As in current microelectronics manufacturing, the reliability of the back-end-of-the-line (BEOL) in nanoelectronic systems is expected to be a challenge from materials integration perspectives. Pareto charts of field failure modes in advanced microelectronic devices show that damage of the final encapsulation dielectric stack is the overriding failure mode. Prior studies by [7] have shown that stresses in metal lines are influenced by the stiffness of the encapsulating dielectric layers used. It has also been shown that the electrical reliability of integrated circuits depends to a large extent on the properties of the dielectrics used. For example, the time-dependent-dielectric-breakdown (TDDB) of metal lines are significantly influenced by the reliability of the cap–metal line interface in a Cu-low-k system [8]; the electromigration lifetime of metal lines is highly influenced by their proximity to the passivation layer [9]. Using a variety of analytical techniques, we have examined the impact of local chemistry, and the mechanical properties, of the encapsulation dielectric films on the post-packaging device rejection rate of integrated circuit devices [10]. Figure 5 shows the correlation between post-packaging failure rates and the Young's modulus of various encapsulating dielectric types. Clearly, apart from film type D, the packaged device failure rate increased with increasing Young's modulus of the encapsulating dielectric film stack. This was attributed to the increase of thermal stress in the metal lines due to the increased constraint, and the inability of the metal lines to expand and contract under thermal stress. Furthermore, our data show that an increase in the non-bridging silanol (SiOH) content of the encapsulating dielectric results in a decrease in Young's modulus of the dielectric. This is anticipated since the non-bridging SiOH disrupts the silica network, which results in the decrease in Young's modulus with increasing SiOH concentration. Thus, the inability of the metal lines to expand and contract under thermal stress stems from the strong adhesion of dielectric material to the metal, thus fixing the loci of the surface planes of the metal, which could result in mechanical damage via voiding and delamination. The observation that a decrease in the stiffness of the encapsulating layer will reduce post-packaging device failure rates suggests that it may be desirable to increase the SiOH networks in the encapsulating dielectric films.

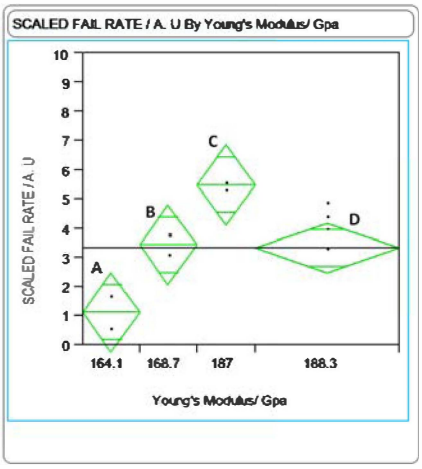

Figure 5: Correlation between post-packaging failure rates and the Young's modulus of various encapsulating dielectric types.

IV SUMMARY

In summary, we are working on various measurement techniques to study, understand and model potential performance limiting phenomena in nanoelectronic systems. The work so far has demonstrated the utility of radio-frequency probes in monitoring systems with large surface to bulk ratios.

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