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A case study on the impact of local material chemistry on the mechanical reliability of packaged integrated circuits: Correlation of the packaging fallout to the chemistry of passivation dielectrics ☆

Chukwudi A. Okoro, Yaw S. Obeng *

Semiconductor Electronics Division, National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20899, USA

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ABSTRACT

In this paper, we use a variety of analytical techniques to examine the impact of local chemistry, and the mechanical properties, of the encapsulation dielectric films on the post-packaging device rejection rate of integrated circuit devices. A strong dependence of lot rejection rate (LRR) on the effective Young's modulus of the encapsulating dielectric stack is demonstrated; specifically, the device fall out rate increases with increasing Young's modulus. The increase in LRR with increasing stiffness of the encapsulating layer is attributed to the increase in thermal stress in the encapsulation dielectric stack layer and in the metal lines due to their increased constraint. This stems from the strong adhesion of the encapsulating dielectric material to the metal, thus fixing the loci of the surface planes of the metal, which could result in mechanical damage through voiding, cracking or delamination.
It is also found that the increase in the local SiOH concentration leads to a decrease in the Young's modulus of the encapsulating SiO_2. Thus, the engineering and optimization of the chemistry of the encapsulating dielectric are essential for improved post-packaging burn-in yields.

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1. Introduction

The continued decrease in device feature size has resulted in a shift in circuit performance from being device-dominated to interconnect-dominated [1]. As a result of scaling, global interconnects have become slower due to the increased resistance and capacitance, and the total interconnect length also increases as the complexity of the chip increases. This leads to an increase in interconnect latency (delay) and power consumption [1]. In order to overcome these setbacks, the electronics industry has kept reinventing itself, which resulted in the replacement of the Al/SiO_2 based back-end-of-line (BEOL) system with a Cu/low-k BEOL system [2]. In recent times, further decreases of the dielectric constant of inter-metal dielectrics below 2.0 have been achieved by the use of porous low-k dielectric materials as well as the use of air-gaps [3–5].

However, the reliability of BEOL has remained a continuous challenge. While many field failures of packaged dies are attributable to both metal line and dielectric damage, Pareto analyses of failure modes have shown that damage of the final encapsulation dielectric stack (CAPS) is the overriding failure mode. CAPS damage is known to be a chip–package interaction phenomenon [6]. It is caused by the generation of interfacial shear stresses on the die surface, which is the CAPS layer. The interfacial shear stresses are due to the volumetric shrinkage of the packaging overmould, as well as differences in the coefficient of thermal expansion and elastic moduli properties of the materials as the devices cool down [6,7]. The generated interfacial shear stress is partly sustained by the passivation film as a membrane stress and partly transmitted on the metal lines as a shear stress [7,8].

Additional stresses are generated in the CAPS due to their coupling with metal lines, thereby forming metal-dielectric monoliths. If the stress concentration at the edges of the CAPS layer exceeds its tensile strength, it will result in the formation of cracks [6].

Studies by [9] have also shown that stresses in metal lines are influenced by the stiffness of the CAPS layer used. It has also been shown that the electrical reliability of integrated circuits depends to a large extent on the properties of the used CAPS dielectric. For example, the time-dependent-dielectric-breakdown (TDDB) of metal lines is significantly influenced by the reliability of the cap–metal line interface in a Cu-low-k system [10], while J. S. Huang et al. [11] have also shown that the electromigration lifetimes of metal lines are highly influenced by their proximity to the passivation layer [8].

These studies underscore the need for detailed studies of the impact of dielectrics on the reliability of back-end-of-line (BEOL) structures. In an attempt to understand the essential attributes of the final passivation dielectric stacks and their relationships to electrical failure, we analyzed the historical device fallout rate data at final packaging

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* Corresponding author. Tel.: +1 301 975 8093; fax: +1 301 975 6513.
E-mail address: yaw.obeng@nist.gov (Y.S. Obeng).

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(also regarded as lot rejection rate (LRR)) for Application Specific Integrated Circuits devices. The device LRR data were obtained from four different commercial nano-fabrication sites, each of which had a unique combination of film deposition tools, hence, differences in the properties of the deposited films. The obtained LRR results from the different fabrication facilities were correlated to the mechanical and chemical properties fall out rates of the CAPS.

For this study, the well-known AlCu metallization system was used. However, the results are very applicable, and invaluable, for the Cu/low-K BEOL system. This study was achieved by the application of various analysis tools such as, burn-in tests, nano-indentation, reflectance Fourier transform infrared (FTIR), and ultrasonic laser sonar.

2. Experiment description

Burn-in tests were conducted on product devices after their packaging. The LRR reported in this paper was determined from the post packaging burn-in data, and represents the packaging-induced device failure rates. The devices studied were encapsulated with a stack of SiN on top of SiO_x. Both dielectric materials were deposited by plasma enhanced chemical vapor deposition (PECVD) and annealed in forming gas at 420 °C for 2 hr, as described elsewhere [11].

The mechanical properties (Young's modulus) of the stack dielectric films, were measured by a frequency specific depth-sensing indentation on Nanoindenter® XP (MTS, Oak Ridge, TN) [12]. The experiments were run in 'constant-strain-to-depth' mode. In order to avoid artifacts due to substrate and 'skin' effects, the reported data represent ≈60% of the total film-stack thickness, since our interest is in determining the effective Young's modulus of the passivation dielectric stack, which consists of SiN and SiO_2 layers. The system has load and displacement resolutions of 0.3 μN and 0.16 nm, respectively. The Young's Modulus was estimated following [13]. The reported error bars represent ± three times the standard deviation of twenty one measurements per sample. The measurement sites were programmed during the experimental set up. The reported variability is a composite of within-sample and systematic experimental variabilities. The local mechanical properties of the dielectric thin film were further examined using a picosecond ultrasonic laser sonar. The laser-induced ultrasound measures single or multi-layer thicknesses of product wafers with 0.1 nm accuracy (MetaPULSE 200, Rudloph Technologies, Flanders, NJ) [12].

Since the silicon oxide dielectric film was in direct contact with the metal lines, we closely examined its chemical and mechanical properties. For instance, the within-wafer chemical and mechanical variability of the PECVD oxide films were studied by dicing the 200 mm wafer into 1.5 × 1.5 cm squares, and the squares were labeled with X–Y coordinates to reflect die placements on the tester wafers. These squares were then analyzed individually; the results from the individual dies were then reconstituted into contour plots. Thereafter, the results obtained from the chemical and mechanical analyses of the dielectric thin films were correlated to the lot rejection rate data acquired after burn-in tests.

The chemical composition of the SiO_x layer was determined by the reflectance Fourier transform infrared (FTIR) technique, using a Perkin Elmer Spectrum 2000 FTIR, equipped with a microscope for focusing the IR-beam spot in the 580–4000 cm^{-1} spectral range. A gold mirror was used for the reference, and the spectra were corrected for Si substrate effects. The area under the various peaks of interest was estimated by integration with a Perkin Elmer supplied algorithm. In view of the possibility of various forms of silanol (SiOH), we estimated the relative local concentration of SiOH by integrating over the 2800 cm^{-1} to 4000 cm^{-1} range [14–16].

3. Results

The LRR data for the four different fabrication sites were studied, as shown in Fig. 1. The horizontal line in Fig. 1 represents the grand mean LRR for all the data analyzed, and is included as a reading aid only. Devices from fabrication site A showed a relatively low LRR (<20%), while those from site D showed a much higher failure rate (>50%) in comparison to the other sites. Interestingly, the data from site C showed the worst spread. Overall, the data indicate a systematic interaction between the dielectric properties and the device fall out rates, with site-to-site differences in the composition of the dielectric films. Fig. 2 shows the LRR data from the four different fabrication sites as a function of the Young's modulus data of the bilayer CAPS films, deposited to simulate the processes used by the various fabrication sites. From this figure, with the exception of fabrication site D, it can be observed that there is a strong correlation between the Young's modulus of the CAPS layer and the LRR data. The LRR was observed to increase with an increase in the Young's modulus of the CAPS layer. On the other hand, fabrication site D is observed to show the highest Young's modulus value of about 188 GPa; however, some of its data points are outliers. This observation seems to indicate that the LRR data from site D is influenced by some other factors in addition to the mechanical properties of the CAPS layer.

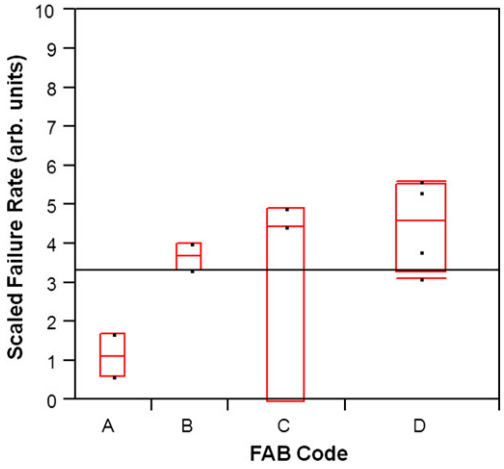

Fig. 1. Lot rejection rate as a function of device fabrication location.

In an effort to understand the underlying reasons for the observed spread in the mechanical and the LRR data, we studied the within-wafer variability of mechanical properties of the proto-typical SiO_x films. Analysis was performed using the picosecond ultrasonic laser sonar to determine changes in sound velocity. Fig. 3 shows the within-wafer variation of sound velocity through a SiO_x encapsulating dielectric film. It shows large inhomogenities in the relative sound

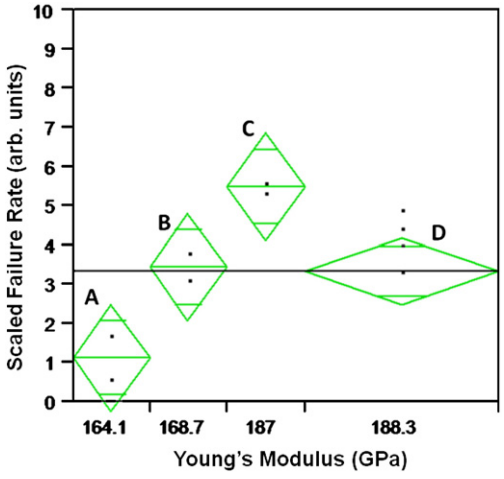

Fig. 2. Lot rejection rate as a function of the effective Young's modulus of the encapsulating dielectric stacks for the four different fabrication sites.

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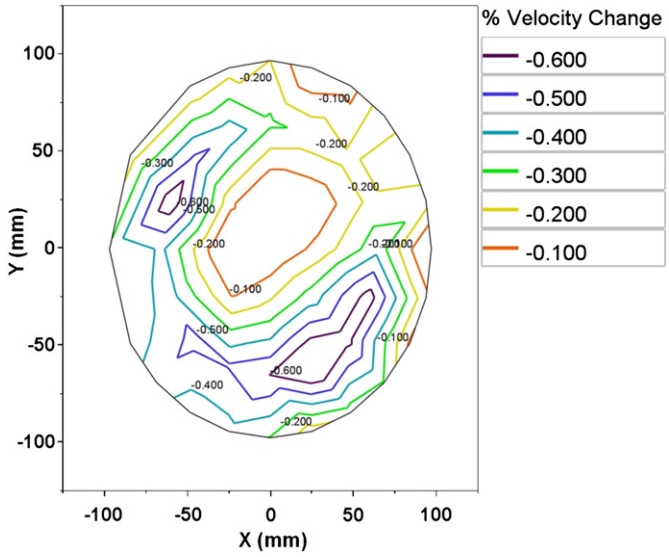

Fig. 3. Composite contour map of the within wafer variation of the change in sound velocity of blanket SiO_x on a 200 mm wafer.

velocity across the wafer, with minimum change in sound velocity observed at the center of the wafer.

In order to further understand the large within-wafer inhomogenities in the sound velocity data as described above, Fourier Transform Infrared Spectroscopy (FTIR) was used to investigate the local chemistry within the SiO_x encapsulating dielectric film, while nano-indentation was used to study the variation in its Young's modulus. For these studies, the same samples as the picoseconds ultrasonic laser experiments were used.

This study was performed on 4 sets of wafers, each consisting of 12 wafers from the four different fabrication sites. Each wafer was diced into 10 samples, thus, the reported data in Fig. 4 is a measurement on 480 samples.

Fig. 4 shows the relationship between local SiOH concentration and the Young's modulus measurement. Each data point is the average variation of the Young's modulus as a function of a given local SiOH concentration. The error bar on each data point represents the variation across wafers and fabrication sites. From this figure, the Young's modulus is observed to decrease with increasing SiOH concentration. This observed variation in Fig. 4 also suggests a within-wafer variation of the Young's modulus of the SiO_x encapsulating dielectric, which is in agreement with the change in sound velocity data in Fig. 3. Clearly, the mechanical properties of the SiO_x film varied across the wafer.

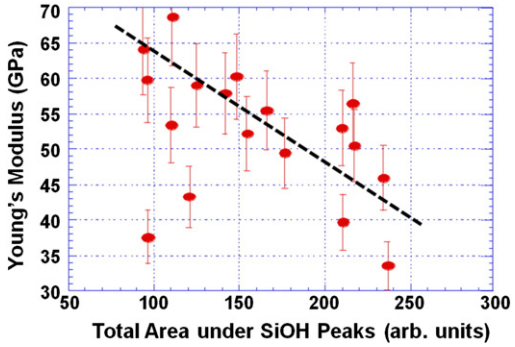

Fig. 4. Correlation of Young's modulus with relative local SiOH concentration from various dies from a typical SiO_2 wafer.

4. Discussion

Based on the various studies performed in Section 3, a correlation can be drawn between LRR data and the chemical and mechanical properties of the CAPS dielectric.

From Figs. 1 and 2 it can be deduced that the LRR and the mechanical properties of the CAPS is site-to-site sensitive. Detailed analysis of variance of the accumulated historical data indicates that the spread in the data is attributable to device layout density and the systematic differences in fabrication protocols from site-to-site, as shown in Fig. 1.

The LRR scaled with the Young's modulus of the CAPS layer, with higher Young's modulus values resulting in increased LRR. For a given device layout, the extent of damage to the upper level metal lines will increase with increasing CAPS stiffness. This implies that the device failure depends on the mechanical properties of the CAPS dielectrics. This is because, higher Young's modulus of the CAPS layer results in the increase in the built up thermal stress in the CAPS layer, since Young's modulus is directly proportional to stress. In turn, higher thermal stresses are induced in the upper metal line as it forms a metal-dielectric monolithic, resulting from its coupling to the CAPS layer.

Additionally, its increased constrain caused by the increase in the stiffness of the CAPS layer, leads to higher stress build up in the metal line. This could lead to the observed increase in device failure rate (Fig. 2) with the increase in CAPS layer Young's modulus. This is in agreement with the open literature [9].

From Fig. 3, it is observed that the mechanical property of the CAPS layer is inhomogeneous across wafer. This implies that the LRR rate of the devices is anticipated to be dependent on the origin/coordinates of particular dies on the wafer. Additionally, from this analysis and the dependence of LRR on CAPS mechanical properties, it is apparent that we could use the effective Young's modulus to reasonably predict lot failure probabilities.

Fig. 4 shows that an increase in the local SiOH concentration results in a decrease in Young's modulus. This is anticipated since the non-bridging SiOH disrupts the silica network, which results in the decrease in Young's modulus with increasing SiOH concentration [17]. The observation that a decrease in the stiffness of the CAPS layer will reduce post-packaging device failure rates (Fig. 2), suggests that it may be desirable to increase the SiOH concentration in the CAPS films, thus, decrease its Young's modulus. This will result in a decrease in the thermal stress in the CAPS layer, as it also becomes more compliant. Therefore, the upper metal lines have more freedom to deform, thereby relieving built up stresses, in contrast to higher Young's modulus CAPS layer. This could reduce the LRR observed after post-packaging burn-in tests (Fig. 2).

This is supported by the studies done by R. Hofman et al. [18], in which the presence of SiOH was found to reduce the susceptibility of SiO_2 to cracking and delamination by lowering the activation energy of stress relaxation. On the other hand, it has been shown elsewhere that high local concentrations of SiOH in the CAPS dielectric may be detrimental to the electromigration lifetimes of AlCu-W metallization schemes [19]. Thus, care must be exercised in optimizing the SiOH content of the CAPS dielectrics to accommodate the competing effects. Therefore, a good understanding of materials interactions (based on chemical and mechanical properties) will be beneficial in the development of more reliable electronic devices.

5. Conclusions

In this work, the role of CAPS dielectric on the reliability of metal lines is investigated. The consequences of the interaction between the dielectrics and metal stacks on the reliability of the IC devices are illustrated with the correlation between lot rejection rate at burn-in and the mechanical properties of the used CAPS layer. There is a strong dependence of LRR on the effective Young's modulus of

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the CAPS layer, as the LRR is found to increase with increasing Young's modulus. This is because stiff CAPS dielectrics generate a significant increase in thermal stress within the metal lines due to their increased constrain, limiting their ability to relieve thermal stresses. This inability stems from the strong adhesion of CAPS material to the metal, thus fixing the loci of the surface planes of the metal. Moreover, a higher concentration of SiOH in the SiO_x CAPS dielectric is found to reduce its Young's modulus, thus its stiffness. Therefore, the effective Young's modulus of the CAPS dielectric must be optimized as to maximize post packaging burn-in yields.

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