More than Moore or More Moore: a SWOT analysis*

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Abstract. Over the last decade, the world of semiconductors has broadened its horizon from More Moore and beyond conventional scaling to More than Moore. Some first hypothesized the end of Moore's law and the beginning of a new era. They saw it as an OR gate while others saw it as a NOR gate. Since then it has been an AND gate as Moore's law has continued to move down its persistent scaling path. Even if it fades, i.e., the end of More Moore, both technologies will flourish. The reason is that More than Moore is complementary to traditional semiconductor technology. More than Moore is a functional diversification incorporating functionalities that are more than digital and analog signals and architectures used in conventional semiconductors. More than Moore product definitions include MEMS, which integrate microelectronics with micromechanical structures that are scaled versions of larger mechanical structures via semiconductor processing techniques, as well as 3D packaging, LEDs, and Photovoltaic cells depending on the source. In the future there are NEMS, or Nano-Electrical-Mechanical-Systems. In all cases the use of manufacturing methods and metrology evolved from semiconductors. Metrology is critical to all these technologies, because to make something, you must be able to measure it, and to do that you must be able to see it.

This paper examines the Strengths, Weaknesses, Opportunities and Threats (SWOT) for both classical semiconductor markets and the subset of emergent technologies that includes 3D packaging, LEDs, photovoltaic cells, and MEMS/NEMS. It delves into how these technologies are evolving and the economic impact of this evolution. It addresses such questions as:

- Is scaling measurably slowing?
- Are design costs getting too high?
- What are the critical factors for a Moore's Wall scenario?
- As chips become an ever big-player game, will there be enough research centers to support measurements and associated standards development.
- How fragmented is the More than Moore Market?
- Will they cross the valley of death from MEMS to Bioelectronics?

Keywords: semiconductors, Moore's law, More than Moore, More Moore, SWOT analysis, scaling trends, MEMS, NEMS, 3D packaging, bioelectronics, emergent technologies, measurements, standards.
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INTRODUCTION

Moore's Law is based on Gordon Moore's observation in 1965[1] that there had been a doubling of components-per-chip for roughly the same areal cost every year (later revised by him to every two years in 1975[2])[1] as a result of lithographic scaling.

People have been predicting the demise of Moore's Law since the sixties. Even Gordon Moore himself originally saw it as mostly a "near-term" phenomenon and has questioned its future several times. One of the biggest fears was that lithography would hit physical limits and scaling would end as a result. As the seventies came to a close, many experts saw the one-micron barrier looming as Rayleigh's limit, and the optical technology of the day seemed an impenetrable wall. By the nineties several leading technologists felt gate oxides would not allow scaling below 0.25 micrometers. Fortunately for one of the authors, GDH, the dire predictions of a Moore's Wall in the nineties led to a first commission by Scientific American [2] to write a more positive perspective as to what would happen. Yet again, leading nanotechnologists were predicting the end of Moore's Law by the early 2000's because of lithographic limitations and wafer fabs becoming too expensive. This led to a second Scientific American [3] paper. The positive outlook for Moore's Law in both papers was based on the observation that technologists had systematically torn down these seemingly impenetrable walls with new discoveries and that it could be expected to continue as a result of sheer human will. In other words, it was a 'we'll think of something strategy' for believing that the Law would continue on unchecked. In fact, it became so critical that we identify these barriers early on, that Robert Doering inserted drawings of red brick walls into ITRS roadmap line items at points where 'no known solution existed. This visual greatly aided the industry by focusing its development resources on the technologies most critical to keeping Moore's Law going. At this writing, Moore's Law has survived 46 years and is clearly positioned to easily pass its golden anniversary.[2] [4]

So, it is time to take another look into just what are the strengths, weaknesses, opportunities, and threats to more of Moore's Law and do the same for More than Moore as well as attempt to pin down a less fluid definition of them.

MORE MOORE

More Moore is a term popularized by Europeans in the last decade to wrap up in a sound bite the concepts in the titles of Moore's two papers. In the first "No Exponential is Forever,"[5] an unpublished keynote presentation given at the 1993 VLSI Multilevel Interconnection Conference, Moore expressed doubts that the Law could continue. In the second "But Forever can be Delayed,"[6] he was surprised by the degree to which technologists had systematically torn down seemingly impenetrable 'red brick walls.'[3] More Moore embodies the idea that the coming of Moore's Wall is unpredictable.

Over time, Moore's Law has taken on additional contextual weight, as people have discovered other methods to achieve Moore's original vision. Within these, contributors to the International Technology Roadmap for Semiconductors use the following definition for **More Moore:[**15]

More Moore is scaling. There are four types of scaling being pursued today that offer the potential of continuing to reduce cost per function:

1) *Geometrical Scaling* at constant field refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density, cost per function reduction, and performance (speed, power, durability, and reliability) values for the applications needed by end customers.

2) *Design Equivalent Scaling* refers to design technologies that enable high performance, low power, high reliability, long durability, low cost, and high design productivity. It occurs in conjunction with equivalent scaling and continued geometric scaling.

3) *Equivalent Scaling* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip. It

[1] There are many false references to Moore's clock period being every 18 months. However, according to Moore in conversations with one of the authors, GDH, and in his 1994 SIA Noyce Award acceptance speech, he never said this, that it was a fabrication of Intel's public relations department which took an average of both papers.

[2] For more on the history and economics of Moore's Law, see H.R. Huff and D.C. Gilmer, *High Dielectric Constant Materials*, Chapt. 1

[3] Red Brick Wall is a simile created by Robert Doering. It was first used by him during an ITRS committee meeting in the early nineties, where he placed red brick wall drawings at various places on roadmap charts to visually draw attention to points in the future where there was no known solution for a particular technology requirement. These were proverbial "for want of a nail" items needed before the node scheduled for that point in time could go to manufacturing.

occurs in conjunction with, and also enables, continued geometrical scaling.

4) *'Beyond CMOS'* refers to emerging research devices that are focused on a "new switch" used to process primarily digital information. They typically exploit a new state variable to provide functional scaling substantially beyond that ultimately attainable with CMOS. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions. Some examples of Beyond CMOS are: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switches, and NEMS switches.

Depending on the source, Beyond CMOS is sometimes also put with More than Moore, and even on its own. We believe it is really More Moore for three reasons: first, Moore's papers only identified lithographic scaling as the driver of more components per given area of substrate. CMOS didn't exist yet. ICs were mostly bipolar with PMOS and NMOS just emerging. CMOS would not become a significant part of driving Moore's Law until the eighties, when power issues began to limit the advance of Moore's Law. Because Since CMOS is beyond NMOS, which is beyond bipolar, Beyond CMOS logically belongs with Moore More.

Second, Beyond CMOS technologies do add more components per given area of substrate, which is clearly More Moore. One could argue that it's a different state mechanism, but Moore never stipulated state as a part of Moore's Law. He didn't even use the term transistors. Instead he used the term components.

Third, the industry's addition of Design Equivalent Scaling and Equivalent Scaling alters Moore's definition significantly because neither adds more components per given area. The addition of Design Equivalent Scaling hinged on another marketing shift that noted computing performance was rising in addition to components. This was certainly a user benefit and it could be affected by design alone. Equivalent Scaling solves leakage and power dissipation red brick walls. In both cases, More Moore becomes more about improving computing power than the simple addition of components for little cost. Since Beyond CMOS does both, it logically belongs in More Moore. Otherwise, the Equivalents and many more things get thrown into More than Moore, and the distinction loses relevance.

Finally, stating that Beyond CMOS is *Not* More Moore entails a logical problem that if there is More Moore and Moore than Moore, then there can only be Less than Moore of which, Not Moore is a subset. Most of the world is Less than Moore. For example most of the industrial age products follow a learning curve, but not Moore's Law. Analog, power, and discretes are also not affected by scaling and thus are Less than Moore. But because Beyond CMOS is clearly about more components and more computing performance, it belongs in More Moore.

Strengths of More Moore

Solved for cost, Moore's Law states that price per transistor will steadily decline. In fact, it has declined 9 orders of magnitude since 1954. Moreover, it actually accelerated after the ITRS roadmap came into being.

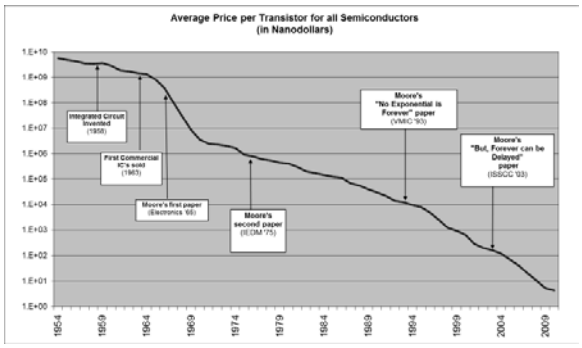

FIGURE 1. Average price per transistor has declined 9 orders of magnitude since 1954. (Reproduced by permission from GDH.)

Enabling decreasing cost per function is the key strength of Moore's Law. It is what made it so powerful over time. What makes it possible is scaling and what makes scaling possible is steady innovation. While there is no scientific law behind the history of continued innovation, there is plenty of statistical evidence that it does come and thus can be expected to come with regularity.[1]

The shrinkonomics behind scaling are quite simple. If a chip maker can shrink the size of the components in a design, chip size gets smaller. If chip size gets smaller, then there are more chips per wafer. Since the wafer cost is similar, it costs less to make each die. Moreover, die yields are also higher because die sizes are smaller. It also means a chip maker doesn't have to build more capacity.

A second strength of Moore's Law is the social feedback loop which makes it a self-fulfilling prophecy. Scaling makes sense from many different angles, which drives technologists to pursue this path and financiers to fund them. Success with each node

reinforces the effort, causing companies and technologists to pursue the next node even harder. The result is that funding and the number of people working to further shrinkonomics has steadily grown and is far larger than what gets spent on More Than Moore.

Weaknesses

The fundamental weakness of Moore's Law lies in the shrinkonomics, which largely happen due to systematic improvements in lithography. Without these, Moore's Law stops.

Some have believed that the increasing price of lithography tools over the years would stop it. The first litho tools only cost ten cents each. They were camel hair brushes, with which operators painted on hot wax for the resist. At this writing, the most expensive tools cost more than $100M each. These costs have steadily risen over the decades while price per transistor has fallen, as depicted in figure 2.

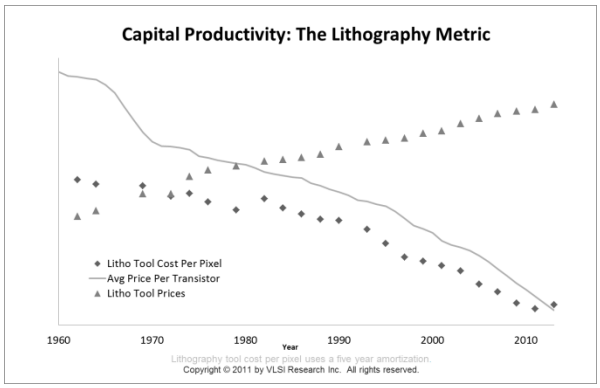

FIGURE 2. Average price per transistor has declined 9 orders of magnitude since 1954. (Reproduced by permission from GDH.)

Litho tool price increases have not been a problem because the cost per pixel exposed has fallen, following the price per transistor. If this does not continue, the main driving force behind Moore's Law breaks down. VLSI Research's models now show that may well happen with Extreme Ultraviolet (EUV). When EUV is first applied, it will be more expensive on a cost-per-pixel basis than previous nodes.

Opportunities

The alternative of adding more immersion exposures per mask layer is also more expensive. This has happened before with each new lithographic technology introduction. In these cases, significant technical breakthroughs were made in the following node to put the industry back on its lithographic cost curve.

Another scaling alternative might be a direct write strategy using electron or ion beams. However, the economics of direct write do not make it Moore's Law compliant.[8] Or as others have proposed, printed nanoelectronics based on nanoparticle technologies is another opportunity. Moreover, these nanoparticle technologies for printed electronics use the word nano loosely, as the printed electronics structures are in the micrometer realm. See for example

http://www.ltnt.ethz.ch/projects/2011_Schneider2.pdf

Thus, a key opportunity for More Moore is to make sure that the engineering developments needed to make EUV successful exist. Failing to do so is its biggest threat.

Material and electrical limitations are other perceived weaknesses of Moore's Law. When these fail, Dennard's scaling rules break down.[9] For example, when gate oxides could no longer be made any thinner, leakage soared. However, material limitations have been steadily overcome as well. New materials such as Oxy-Nitrides and High-K dielectrics for gates; Germanium stress layers and Metal Gate for channel mobility; and Copper and Low-K dielectrics for interconnect have systematically appeared due to materials engineering breakthroughs. The ultimate materials limit will be when film thicknesses of one atom are reached. While this is still far away, no one has yet figured out how to make films that are thinner than a single atom. However, we have figured out how to make them electrically thinner, with materials like Hafnium-oxide for the gate dielectric. This shows that the world that the electron sees is far more important than the material world.

Threats

Finally, one of the most critical threats to More Moore is the failure of metrology to continue to be able to measure within a tenth the dimensions of what is being made. Over the years, we have come to believe it is a fundamental law of economics that if something can't be measured, it can't be manufactured. It's never been violated in any observation that I know of. It may be possible to make something without measuring it, such as fine art. But without metrology, nothing can be manufactured in volume with repeatability, yield, and thus, cost effectiveness.

Therefore, the economic value of Moore's Law would be lost without coincident improvements in metrology. On the surface, that makes metrology a key opportunity. However, because the market for metrology is relatively small it often does not have the profit scale to justify high dollar research into future technologies. This is especially true of mask making, where the need for measurement and inspection tools could cause EUV to fail and yet the funding to develop these tools is lacking. Billions have been invested in EUV to get it to this point and yet its future hinges on the proverbial want of a nail.

MORE THAN MOORE

More Than Moore (MTM) is a term popularized by Europeans in the last decade to wrap up in a sound bite the concepts of new offshoots in technology that either 1) extend the benefits of Moore's Law without scaling (this is generally referred to as advanced packaging) or 2) create entirely new value chains using the same technology developed for Moore's Law. MEMS, solid-state lighting, and photovoltaic solar cells are generally considered More Than Moore class technologies.

It became popularized outside of Europe when Nanotechnology faltered as a name for these markets. Nanotechnology was popularized by U.S. academics as a future replacement for conventional semiconductors. They had extrapolated fab costs from dated data to conclude semiconductors could never make the transition from microchips greater than 100 nm to nanochips with dimensions less than that. It worked well for grant trolling until Intel became the first to manufacture chips below 100 nm in 2003.[10] It was at that point that the term nanotechnology began to fall back in popular consciousness and became displaced by MTM. Proponents of nanotechnology had thought More Moore would never make it past 100 nm due to scaling limits and erroneous assumptions about the cost of fabs. So, with semiconductors having passed below 100 nm in production, they could now claim ownership of the term.

More than Moore is a functional diversification of semiconductor manufacturing and process technology. The best examples are sensors, actuators, and similar MEMS devices. They also do not scale, which fits the view of More than Moore being the incorporation of devices that do not scale in a manner similar to that of "Moore's Law."

However, many things do not scale that would not be considered More than Moore, while some technologies, such as 3D packaging do scale. So lack of scaling does not adequately define More than Moore.

More than Moore technologies have to add value for the end customer in different ways, otherwise they would not be salable. Some view More-than-Moore as being made up of non-digital applications, such as RF and analog/mixed-signal technologies for communication, power control, passive components, which with the exception of antenna, are all conventional semiconductor technologies that have been around for decades. This is also true for particular package-level (SIP/MCP) or chip-level (SoC) solutions that sometimes get lumped into More than Moore. Most of these are Less than Moore, because they do not scale and are not new functionalities. The exception is mixed-signal. It belongs with More Moore due to its heavy reliance on digital signal processing and embedded processors; it does scale and relies on increasing complexity.

Finally, most do agree that 3D packaging is a More than Moore technology as well because of the new functionalities. One could argue that 3D packaging is not so much a new functionality as it is a new technology that enables greater integration and thus belongs with More Moore. However, it is more a packaging technology, and because it is relatively new, it can't be placed logically with Less than Moore.

Like More Moore, More Than Moore has been around for decades. In the case of advanced packaging, the first instance is Jack Kilby's integrated circuit. When Robert Noyce's IC superseded it with lithographic interconnections, Kilby's IC, based on single transistors wire bonded together, became known as the hybrid IC. Later, IBM would invent its C4 process for interconnecting chips together on a single substrate.

As the term 'hybrid IC' aged, it morphed into Multi-Chip-Module (MCM) in the eighties. This was largely for marketing purposes, as large electronics companies wanted to spin-out their in-house hybrid operations to private investors. As these failed in the open sub-con market, the same concepts were quietly adopted by IDM (Integrated Device Manufacturer) chip makers. The term morphed into MCP or SIP (Multi-Chip-Package and System-In-a-Package, the latter a misnomer because it is still rare to see an entire system electronics in a single package). Neither term became popular because customers still only saw a single chip when they bought either an MCM or a classical single IC in a package.

Marketing has as much to do with the evolution of what we call these technologies as does the evolution of the actual technologies. So today we have the term advanced packaging replacing MCP. It gives the originally ill-defined More-Than-Moore crowd something to hang their hat on that sounds different. It also makes some technical sense, because under the covers there are several combinations of technologies to be found in advanced packaging: wire bonding, flip chip, Stacked Die, and TSV (Through-Silicon-Via) for example.

Strengths of More than Moore

More importantly, these technologies are coming into their own because they solve real technical problems with More Moore approaches.

The greatest strengths of MTM for advanced packaging at the IC level are in power distribution, faster memory access, smaller size, and lower vertical costs in the case of mixed process technology.

The most commonly used are lower vertical cost and smaller size. These go hand in hand, because More Moore also solves cost and size problems. However, it only does it on the horizontal plane of the device. If the device requires radically different process technologies, the additional vertical cost of putting both on the same wafer can be greater than the horizontal savings and the elimination of a second package.

Flash memory is a classic example, because flash needs both a flash process and a plain CMOS logic process for the controller. Merge them into a single device and more mask levels are needed than for processing each on separate wafers. Plus, there is a savings from not having a redundant logic masking for the flash area of the chip and vice versa. In the case of flash, it is also possible to stack the controller on top of the memory, substantially reducing the chip's footprint on the board. You can even stack multiple flash memory chips for yield reasons and put a single microcontroller on top, further reducing footprint. This is why MCPs with stacked die became so popular early on in flash memory.

Turning to the creation of new value chains, using the same technology developed for Moore's Law is no threat to More Moore. In fact, it is very complementary. MEMS, solid-state lighting, and photovoltaic solar cells all drive demand for more semiconductors while they open up new applications for them.

After decades of being in electronics, solid-state lighting (LEDs) and photovoltaic solar cells are drawing semiconductors more into the realm of energy and its conservation. Moreover, they have become important markets in and of themselves.

The Solar PV market passed $25B in 2010. It has been growing at a 34 % compound annual rate since 2006. Equipment sales to PV cell and module manufacturers were north of $5B. Solar offers a critical solution to carbon emissions and climate change issues. More importantly, photovoltaics have been on their own Moore's-Law-like curve, as cell efficiencies have steadily increased with time.[12]

LEDs were a $6.6B market in 2010 and growing 17 % per annum. They are seen by many as a way to save energy due to the greater efficiency of LED lights over incandescent bulbs.[13]

MEMS reached $6.9B in 2010, jumping 45 % as the automotive market resurged. The companies leading this segment are very familiar to many, including HP, TI, Robert Bosch, STM, and Canon to name a few. The first MEMS applications were Ink Jet Heads for printers and Accelerometers for airbags. These, gyroscopes, RF, and pressure sensors are currently the largest markets.

Weaknesses

One weakness in the advanced packaging approach is that final test yields have to be closely balanced with wafer probe yields. Otherwise, a 3D or even a multi-chip package can be more expensive than a traditional More Moore approach. This is largely why Kilby's IC was displaced by Noyce's. At this point, there is no threat to using advanced packaging whenever performance, size, and cost present an opportunity.

In contrast, using TSV technology offers the primary benefit of faster access to memory, which makes a processor run faster, as well as better power distribution between chips. However, its primary weaknesses are excessive cost, mechanical test issues, and lack of an EDA (Electronic Design Automation) infrastructure to support its use. These are steadily being overcome, but they limit TSV applications to high-end cost-insensitive markets at this writing.

A critical threat to advanced packaging is that technological leaps often provide only one time cost gains. There is no similar technology driven cost reduction model for it like there is with shrinkonomics.

With More Moore, a shrink doubles the transistors on a piece of silicon for around a 30 % rise in processing cost. But more transistors tend to lead to more I/O pins due to Rent's rule. [11] With packaging, costs are more closely tied with pins with a systematic reduction rate of slightly less than 5 % per node. So, fractional pennies of cost reductions per pin are seldom offset by the increase in pins.

The gains from packaging are seldom measured in orders of magnitude. They are hard-fought gains made either in negotiation or manufacturing. For example, wire bonders use to cost $80K to $100K and are now in the $40K to $50K range. The biggest reduction in cost came from the switch to copper wire from gold. This is a onetime gain than took more than 30 years of engineering effort to pull off.

Opportunities

MEMS are becoming ubiquitous as they move from automotive and printer applications to games, cell phones, tablets, and even medical devices. For the most part, MEMS are the sensory system for electronics, making ordinary electronics systems much more valuable. They put the 'wee' in the Nintendo Wii. With this comes a level of maturity in which it becomes clearer how these markets are driven and the underlying technical and economic factors that make it possible.

The great diversity of More than Moore applications presents multiple opportunities for industry-wide technology roadmaps to establish agreements and priorities for pre-competitive direction that leads to more efficient commercial success as well as job creation. For this to occur, six pre-existing conditions [16] are needed for the successful implementation of industry-wide technology roadmaps:

1) Market potential for the technology is large and mature enough to justify pre-competitive roadmapping efforts.
2) A community of industry leaders that believe the full potential of the technology can be better achieved (i.e., more cost effectively) by working together to align the supply chain towards a common vision.
3) Leaders must see themselves as stakeholders, which is testable by their willingness to provide resources for roadmapping.
4) These stakeholders are willing to share by contributing not just resources but also knowledge to the roadmapping process.
5) A manageable set of commonly used driver variables with vectors of improvement that can be used as measures of progress in the adjacent and complementary technologies that drive the industry.
6) A process for generating consensus of opinion on expected progress and timing needed for critical milestones to be met among a majority of the stakeholders.

When these six conditions are met, roadmapping presents the opportunity of accelerating technical development with more efficient use of resources. But, when one or more of them are not met, roadmapping efforts will not move forward.

Threats

While MEMS have been wildly successful with simplistic mechanical functions, the two-decade-old hopes that MEMS would develop into micro- and even nano-robots is still more science fiction than fact.[14] While many of these products show great promise, such as tissue repair nanobots – a medical MtM application, the best are still relatively small markets-wise and many are in the development phases or only exist as artists' conceptions.

Other threats are that packaging and testing costs for many MEMS products can account for two-thirds of the total cost[17] versus a tenth for conventional MtM products. And for some applications, such as medical/biological applications, biocompatibility and reliability are considerable challenges. Regional regulation adds an additional risk and management factor to business operations.

Another threat is that so much of More than Moore is either ill-defined or subject to marketing and grant-trolling abuse. Thus, the term could fall prey to the same forces that took the term nanotechnology down. However nanotechnology was limited to manufacturing below 100 nm, which was very specific. In the case of More than Moore, it is highly balkanized and more an ideology than a single market or technology. Each of the technologies that are contained in More than Moore can subsist alone without the term.

The great diversity of MtM technologies leads to the threat that any given MtM approach will not be able to capture adequate resources. Without cross-

platform roadmapping to direct resources, resources will be spread so thin that many deserving technologies will never achieve the breakaway energy needed for commercialization.

CONCLUSIONS

We summarize our answers to the questions presented in the abstract.

- Is scaling measurably slowing? - *No, as shown early on, scaling continues to proceed on a predictable two-year cadence. While EUV looks problematic, multi-exposure immersion is already proving to get the industry down to 22 nm.*
- Are design costs getting too high? –*Yes and no. Yes they have been getting higher, but they have proven manageable. While there wasn't enough time to fully address it here, predictions that design costs would be a red-brick wall that first emerged at 350 nm have not proven out. This is even true for smaller companies. In fact, more fabless design houses exist today than did all chip companies at 350 nm.*
- What are the critical factors for a 'red brick wall' scenario? – *Lack of adequate knowledge and resources is the biggest threat that the industry will unknowingly run into a 'red brick wall.' As Robert Noyce once said, "knowing there is a problem is 90% of the solution." So far, the ITRS roadmap has correctly identified the red-brick walls and aligned the resources to systematically either remove them or route around them.*
- As chips become an ever big-player game, will there be enough research centers to support measurements and associated standards development. – *So far this has not been the case.*
- How fragmented is the More than Moore Market? - *Extremely, but that is a great opportunity.*
- Who are the leading players? *The Top 5 MEMS players are TI, HP, Bosch, STM, and Panasonic and none are over $1B in size.*[18] *There are consortia members like MIG, for RF and AMS there are RFMD, IBM, Intel, Siemens, Infineon, and the list goes on and on.*
- Will they cross the valley of death from MEMS to Bioelectronics? – *Some already have: Pressure monitors and microfluidics are viable markets today. Drug delivery, in vitro diagnostics, food control are emergent.*

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