Graphene: materials to devices

J. Chae[2], J. Ha[1,2], H. Baek[1], Y. Kuk[1*], S. Y. Jung[2], Y. J. Song[2], N. B. Zhitenev[2], J. A. Stroscio[2], S. J. Woo[3], Y.-W. Son[3]

[1]Department of physics and astronomy, Seoul National University, Seoul 151-747, Korea, [2]Center for Nanoscale Science and Technology, National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, MD 20988, USA, [3]School of computational Sciences, Korea Institute of Advanced Studies, Dongdaemoon-gu, Seoul, 130-722, Korea

Despite recent progress in understanding geometric structure, electronic structure, and transport properties in a graphene device (GD), role of point defects, edges, traps in a GD or a gate insulator has been poorly defined. We have studied electronic and geometric structures of these defects using scanning probe microscopy and try to link those with the transport properties of the GD. We perform scanning gate microscopy study to understand the local carrier scattering. It was found that geometric corrugations, defects and edges directly influence the local transport current. This observation is linked directly with a proposed scattering model based on macroscopic transport measurements. We suggest that dangling bonds in insulator-material SiO_2 mainly used in GDs produce charge puddles and they work as scattering centers.

* Correspondence should be made to: Young Kuk, Tel.: +82-2-880-5444, fax: +82-2-873-7039, e-mail address: ykuk@phya.snu.ac.kr.

Graphene has been widely studied due to scientific interests and its possible application to high-speed devices[1-4]. A single graphene was first isolated mechanically[2] in 2004 and a large-scale graphene layer can now be grown by chemical vapor deposition (CVD) method. Graphene has many unique physical properties, such as its linear dispersion relationship in the electronic band structure near the Dirac point, relativistic fermionic behavior in the conduction and the valence bands, two-dimensional electron gas (2DEG) behavior, and back-scatteringless tunneling[5-9]. These theoretical predictions have been confirmed by macroscopic transport measurements[2,3,10]. However, nature of defects and their role in the carrier scattering is not fully understood with a microscopic picture. For example, the mobility of graphene measured in a suspended graphene device (GD) is reportedly as high as 200,000 cm/V•s[11-16], while that in a GD fabricated on a SiO_2 substrate is only in the range of 5,000~10,000 cm/V•s[17-19]. The difference is explained by the carrier scattering by various defects in the GD or at the interface between the GD and the SiO_2 substrate. In this study we report scanning probe microscopy study of defects and try to correlate them with the carrier scattering model.

Two custom-made atomic force microscopes (AFMs), one under argon-filled, ambient-pressure at room temperature and the other under ultrahigh vacuum (UHV) at a cryogenic temperature[20], and a UHV scanning tunneling microscope (STM) at a cryogenic temperature were used in this study. The UHV AFM or UHV STM head has a rigid three-column structure inside a UHV chamber, and the chamber is immersed in a liquid-helium Dewar and cooled by the helium exchange gas (at nearly one atmospheric pressure) to ensure optimal thermal and vibrational stability. In the AFM system, an objective and zooming lenses and a CCD detector are used to operate the optics as a long-range optical microscope. With this optics, a micron size GD can be aligned under the AFM cantilever using custom-made vacuum motors. For scanning gate microscopy (SGM) operation, the cryogenic AFM was used; the transport current is measured through two electrodes, source and drain, during AFM

operation. We can map spatially-varying, modified-transport current with a tip gating bias at the same site where AFM topography is taken. On top of a scattering center, the transport current may change more than defect-free area as a bias is applied to the site. Therefore we can obtain local transport information with SGM. A typical total conductance value without the tip gate is ~ 100 μS whereas the variation in the conductance with the tip gate is ~ 1 μS.

GDs used in this study were fabricated as reported earlier[4]. Mechanically exfoliated or chemical vapor deposition graphenes were used to fabricate GDs. For comparison, monolayer graphenes were transferred onto three different substrates, a SiC substrate, a thermally grown 300-nm thick SiO_2 and a 300-nm thick SiN_x on a highly doped Si substrate, that were used as back gates later. A single layer of graphene was confirmed via image contrast of an optical microscope and micro-Raman spectroscopy. Source-drain metal (3 nm Cr / 30 nm Au) contacts were defined by conventional electron beam lithography and a lift-off process to fabricate a GD. For GD, a macroscopic transport measurement was performed to check the device characteristics, including the position of the Dirac point, the electron and hole mobility. A sample couldbe annealed with current through a device or annealing of the whole chamber could be accomplished at an elevated temperature inside STM or AFM chambers.

Figures 1a, 1b and 1c show AFM images and a schematic illustration of a fabricated GD with metallic contacts. The corrugation is smaller on top of the GD than on top of SiO_2 substrate. The average corrugation on the GD is ~ 0.7 nm with the characteristic width of few tenth of nanometer as shown in Fig. 1b. As we measured three different graphene layers on SiC, SiO_2 and SiN_x with STM, the STM images are quite similar; they show a honeycomb structure with similar corrugation as shown Figs. 2a, 2b and 2c. The corrugation is smallest on SiC surface and largest on SiO_2. There can be more geometrical defects on a SiO_2 surface, or this corrugation may be originated from dangling bonds at the interface and it may act as scattering centers in a GD. In an annealed sample, the Dirac points initially move upon

annealing but it does not move with additional annealing. The initial movement may be due to desorption of weakly bound water molecules on graphene, but defects created by dangling bonds may not be cured with additional annealing. This result is quite consistent with earlier scanning tunneling spectroscopy results[21].

Ando predicted unique characteristics of transport through a perfect GD only with short-range scatters[22]; the conductivity should not depend on the carrier density because the scattering rate would be divergent as the carrier density goes to zero near the Dirac point. As the long-range scatters would be dominant in the low-density limit, the GD becomes insulating at the Dirac point. Unlike this prediction, it was found that the conductivity is linearly dependent on the charge density induced by the back gate bias[2,3], suggesting that the long-range scatters are dominant in the GD transport. In addition, the carrier transport would be affected by scattering with charged impurities, short-range scatterers, mid-gap states, various phonon modes, surface corrugations, and defects in a GD[17-19, 23-27]. In the case of the charged impurity potential at a high carrier density limit, the conductance is linearly dependent on the induced charge density[17] as that was confirmed by recent experiment in a potassium doped GD[25, 28].

Mapping charge puddles in a GD was pursued by many groups using scanning probe microscopy. That was first demonstrated in a GD fabricated on top of a SiO_2 substrate using a scanning single-electron transistor microscope[29]. That experimental result showed good agreement with a theoretically predicted transport property near the Dirac point[30]. More recently, spatially resolved charge impurities were mapped using a spatial map in scanning tunneling spectroscopy (STS). In that study, the Dirac point was locally mapped from STS data and the charge puddle was mapped with scattering centers [20].

In order to understand the correlation between geometric or electronic defects and local transport property, we performed scanning gate microscopy study on a GD. After a GD on

top of SiO_2 was installed in a cryogenic AFM-SGM chamber, it was imaged in AFM mode. After the corrugation was confirmed by AFM topography, SGM experiments were conducted. Figure 3a depicts a 450 x 450 nm AFM topography of a GD and Figs. 3b-g show SGM micrographs from a tip bias voltage range of –2.5, -2.0, -1.5, 2.5, 2.0, 1.5 V. The Dirac point of this GD was –24 V, as set by the back gate bias. All of the SGM measurements were taken at Dirac point by back-gating. Corrugations on graphene surface can be seen in topography image with lateral dimension of ~100 nm. The spatial variations of conductance change become more prominent as the absolute value of the tip gate bias increases in either negative or positive polarity. Negative (positive) polarity of electric field from the tip is related to the scattering dynamics of electron (hole) carriers. The small features in the SGM data are tens of nanometers, revealing good agreement with the AFM observation. There is strong correlation between the SGM signal and the topographic corrugations; the SGM peaks, indicated by arrows appear at the bottom of the valley in topography. This indicates excess electron puddle appears at the bottom of geometrical corrugation. The SGM peaks, indicated by arrows, appeared at positive bias, indicating hole puddles surround the electron puddles. The range of hole carrier puddles is extended more than that of electron carrier puddles at the same electric field strength. This difference is mainly due to the structure of charge puddle. The correlation between topographic data and SGM data implies that the charge puddles exist at the bottom of each ripple. The difference features in electron and hole carriers indicates that electrons are more locally confined at the bottom of the ripple induced by the interaction with substrate and hole carrier screens around confined electrons. From these results, we can clearly see charged puddles are main scattering center in a GD on SiO_2 layer. In a GD on SiN_x layer, the similar charge puddles could not be imaged in SGM.

In conclusion, we show electron puddles are formed around dangling bonds on a SiO_2 substrate and hole puddles screen around the electron puddle. These puddles may work as

carrier scattering centers in a GD. We acknowledge this work was supported by National Research Foundation (NRF- 2006-0093847) and (NRF-2010-00349).

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Figure Captions

Fig. 1: (a) AFM topography of a GD measured in non-contact mode. (b) An AFM topography in non-contact mode. Maximum vertical corrugation is ~ 1nm. The scale bars indicate 1 μm (a) and 50 nm (b), respectively. (c) A schematic illustration of a graphene device.

Fig. 2: STM images of CVD grown graphenes transferred on (a) SiC, (b) SiO_2 and (c) SiN_x. The scales bars indicate 2 nm in (a) and (b), 1 nm in (c).

Fig. 3: (a) An AFM topography of 450 x 450 nm area on a GD. (b)-(g) SGM data on the same area at tip gating bias of −2.5 V, −2.0 V, −1.5 V, 2.5 V, 2.0 V and 1.5 V respectively.

Fig. 1 Chae et al

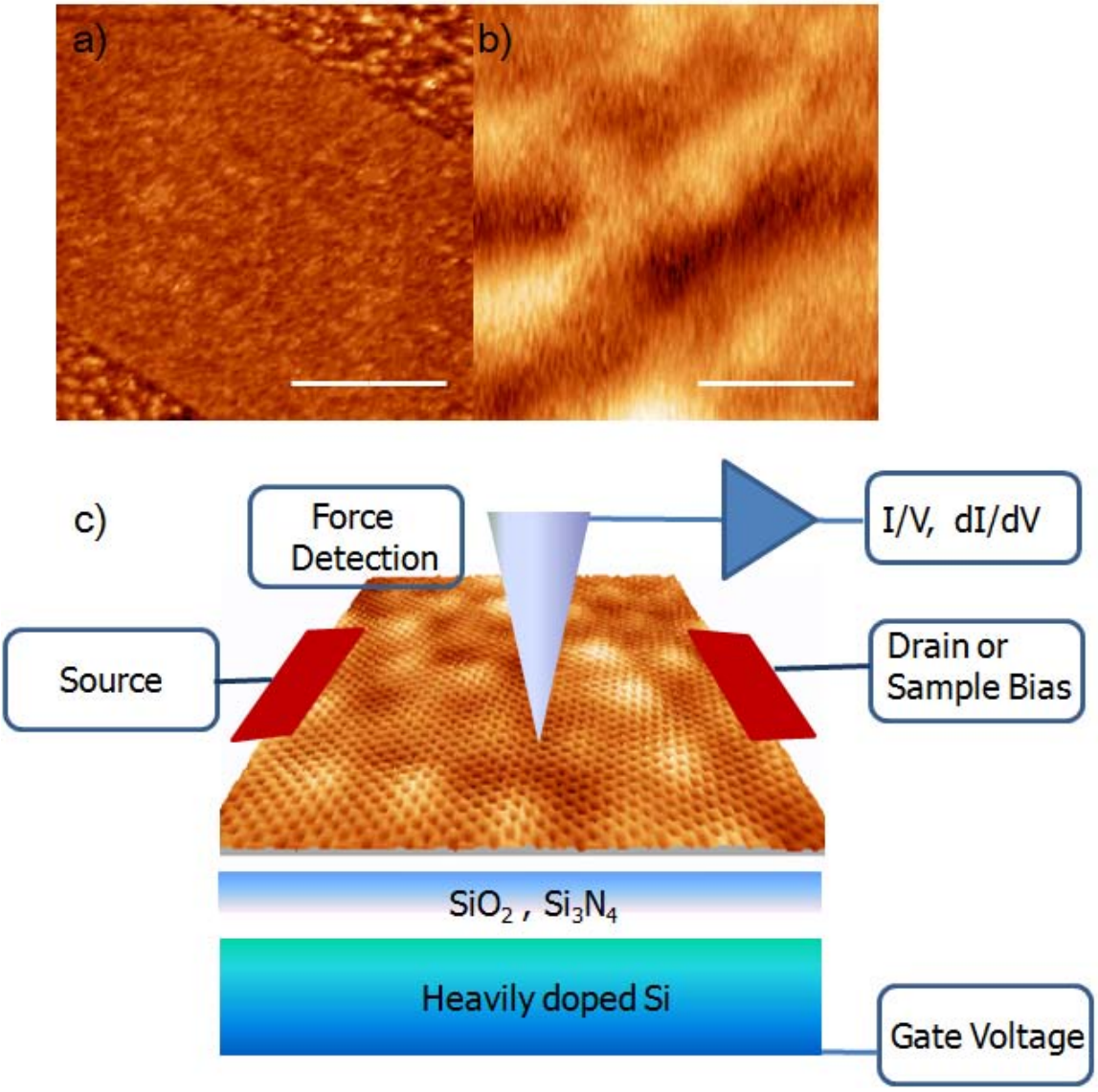
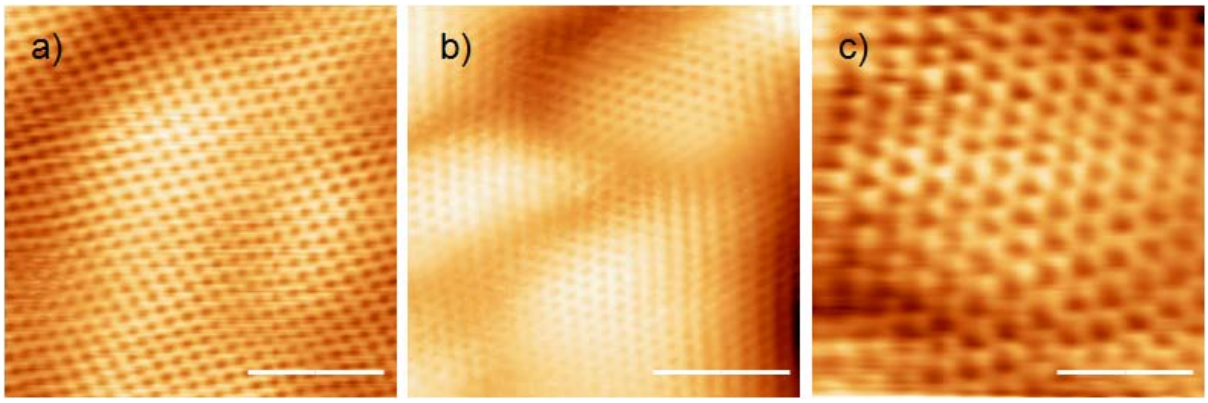


Fig. 2 Chae et al



Chae Fig. 3