A Physics-Based Simple Series Resistance Extraction Methodology

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***Abstract*— Series resistance has become a serious obstacle encountered in the development of advanced CMOS devices. At the same time, series resistance quantification in these same advanced CMOS devices is a difficult challenge. In this study, we demonstrate a very simple series resistance extraction procedure which is derived from the ratio of two linear I_D-V_G measurements on a single device. The physics of this method is intuitively simple and the assumptions readily justifiable. The validity of this technique has been verified by a self-consistent methodology as well as the reproduction of a known external series resistance.**

***Index Terms*—Series Resistance**

I. INTRODUCTION

The extraction of series resistance (R_{SD}) has always been an important but challenging issue for CMOS technology development. Without an accurate handle of R_{SD}, the extraction of many other transistor parameters becomes complicated and the comparison of measured transistor behavior to transistor models becomes difficult. As MOSFET scaling continues to reduce the channel resistance ($R_{channel}$), R_{SD} is becoming a larger fraction of the total device resistance ($R_T = R_{SD} + R_{channel}$) and is soon expected to limit the performance in advanced devices [1-3]. One of the frontiers of advanced CMOS process optimizations is currently focused on R_{SD} minimization [3]. However, quantification of these efforts is quite difficult [4] because R_{SD} extraction is often full of pitfalls [4]. Historically, most R_{SD} extraction techniques involve R_T measurements on an array of devices with various gate lengths or, at the very least, a comparison between a long and short channel devices [5-8]. These "*L*-array" extractions all suffer from several disputed assumptions that are more problematic for submicron devices with lightly-doped drain (LDD) or source/drain extension [4]. These difficulties have led many researchers to pursue R_{SD} extraction methodologies based on a single device [9-14]. However, these approaches still involve assumptions leading to significant error [10]. In addition, some methods require independently known device parameters that are not easy to measure accurately.

In this study, we detail a very simple R_{SD} extraction procedure that only requires two linear DC I_D-V_G measurements on a single device. It also does not require differentiation of data like many proposed methods. It is entirely physics based. It does not require knowledge of the L_{eff}, the effective channel width (W_{eff}), oxide capacitance (C_{ox}), or μ_{eff} and thus frees it from the most troubling concerns inherent to the commonly used "*L*-array" methods. Since these parameters are particularly difficult to quantify in short channel devices, the proposed extraction procedure is well suited to monitor R_{SD} as channel lengths continue to scale.

The proposed method relies on the common linear drain current expression [7]:

$$I_D = \mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \left(V_G - V_{ON} - \frac{m}{2} V_D \right) V_D \tag{1}$$

where m is the body-effect coefficient, and V_{ON} is the V_{TH} as obtained by the linear extrapolation method minus $mV_D/2$. Our first approximation is to set $m=1$. We call this new V_{ON} our V_{th}, which is the true threshold voltage by definition (when $m=1$). Next, we keep V_D at very low value such that (1) simplifies to a linear (to V_D) form:

$$I_D = \mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} (V_G - V_{th}) V_D \tag{2}$$

Clearly, (2) is valid only when gate overdrive is much larger than $V_D/2$. For the proposed method to work, V_D must be kept small. We note that at low drain biases, both the common square-law formalism as well as the more accurate sheet charge model both simplify to eqn. 1. Even the recently proposed semi-empirical model for short-channel MOSFET [15] reduces to eqn. 2.

II. EXPERIMENTAL

When source/drain series resistance R_{SD} is included, (2) becomes:

$$I_D = \mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \left(V_G - V_{th} - \frac{I_D R_{SD}}{2} \right) (V_D - I_D R_{SD}) \tag{3}$$

where V_G is the applied gate to source bias, V_{th} is the threshold voltage, and V_D is the drain to source bias. The key of our method is simply take the ratio of two I_D-V_G curves recorded at two similar but low drain biases. This leads to:

$$\frac{I_{D1}}{I_{D2}} = \frac{\mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \left(V_G - V_{th1} - \frac{I_{D1} R_{SD}}{2} \right) (V_{D1} - I_{D1} R_{SD})}{\mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \left(V_G - V_{th2} - \frac{I_{D2} R_{SD}}{2} \right) (V_{D2} - I_{D2} R_{SD})} \tag{4}$$

The advantage of this approach is that these two linear I_D-V_G measurements are taken on the same device under very similar conditions. This allows one to quite reasonably cancel out the most difficult to measure quantities in eqn. 4 (μ_{eff}, C_{ox}, and L_{eff}). The validity of these cancellations will be examined carefully in the next section. After cancellation, eqn. 4 can be rearranged to:

$$R_{SD}^2\left(\frac{I_{D2}-I_{D1}}{2}\right)+R_{SD}\left(V_{th2}-V_{th1}+\frac{V_{D1}-V_{D2}}{2}\right)-\frac{(V_G-V_{th1})I_{D2}V_{D1}-(V_G-V_{th2})I_{D1}V_{D2}}{I_{D1}I_{D2}}=0 \quad (5)$$

which is an easily solvable quadratic equation yielding R_{SD} as a function of gate overdrive:

$$R_{SD}=\frac{-b\pm\sqrt{b^2-4ac}}{2a} \quad (6)$$

Where

$$a=\left(\frac{I_{D2}-I_{D1}}{2}\right)$$

$$b=\left(V_{th2}-V_{th1}+\frac{V_{D1}-V_{D2}}{2}\right)$$

$$c=-\frac{(V_G-V_{th1})V_{D1}I_{D2}-(V_G-V_{th2})V_{D2}I_{D1}}{I_{D2}I_{D1}}$$

We note that in this formulation we extract a different V_{th} for each drain bias. We note also that for consistency, V_{ON} extraction must use the method of linear extrapolation of the I_D-V_G curve at the peak transconductance value [16]. As noted before, (2) is an approximation which is accurate only when the gate overdrive is much larger than $V_D/2$. The extracted R_{SD} values are most accurate under the same condition of higher gate overdrives (V_G-V_{th}) and become more erroneous at lower gate overdrives.

We want to emphasize that the proposed method does not require any additional measurements beyond the two DC current-voltage sweeps. No a priori knowledge of any transistor parameter is required. Furthermore, no differentiation of any measured or extracted data is needed. This is the simplest method to the best of our knowledge.

The simplicity of this technique also leads to a simple validation methodology for the extracted R_{SD}'s. The extracted R_{SD} values can be used to correct the original I_D-V_G curves. The corrected curves can then be used to re-extract a new set of R_{SD} values (R_{SD}') which can be thought of as a residual resistance. The closer R_{SD}' is to zero is an indication of the accuracy of the originally extracted R_{SD} values.

To verify this approach we extract R_{SD} from a series of nMOSFETs (90 nm technology) with 1.6nm SiON gate dielectric. All measurements are performed at room temperature using conventional wafer prober equipment. We admit that the simplicity of this technique might be reason to question its novelty. However, quite surprisingly, we are unable to find evidence of earlier works proposing this simple approach.

III. RESULTS AND DISCUSSION

Fig. 1 illustrates the total resistance ($R_T = V_{DS}/I_{DS}$) for two linear drain biases (10 mV and 50 mV) as well as the extracted R_{SD} from a 10 x 0.2 μm^2 nMOSFET for the full range of gate overdrive. At high gate overdrives, we observe R_{SD} values (≈ 32 Ω) which are approximately ½ of the total "on" resistance (≈ 65 Ω) of the device. R_{SD} increases slowly as gate over drive decrease at first, the pace of increase picks up as gate overdrive approaches threshold. This general trend is consistent with most series resistance models [17, 18]. The extracted R_{SD} values are then used to correct the original I_D-V_G curves to produce a set of "series-resistance-free" I_D-V_G curves. The series resistance extraction method is applied again on this new set of I_D-V_G curves to extract a second set of series resistance (R_{SD}') which is also shown in fig. 1 as residual. As can be seen, residuals are quite small at higher gate overdrives and become more erroneous at lower gate overdrives. This is consistent with our previous discussion on the validity of the approximate assumption.

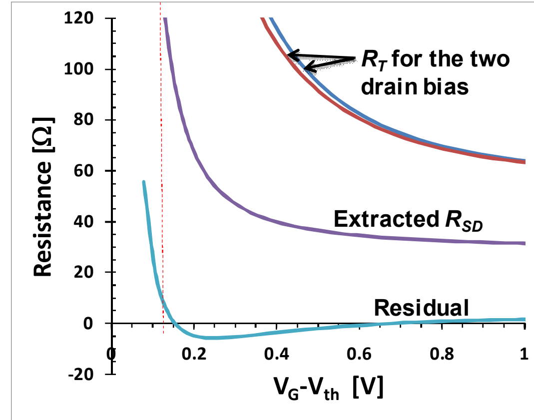

Fig. 1 The total resistance ($R_T = V_{DS}/I_{DS}$) as a function of gate overdrive for V_D = 10 mV and V_D = 50 mV as well as the extracted R_{SD} and R_{SD}' for a 10 x 0.2 mm^2 nMOSFET is shown. The dotted vertical line shows the 10% error limit.

Next, we demonstrate the proposed method on short channel devices and to verify the method with another independent confirmation. We extract R_{SD} on a 10 x 0.05 μm^2 device in which we purposely inserted known external series resistances. Fig. 2 illustrates the extracted R_{SD} values for external series resistances (R_{ext}) of 0 Ω, 10 Ω and 20 Ω.

At higher gate overdrives, the extracted R_{SD} values, in the absence of external series resistance is somewhat lower than the longer channel length device shown in fig. 1. Since they are from the same wafer, this difference suggests that series resistance is channel length dependent. For the cases with added external series resistance, the extracted R_{SD} values increase roughly by the corresponding amount, proving once again the proposed method works.

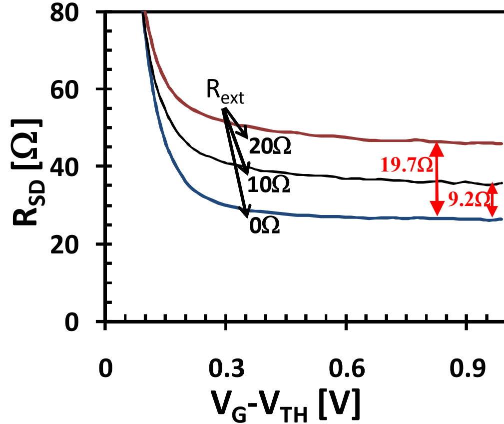

Fig. 2 The extracted R_{SD} as a function of gate overdrive for a 10 x 0.05 μm^2 nMOSFET is shown for three different values of external resistors (R_{ext}) inserted in series with the device.

The disagreement between the known resistance value of the external resistors and the extracted value is in part due to the sensitivity of measurement noise. Figure 3 shows the extracted R_{SD} for the same 10 x 0.05 μm^2 nMOSFET for repeated measurements. Clearly, the measurement noise alone can account for the observed discrepancy.

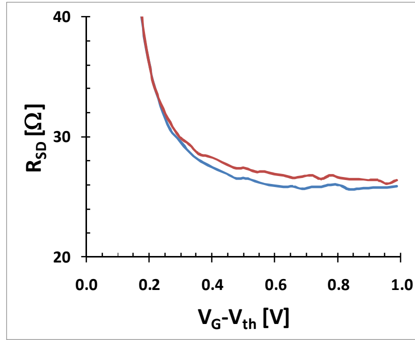

Figure 3: Extracted R_{SD} from repeated measurement of the same 10 x 0.05μm^2 nMOSFET showing sensitivity to measurement accuracy.

Thus far we have experimentally demonstrated the validity of this simple R_{SD} extraction procedure, and discussed the main source of error coming from the validity range of (2). We now turn our attention to the validity of the other simplifying assumptions used in this methodology. These issues are examined through the use of simple simulations to determine how much error is introduced.

We first investigate the assumption that L_{eff} can be taken as constant at two linear drain biases. If we assume that L_{eff} equals the combined depletion width of the source and drain junction at saturation drain bias (V_{DSAT}) (the worst case L_{eff} when the short-channel effect is under reasonable control), we can estimate the effect of a small linear drain bias perturbation using:

$$\%\,\text{Change in } L_{eff} \propto \frac{\sqrt{V_{bi}+V_{D2}}-\sqrt{V_{bi}+V_{D1}}}{\sqrt{V_{bi}}+\sqrt{V_{bi}+V_{DSAT}}} \qquad (7)$$

where V_{bi} is the built-in potential between the source/drain to substrate junction. For silicon at room temperature with typical source, drain, and substrate doping levels, $V_{bi} \approx 1$ V. For the short channel devices utilized in this study, V_{DSAT} should also be taken to equal 1 V. Thus, one can compute (using eqn. 7) the percentage change in L_{eff} for various small (linear) drain bias perturbations. Fig. 4 shows the percentage error in the effective channel length as a function of the difference of the two linear drain biases. For the drain biases used to generate Fig. 1 (10 mV and 50 mV), one introduces less than 0.8% error by assuming a constant L_{eff}.

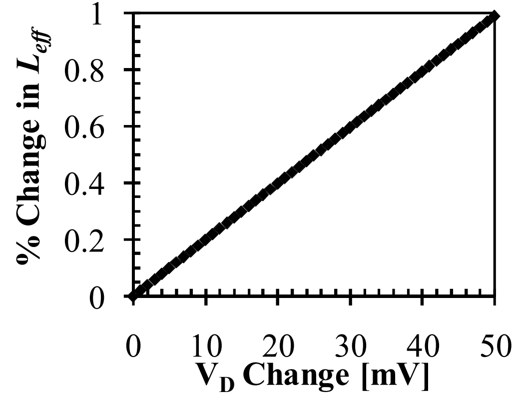

Figure 4: Simulated percentage change in L_{eff} as a function of linear drain bias change. The small linear drain bias perturbation results in very little change in L_{eff}.

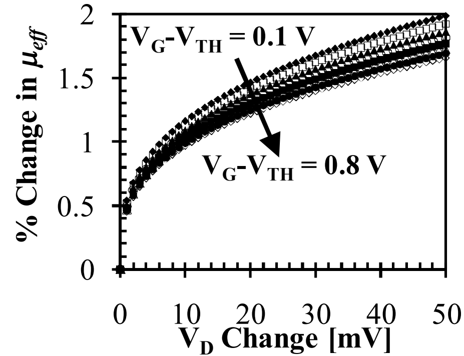

Figure 5: Simulated percentage change in μ_{eff} as a function of linear drain bias change. The small linear drain bias perturbation results in very little change in μ_{eff}.

Next we investigate the consequences of assuming that μ_{eff} is constant at two linear drain biases. Mobility is sensitive to drain bias via the perturbation of the vertical electric field in the channel. This effect can be estimated by modifying the simple effective field (E_{eff}) approximation to include the drain bias perturbation as:

$$\%\,\text{Change in } E_{eff} = \frac{E_{eff}(V_{D2})-E_{eff}(V_{D1})}{E_{eff}(V_{D1})}\times 100\% \qquad (5)$$

where

$$E_{eff}(V_D)=\frac{V_{th}+0.2+V_D/2}{3t_{ox}}+\frac{V_G-V_{th}+V_D/2}{6t_{ox}} \qquad (6).$$

Using the approximation, $\mu_{eff} \propto (E_{eff})^{1/3}$ [7], the effect of a small drain bias perturbation on μ_{eff} can be calculated (Fig. 5). For the drain biases used to generate Fig. 1 (10 mV and 50 mV), one introduces ≈ 1% error by assuming a constant μ_{eff}.

Finally, the last implicit assumption involved in our R_{SD} extraction methodology is that C_{OX} is independent of gate bias. Again, the drain bias alters the vertical electric field which indirectly impacts C_{OX}. Near threshold, a small variation in the vertical electric field has a large impact on C_{OX}. However, as discussed earlier, our extraction procedure is already untrustworthy in this gate overdrive range. Outside of this range (~ 6kT above threshold), the C_{OX} variation is actually quite small and can safely be assumed constant. Thus, all of our assumptions (constant L_{eff}, μ_{eff}, and C_{OX}) are all quite justified.

We would be remiss not to acknowledge the thoughtful work of Lin *et al*. [13, 14], who also report an R_{SD} extraction procedure involving DC I_D-V_G measurements of a single device under the constant mobility criteria. In their work, the constant mobility criterion is met through the application of a back bias as well as several fitting parameters. In ultra-short channel devices, the constant mobility criterion is much more difficult to confirm and requires the assumption that mobility is a well known function of L_{eff}. Recent reports indicate that μ_{eff} decreases sharply as L_{eff} is scaled [19, 20]. This behavior is not well understood and may threaten the validity of the constant mobility R_{SD} extractions. For most cases, our simplistic approach (without the constant mobility criterion or fitting parameters) is actually quite sufficient.

IV. CONCLUSIONS

In summary, we have presented a very simple R_{SD} extraction methodology which utilizes a single device thereby avoiding many of the assumptions used by other R_{SD} extraction techniques. Other than two DC current-voltage sweeps, no other measurements are needed. No knowledge about the device parameters is needed either. The technique has an implicit verification procedure to determine correctness. We demonstrate the utility of this procedure by extracting R_{SD} as a function of gate overdrive in several highly scaled nMOSFETs. The validity of this approach is further verified with the addition of known external series resistances. The assumptions of drain bias independent L_{eff}, μ_{eff}, and C_{OX} are also shown to be quite justified when restricted to linear drain biases and higher gate overdrives.

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