Wafer-level magnetotransport measurement of advanced transistors – making a powerful technique even more powerful

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For transistor research and development, one of the important figures of merit is the carrier mobility. The measurement of mobility is cumbersome in large devices, and nearly impossible in nano scale devices. Very often, effective mobility (μ_{eff}) is extracted from the I-V curve instead. There are many pitfalls in equating μ_{eff} to mobility (μ), including charge-trapping and series resistance effects. The error can be quite large. This is a urgent issue for advanced CMOS technology.

In this paper, two novel advances in mobility measurement introduced by our group recently [1, 2] are presented. Both are Hall Effect based and are well known. Our innovations enable both techniques to be deployed easily in any laboratory as well as factory floor.

Hall Effect has long been employed to measure Hall mobility [3]. Hall mobility (μ_H) is related to μ by:

$$\mu_H = r\mu \qquad (1)$$

Where r is the Hall factor which is defined as:

$$r = \left\langle \tau^2 \right\rangle \Big/ \left\langle \tau \right\rangle^2 \qquad (2)$$

Where τ is the mean time between collisions for the carriers, or the relaxation time. r is close to 1 for silicon MOSFET in most of the gate bias range [4, 5].

To measure μ_H, special test structure is needed, along with special equipment that can produce a large uniform magnetic field. Typically, wafer must be diced and packaged in order to insert into the magnetic cavity for measurement. As a result, Hall mobility measurement is a special effort and usually on limited number of devices.

Our new approach to Hall mobility measurement is to eliminate the large magnet, as well as the need to dice the wafer and to package the device. The result is a Hall mobility measurement that can be done in any probe station, and changing chip is a simple matter of moving the wafer.

To achieve strong and uniform magnetic field across the device, we take advantage of the fact that the device is very small and that high magnetic field is achievable near the surface of modern rare earth magnets (figure 1).

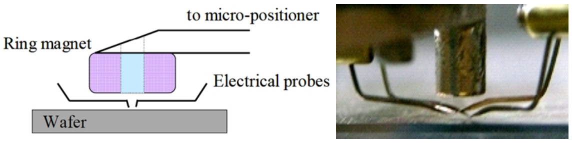

Fig. 1 Basic setup for wafer-level Hall mobility measurement. Schematic (left) and actual photograph (right). The magnetic field is controlled by the distance of the magnet to the wafer surface, ranging from 1.5 mm to 5 mm.

It is clear from figure 1 that Hall mobility measurement with our unique setup no longer requires wafer dicing and packaging. An added advantage is that the magnetic field is extremely stable. Micro positioner allows the magnetic field to be precisely controlled (figure 2).

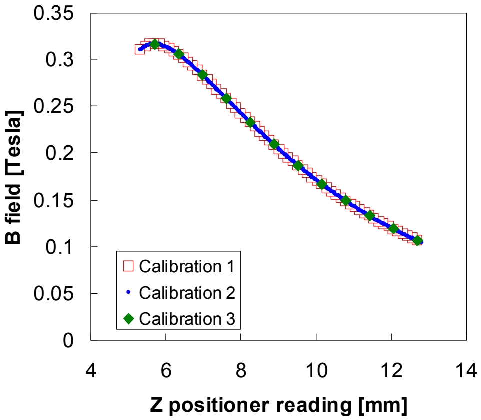

Fig. 2 Measured magnetic field as a function of the micro positioner reading. Three measurements at different days are highly reproducible.

Typical Hall mobility measurements involve measuring the DC Hall voltage. To obtain reliable value, the magnetic field needs to be large and the measurement slow. For many new devices such as III-V channel MOSFET at their early stage of development, instability can cause the measured Hall voltage to drift. Since we cannot increase the magnetic field much beyond 0.3 T, we intorduce a novel AC approach to improve the signal-to-noise ratio as well as to minimize the effect of device drift.

The Gated Hall Bar structure used in our measurement is schematically shown in figure 3.

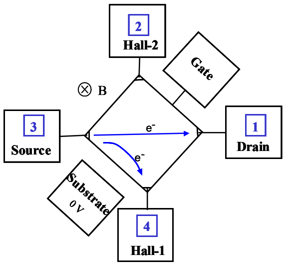

Fig. 3 Gated Hall Bar structure for Hall voltage measurement and sheet resistance measure using the Van der Pauw method.

Current modulation during the Hall voltage measurement is achieved by modulating the drain bias in the linear regime. It can be shown that plotting Hall voltage per unit drain current versus B field results in a straight line with the slope equal to the inverse of the sheet charge density [1], as shown in figure 4 for a SiC MOSFET.

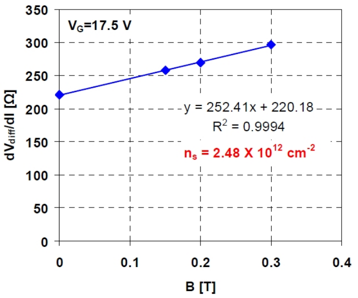

Fig. 4 Hall voltage per unit drain current vs magnetic field plot. The slope is *$1/qn_s$*, where n_s is the sheet charge density.

The excellent fit to a straight line is testimonial to the accuracy of the AC approach.

To extract the Hall mobility, one combines the sheet resistance from the Van der Pauw method with the sheet charge density from the Hall voltage measurement. An example is shown in figure 5 for a SiC MOSFET – a device that is still in development and therefore has stability issues.

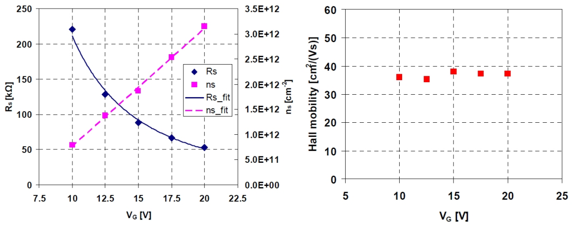

Fig. 5 Measured sheet resistance (Van der Pauw) and sheet charge density (Hall) as a function of gate bias (left) for a SiC MOSFET. The extracted Hall mobility (right) is almost independent of gate bias.

The mobility as extracted for the SiC MOSFET is in good agreement with conventional Hall measurement, with smoother distribution. Thus we have demonstrated a novel new method for Hall mobility measurement that is much easier to use and produce better results.

While the new Hall mobility measurement method greatly benefits the device research community, it is not capable of solving the mobility extraction problem for ultra scaled MOSFETs. At issue is the need for a special test structure – the gated Hall bar which cannot be made on ultra scaled devices.

An alternative magnetotransport method for mobility measurement is the geometric magnetoresistance method. This method does not require a special test structure. It can be used on standard transistors found in most technology development wafers. All that is required is that the transistor has a channel width at least 5 times larger than the channel length. Thus it is very convenient.

Geometric magnetoresistance mobility measurement is less well known to the silicon community because the signal is very small for silicon device. Intuitively, it is just an extreme case of Hall measurement where the source and drain short-circuited the Hall voltage. The Lorenz force is acting on the channel electron just like in the Hall measurement. It results in an increase in channel resistance. For MOSFET geometries with channel width/channel length > 5, the geometric magnetoresistance effect is often described as [6]:

$$\frac{R_B}{R_0} \cong 1 + \mu_H^2 B^2 \qquad (3)$$

where B is the magnetic field, R_B is the measured resistance with $B \neq 0$, and R_0 is the measured resistance when $B = 0$. For typical silicon MOSFETs with mobility of 350 cm2/Vs, a typical Hall magnet

(B = 0.4 T) can only produces a (0.035 $m^2/Vs)^2$ x $(0.4\ T)^2 \approx 0.02$ % resistance change.

Traditional wisdom has it that geometric magnetoresistance measurement is not suitable for silicon devices. However, the severe need to measure mobility for advanced CMOS technology has prompted some heroic effort to use it on ultra scaled silicon MOSFET utilizing really large magnetic fields (>10 T) [7-9].

The need for very large B field naturally means highly specialized equipment that exists in only a handful of laboratories in the world. Dicing the wafer and packaging the device is also a necessity. If Hall mobility measurements are done only occasionally, geometric magnetoresistance measurement of silicon device is done only by heroic efforts.

A further complication arises when using geometric magnetoresistance measurement on ultra scaled silicon device is that the channel resistance is comparable or smaller than the series resistance – an issue that is unique. To correct for the series resistance effect, a second device must be measured and some questionable assumption must be used [7].

Can we apply the same trick on Hall measurement to the geometric magnetoresistance measurement to make it not only much more user friendly but also much more accurate by eliminating the need for a second device and the associated assumption? At first glance, it does not look promising. As seen in the Hall mobility measurement method above, the maximum magnetic field achievable by a single permanent magnet is only 0.3 T. The signal will be extremely small. On the other hand, MOSFET drain current noise can get really small as well. If we move away from the standard DC measurement, the drain current noise can be low enough to allow very small signal to be detected.

From equation (3), it is clear that modulation of the drain current, like we did in the Hall mobility measurement case, will not work. The only modulation that will work is the magnetic field. The standard method for magnetic field modulation is to modulating the current of an electromagnet. However, the maximum modulation achievable is on the order of 0.05 T – much too small for our need. In addition, the electromagnet will have to be big, making it difficult to build a user-friendly wafer-level measurement system.

From figure 2, it is clear that significant magnetic field modulation can be achieved by modulating the distance between the magnet and the wafer. This leads to mounting the small magnet on a voice coil to facilitate the distance modulation. Figure 6 shows the magnetic modulation.

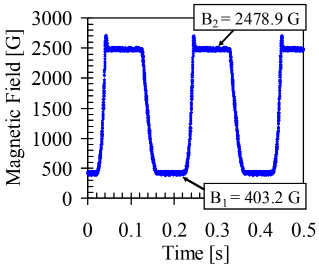

Fig. 6 The magnetic field waveform

As can be seen, we achieved a 0.2 T of magnetic field modulation. The frequency is 5 Hz. Higher frequencies would have been better, but we were not able to maintain a trapezoidal waveform. A trapezoidal waveform is important for the magnetic field. More specifically, flat top and bottom are important to separate inductive current from the change in drain current. A newer design is in the work to reach 1 kHz. Figure 7 shows the resulting drain current change for a 90 nm channel length nFET.

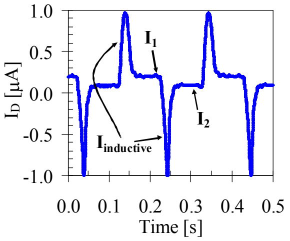

Fig. 7 Drain current change as a result of magnetic field modulation.

The peaky transients in the figure are the inductive current. The geometric magnetoresistance effect manifests itself by I_1 and I_2, corresponding to the low and high magnetic fields. It is straight forward to show from (3) that

$$\mu_H^2 \cong \frac{\Delta I}{I_{DC}\left(B_2^2 - B_1^2\right)} \qquad (4)$$

Thus, we can obtain the Hall mobility from the change in drain current.

An important distinction between our approach to geometric magnetoresistance measurement and the standard approach is that we measure current change instead of resistance change. This subtle difference is very important. In measuring the total resistance change, error due to series resistance is included. In measuring current change, series resistance does not play any role. ΔI is entirely coming from the channel. Since I_{DC} is the total current as well as the channel current, $\Delta I/I_{DC}$ is completely free from the inference of series resistance.

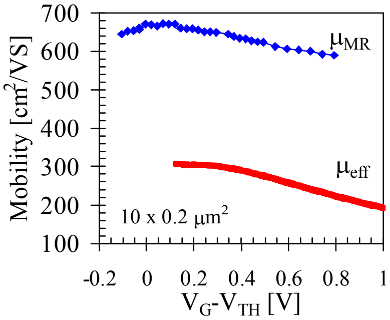

Fig. 8 Comparing measured mobility by the geometric magnetoresistance method and the effective mobility obtained from the I-V curve.

Figure 8 shows the measured mobility along with the μ_{eff} extracted from the transistor I-V curve. The difference is huge. This difference is in large part due to error introduced by series resistance to μ_{eff}. After correcting for series resistance, the μ_{eff} become much closer to the measured magnetoresistance mobility (figure 9).

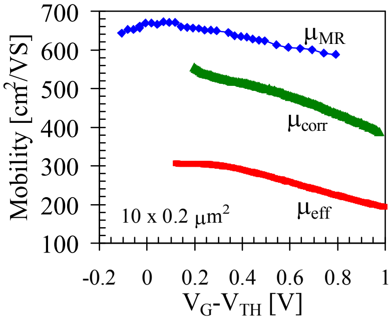

Fig. 9 The corrected effective mobility is much closer to the magnetoresistance mobility.

Clearly, there is still difference. However, the error is more likely in the μ_{corr} than in the μ_{MR} because many of the factors in the extraction of μ_{corr} can only be approximated, including the series resistance. The measured μ_{MR} is consistent with highly strained nFET.

Note that technically $\mu_H = \lambda \mu_{MR}$ with $\lambda \neq 1$. However, when carrier scattering is near isotropic (Hall factor $r \sim 1$), λ is ~1 as well.

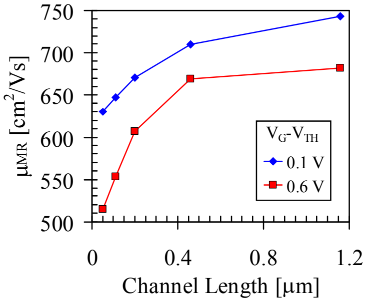

Fig. 10 Mobility degradation as channel length decreases.

Figure 10 shows the Magnetoresistance mobility as a function of channel length. The observed degradation as channel length shorten is a current issue that is not quite understood, and is one of the reason reliable mobility extraction method is urgently needed.

In summary, we demonstrated two ways to measure carrier mobility easily and reliably. No special equipment is needed, and no wafer dicing and device packaging is required.

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