Smart Clocks Have a Hand in the Smart Grid

J. G. Fletcher, M. Chaluvadi, D. M. Anand, J. Amelot, Y. Li–Baboud, and J. Moyne

***Abstract*—Clock synchronization is becoming an increasingly important characteristic of modern wide area monitoring and control systems such as the power grid. It provides an opportunity to coordinate control actions and measurement instants across hundreds of miles and numerous network topologies. Devices and networks have advanced to a point where synchronization across a wide area can be achieved within $1\mu s$ of UTC (Coordinated Universal Time). Along with these advances in clock synchronization must come a shift in the way analysis is performed. Modeling techniques must incorporate the effects of a clock synchronized device, and control techniques can leverage the knowledge of "time" to achieve unique results. This paper discusses various ways in which clock synchronization affects analysis and performance of the power grid, and presents a few projects related to the technology. Preliminary work has demonstrated the ability of various commercially available devices to provide reliable $1\ \mu s$ synchronization of clocks, and large variation across devices in terms of clock performance under transient events.**

Keywords: time synchronization, networked control, model order deduction, data quality, PTP, NTP, GPS, Smart Grid

I. Introduction

The Northeastern blackout of 2003 brought to the attention of the power distribution industry the need for a comprehensive look at requirements for synchronized distributed measurements to preempt cascading failures in the grid. The event also heightened the need for more accurate data recorders on the electrical grid to aid in rapid fault diagnosis. Inaccurate time-stamps caused significant delays in diagnosing the cause of the blackout. Realizing the importance of time synchronization, the power distribution industry adopted several standards dictating minimum synchronization requirements for time synchronization and time-stamping accuracy. To ensure that the upcoming industry requirements are feasible and sufficient, National Institute of Standards and Technology and University of Michigan are jointly developing a grid control and data simulation testbed with the objective to develop metrics, measurement methods, and recommended practices based on practical industry scenarios for meeting distributed time synchronization requirements, distributed control specifications and a sandbox environment for next generation software and data acquisition devices in power distribution applications. The testbed enables the characterization of the factors impacting synchronization precision and the determination of how the synchronization precision in turn affects the reliability and integrity of power distribution monitoring and control. This paper will discuss the multiple aspects of this testbed and the early results from several focus areas within it.

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II. Device Clocks

As processing power advances and computer components reduce in size, it becomes possible to include more functionality within a device. As a result devices are often called upon to do more than just collect measurements. This is especially true of the power grid, where it is critical that a device be aware of the global time at which an operation is performed or measurement taken so that, for example, it may be able to coordinate its operation with other components to collectively deliver uninterrupted power. The device's clock may need to be synchronized to a global time source with an accuracy within $1\mu s$ in order to perform these tasks. Time stamps based upon this synchronized time are applied to measurements and provide a reference to the time at which the measurement occurred. The measurements can then be ordered by any user based upon time stamps to provide a time-line of events or a snapshot at a particular instant of time. The authors in [1] present a solid overview of the importance of clock synchronization for power grid devices. The next few paragraphs will discuss some critical uses of clock synchronization.

A device which is playing an increasingly important role in grid health monitoring is the PMU (phasor measurement unit). PMUs are used in wide area monitoring and protection schemes to compare voltage and current measurements collected throughout the grid at specific times. The PMUs collect this information and transmit it with an associated timestamp to a PDC (phasor data concentrator), where data from multiple PMUs collected at the same point in time are combined to essentially provide a snapshot of the grid condition. A device which is playing an increasingly important role in grid health monitoring is the PMU (phasor measurement unit). PMUs are used in wide area monitoring and protection schemes to compare voltage and current measurements collected throughout the grid at specific instants in time. The PMUs collect this information and transmit it with an associated timestamp to a PDC (phasor data concentrator), where data from multiple PMUs collected at the same point in time are combined to essentially provide a snapshot of the grid condition.

The accuracy of the data packets, also known as synchrophasors, is determined by the TVE (total vector error), which is required to be less than 1 percent [2]. The error arises from inaccuracies in the initial measurement, internal processing time, and errors with the timestamp. To illustrate the importance of clock synchronization on PMU performance, a timestamp error of $26\mu s$ will lead to a 1 percent TVE on its own. In order to maintain an acceptable TVE in the presence of the other errors mentioned above, PMU clocks should be synchronized to within $1\mu s$ of UTC. More information about this can be found in [3] and [2]. The following list is a brief overview of PMU specifications;

- The PMU is a high fidelity sensor capable of sampling voltage and current waveforms at rates up to $10,000$ Hz.
- The synchrophasor is a vector measurement which is reported at a rate of up to 60 Hz.
- These compiled reports are time-stamped, accurate to within $1\mu s$ of coordinated universal time (UTC).
- Synchrophasors from multiple PMUs are combined based upon corresponding time stamps to provide a snapshot of grid conditions.
- Inaccurate time stamps create noise in the form of phase error of the vector measurement [4]. More accurate time stamps means lower phase errors.

An important and often overlooked factor of device performance is the local oscillator within devices. These oscillators are responsible for providing the basic unit of time for the device, as well as the basis for the local approximation of global time. While oscillators have varying accuracies depending on the material and housing, each individual oscillator will display unique drift and offsets. If devices are to be used in coordination with one another effectively, this variation in oscillator offset and drifts must be minimized. Clock synchronization techniques address this issue by periodically correcting the local estimated time to reflect the accepted global time. Current technology can synchronize local clocks to within 100 *ns* of the global reference [1]. Various methods will be discussed further in Section IV.

With this accurate knowledge of global time, devices can be coordinated to perform actions or take measurements at a specific instant in time. However, the accuracy of this performance is bounded by the accuracy of the device's local time estimation. For example, if a device were to apply a 1 μs accurate timestamp as a measurement is taken, the measurement could have occurred at any point within the 1 μs window. Therefore, increasing the performance of device clock synchronization can only improve measurement capabilities.

III. Impact of Clock Inaccuracies on Models

As more devices incorporate clock synchronization into basic performance, it becomes imperative to reflect this in the model. Devices which synchronize clocks to a global reference will show delay and jitter patterns unique to each device. Additionally, time stamps have a base time granularity which limits time accuracy, and consequently place an additional bound on measurement accuracy. Both of these factors mean that actual device performance will vary between devices. If models are not designed to reflect these variations, the model will not be able to accurately reflect the device's physical performance.

Addressing modeling techniques is important because modeling, combined with high performance sensors and networks, is a critical component of improved monitoring and control of the wide area networks found in the power grid. In large networks with numerous nodes and large communication delays, it is often infeasible to simply place a sensor at every node. Instead, models are used to estimate nodes between locations where measurements are taken, or to smooth reported data.

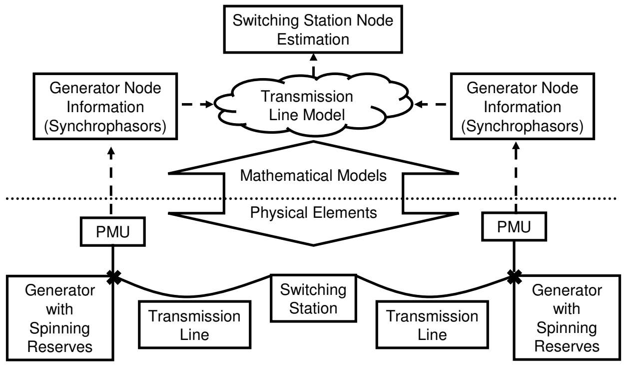

Fig. 1. Schematic representation of the coupled interaction between physical elements and mathematical elements discussed in the use case. PMUs serve as the interface between the two domains.

In this situation, virtual sensors must interact with physical sensors to create as accurate of a representation of the grid as possible. Additional examples of modeling applications can be found in [5] and [6].

Especially in the case of node estimation, the model must be able to reproduce the characteristics of the device, including time synchronization. This is illustrated in Figure 1, which shows an example of interaction between the mathematical model and the physical system. Ideally, the model in this figure will represent as many characteristics of the physical system as possible, which includes clock synchronization.

The authors in [7] present an argument for including time synchronization in model syndication. They show that as model complexity increases, the model becomes more sensitive to the limits placed on devices by clock synchronization. It follows that at some point, the model complexity will have increased enough so that the modeled device, unburdened by the bounds of clock synchronization, essentially outperforms the physical clock-synchronized device. From then on, increasing model complexity will lead to increased deviation between the model's and physical device's performance. Therefore, including clock synchronization as a model design parameter will increase model accuracy and help limit unnecessary complexity in the model.

IV. Networks and Clock Synchronization

As we have shown in the previous sections, the infusion of clock synchronization into power grid technology has opened the door for advanced measurement and simulation techniques. However, device performance and network modeling techniques reflect the capabilities of the network used. As a result, network theory must continue to advance in order to take advantage of the gains made possible through improved clock synchronization. Advanced network protocols such as the IEEE 1588 Precision Time Protocol (PTP) provide clock synchronization within 1 μs across an Ethernet network [8]. Additional communication mediums such as fiber-optics may provide a platform to further increase synchronization. Model fidelity can also be improved as more accurate clock synchronization will lead to lower noise introduced by clock variations. The remainder of the section will detail the types of networks and synchronization commonly found throughout the modern power grid.

PMUs and many other IEDs are currently synchronized to UTC (coordinated universal time) via GPS. This system is capable of providing clock synchronization within 100 *ns* of UTC depending on the wiring of the antenna and the availability of the GPS signal [1]. GPS synchronization is ideal for wide area networks since no wiring is needed between locations, but does not provided economical synchronization within a local network. As the number of devices on a network requiring synchronization increases, additional antennas must be installed and the cost of the network quickly escalates. IRIG-B and PPS are often used to extend GPS synchronization to devices [1].

A promising solution is the introduction of PTP into the synchronization path. PTP is an Ethernet specific clock synchronization protocol which is capable of providing synchronization of all clocks on a local network to within 1 μs. This level of synchronization can be used to extend the time accuracy of a GPS clock received through one antenna to all devices on the same Ethernet network. The following table compares important characteristics of the current use of various synchronization protocols. Additional information on PTP can be found in [8] and [9].

	communication medium	**time accuracy**	**network type**
GPS	satellite	< 100 *ns*	wide area
PTP	Ethernet	< 1 μs	local
IRIG-B	dedicated	< 100 *ns*	either
NTP	Ethernet	1 *ms*	either

V. Time aware Control

Time stamping of measurements is useful for data acquisition especially when the data is aggregated from distributed sources. Nodes can reorder data received out of order based upon the time stamp, as long as the time stamp accuracy is greater than the frequency of packet creation. In addition, data recorded at one point on the network are valid globally as PTP synchronizes all clocks on the network to Coordinated Universal Time (UTC). Controllers can receive data packets and determine the absolute time at which the data originated, instead of estimating this time based upon the packets arrival time. The effect of network jitter is thereby limited, and real-time estimation or control algorithms can be implemented in a cluttered network.

Control using PTP has been implemented on a much smaller scale. One example is the motion control system developed by SERCOS [10] which uses PTP to send and receive data at precise time schedules. The specific application of accurate networked clocks to a control algorithm vary with each particular case, but there are some general improvements that are applicable to several control strategies. We picked two major directions to study that apply to a general class of closed loop control with networked resources, and are especially relevant to very large, spatially distributed network architecture similar to those found in the power grid. They are broadly classified under *improved state estimation* and *improved trajectory or command scheduling*. The illustrative example we use is a testbed consisting of two identical

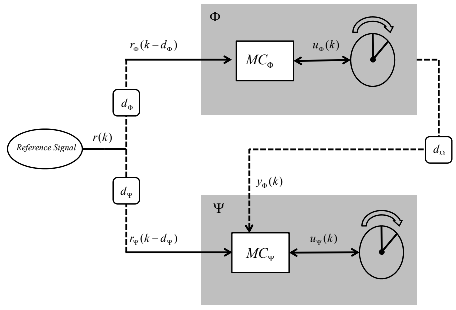

Fig. 2. A schematic showing the control layout for the networked master–slave pair. The blocks $d_\Phi, d_\Psi, and\, d_\Omega$ symbolize network delays between the respective components. MC_Φ and MC_Ψ are the motor controllers. $y_\Phi(k)$ is the trajectory of Φ: and $u_\Psi(k)$ and $u_\Phi(k)$ are the control signals sent to the motors. Φ: and Ψ denote the two individual dynamic systems.

DC motors with coded rotors spinning at 60Hz (chosen to emulate a generator producing a voltage waveform at 60Hz), the rotors are instrumented with an optical encoder and a photo interrupter which generates one pulse per revolution. The control infrastructure is tasked with synchronizing both rotors in frequency and removing the phase error between the two rotors. Additionally both rotors have to track a remote frequency reference.

A. State Estimation

An integral part of designing a controller is the assumption that the controller has a clear picture of the current state of the plant as well as other controllers in the network neighborhood that share resources or dependencies. The local assumption of the environment the controller is operating in is called the state estimate. Consider the system presented in Figure 2, which is an illustrative block diagram of a hierarchical system where local nodes Φ and Ψ are tasked with synchronously following a remote reference signal. The challenge in doing this is that the three terminal locations in the diagram are located far apart such that signals between them are transmitted over a non-deterministic network and experience random delays $d_\Phi, d_\Psi, and\, d_\Omega$.

In order to achieve the desired closed loop performance each node has to implement control based on an estimate of each of the collaborating nodes since waiting for an update from each node is not possible. As a specific case consider that system Ψ needs to build an estimate of system Φ. It can be shown that standard estimation algorithms fail when used in the presence of network jitter in the scale of 5ms [11]. We therefore adopt a two step process to introduce synchronous estimates for y_Φ into Ψ. At the first step we generate a time stamped vector table of input and output values from Φ, $[r(k-nk)...r(k)]$ and $[y_\Phi(k-nk)...y_\Phi(k)]$ where $y_\Phi(k)$ is the current output measurement and $y_\Phi(k-nk)$ is an output measurement from n samples ago. As this vector table is transmitted to the Estimation and Propagation module (which is physically co-located with the slave system), it incurs a delay d_Ω. We use this time stamped vector table for parametric system identification with an assumed linear 2^{nd} order structure. An Auto-Regressive Moving Average (ARMA) model [12] is used to identify the system parameters and generate an identified model $(\widehat{(A_\Phi + B_\Phi K_\Phi)}, \hat{B_\Phi})$. Once the identification model is updated, we have a local model of Φ at Ψ validated against

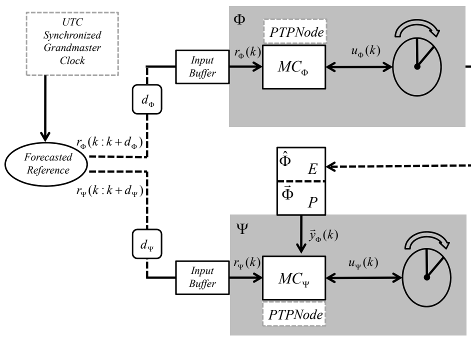

Fig. 3. A schematic of the same control layout shown in Figure 2. Modules E and P denote the Estimation and Propagation blocks added to compensate for delays d_Φ, d_Ψ, *and* d_Ω.

a measured dataset up to $\hat{y}_\Phi(k-d_\Omega)$. We use this estimation model $(\widehat{A_\Phi + B_\Phi K_\Phi})$ to propagate y_Φ forward to $\vec{y}_\Phi(k)$. This process is schematically presented in Figure 3.

B. Reference forecasting

For the communication to the higher level controller which sends out the reference trajectory, we employ a strategy we call reference forecasting. This strategy addresses the problem of random delays in the reference signal by using an input buffer on the individual control modules and aggregated data transmissions to systems Φ and Ψ of the form $[r(k)...r(k+d_\Phi)]$ and $[r(k)...r(k+d_\Psi)]$ with corresponding time-stamp vectors $[t|_k...t|_{k+n})]$. While this is a conceptually simple solution, it is difficult to implement physically due to the unavailability of estimates for d_Φ and d_Ψ. With the PTP implementation we are able to draw estimates of the network delay between any two network components by comparing the delay value computed by the PTP algorithm. The PTP algorithm uses advanced network modeling techniques to establish a network delay when computing offset estimates, and we use the same data to estimate reference delays. To accommodate differences in state since the last PTP update cycle we use additional points in the reference table to get $[r(k)...r(k+d+nTs)]$, where Ts is the sampling time. The input buffer module records these vector tables and presents a valid $r(k)$ on being polled by the control recursion. Figure 3 shows the input buffer component.

The testbed and the control design are discussed in more detail in [11] and [13]. Comparative results are also presented in [11] showing an order of magnitude improvement in the mean squared error between Φ and Ψ.

VI. Future Work and Conclusion

A. PMU Clock Synchronization

PMU devices are currently synchronized by some combination of GPS and IRIG-B signals. This setup can provide sub 1 μs synchronization to a few PMUs in a local area via a splitter. PMU technology is beginning to be incorporated into other devices which can benefit from, or provide, synchrophasor measurements. As more devices require GPS synchronization, more antennas must be installed in the same local area to provide the needed GPS clock synchronization. This can quickly lead to an increasing network cost which may become unreasonable.

An alternative is to use PTP within the clock synchonization loop. Since PTP can be implemented through Ethernet networks, it presents a cost effective solution to the problem of synchronizing many devices in the same location, and still meets the $1\mu s$ requirement for PMU operation.

In coordination with NIST, we plan to examine the feasibility of including PTP in the PMU synchronization loop. A PTP slave node will be synchronized to a Grandmaster via an Ethernet network. The PTP slave will provide an IRIG-B signal based on its internal PTP synchronized clock to a PMU. The entire synchronization path should be able to maintain the required sub 1 μs synchronization required to maintain an acceptable TVE. We will compare the synchrophasor output to the synchrophasor output from the same PMU synchronized without PTP in order to determine any differences.

B. Testbed

A NIST IEEE-1588 testbed [14] is being developed in collaboration with the University of Michigan to evaluate the latest IEEE 1588 solutions for Power Systems Application. The objectives of the testbed are to establish methods for measuring and testing the accuracy and reliability of PTP, as well as to characterize factors impacting PTP performance using commercially available products. We conducted tests on hardware and software developed by commercial vendors. Grand Masters, Boundary/Transparent Clocks and Ordinary Clocks are being tested to ensure that at any time, the 1 μs end to end synchronization offset constraint required for PMU TVE (see Section IV) is met. Other aspects of the products are studied as well, like the interoperability between manufacturers, and compliance to the 1588-2008 standard. Steady state performance is studied over extended durations (typically days), as well as performance during specific event-related scenarios. These include Grandmaster (GM) loss or switching, topology change, different network load, and traffic patterns, all of which aim to closely replicate the environment of an electric substation. The test scenarios also cover a variety of experiments aiming to test the PTP parameters (such as different sync rates), or the type of topology used (star, ring, high availability seamless ring). The resulting conclusions are based on a set of established metrics including the sync offset, its distribution, the convergence rate and convergence patterns of the slaves, the Maximum Time Interval Error, the statistical error rate, and the mean path delay. The monitoring of the devices can measure the synchronization offsets with an 8 ns accuracy, and has been designed to be scalable. It is under constant improvement and is currently expanding (Please contact JA for hardware donation in exchange for our feedback).

The Initial results, based on a network consisting of 7 hops, conducted over 48-hour periods (without traffic injection for the first phase) showed that the commercially available products which have been tested are able to provide a reliable 1 μs time synchronization. That is true even when the BMCA

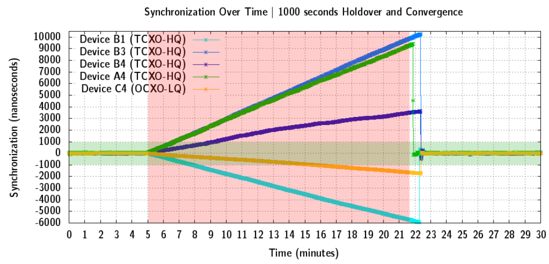

Fig. 4. A plot of the drift upon loss of connection to the Grandmaster and resynchronization of PTP slave devices. Note the large variation in performance.

(best master clock algorithm) switches GMs, showing that PTP is a excellent candidate for electric substations to progressively update their current architecture. Figure 4 illustrates the importance of the quality of the local oscillator, which affects the stability and 1 μs holdover achieved by the slaves when a network failure leaves them on their own (clocks free running). In an event where this problem is caused by a GM failure, the obvious solution is to add GM redundancy. This prevents the drift from happening as the BMCA will pick up the backup GM as soon as the primary one becomes unavailable [14]. However, the slaves must re-synchronize quickly to the backup GM, with minimal peaks in the synchronization offset.

C. Smart Grid Communication Simulation

Smart grid operation requires long distance, high frequency communication, which amplifies the necessity to analyze the network performance characteristics such as time synchronization, delay, packet loss etc. This network analysis can be done via three methods, namely by analytical modeling, simulation, or real life measurements [15]. Analytical and real life measurements are not a fast or economical way to proceed for a preliminary analysis of a complex network, while simulators can quickly provide a flexible and scalable simulation environment. We have thus determined that an OPNET simulation[1] platform is a valuable accessory to complement the hardware testbed.

The OPNET simulation focus is twofold; to provide a platform from which to test power grid specific networks, and to create a environment to test wide area control methodologies. This project is specifically concerned with establishing the performance capabilities and issues associated with introducing PTP to currently existing power grid wide area and substation networks. The project will provide a library of PTP and power grid related devices, communication mediums, and topologies from which any network can be modeled. Future devices can be validated in this environment and network topologies can be examined to determine the operational bounds of the topology and PTP.

The simulation is meant to complement the testbed discussed in Section VI-B. It provides customization and scalability which is not possible with a physical testbed, and can interface with the testbed in order to act as a background extension to the physical devices found in the testbed. Metrics that have been developed from experiments on the testbed will be tested in large scale networks within the simulation, and new devices can be included in order to determine their performance when interacting with other devices.

Simulation of the base network using OPNET can be done by logically relating the network functionality of the individual devices to the extensive library available with the software. To start with, a PMU's network functionality is to generate packet data as per the C37.118-2005 standard [2] and send it across to the PDC. The PDC stacks the received packets based on the timestamp, and forwards them to the control application, which can then develop the snapshot of the grid and take further action if required. In the simulation, this functionality can be achieved by modifying OPNET Ethernet modules available in the library to generate the required packets at a realistic rate [16]. Further, additional modifications must be made in order to include PTP in the simulation through the addition of a local oscillator to the modules, along with PTP specific functionality.

Background traffic can be customized to match a myriad of patterns. This is important as testing PTP performance in an unloaded Ethernet network does not provide any useful information. The most important information comes from situations where network loads are changing or pushing the bounds of the network's capacity. In these conditions, PTP must be able to maintain the required clock synchronization levels or device performance will suffer. Testing PTP performance in a simulation permits easy customization of traffic patterns and evaluation of key network components ability to maintain their PTP functionality.

D. Future Controls

Our current work in the area of control design is focused on improving the robustness of the system. Control delegation is a challenge when local nodes do not guarantee participation. In the power grid, local consumers or distributed generators may not comply immediately or dependably to commands sent out by a higher level controller. In order to meet this challenge we are currently studying the necessary conditions to assure that a given control action will be executed in a 'safe' manner with favorable stochastic properties. In an effort to do this we are also working with NIST to develop a standardized rule exchange format. Looking forward we would like to use the state of the art in path planning and optimization techniques to produce intelligent trajectory maps for the higher level controller; the idea being that we can express the uncertainty about local nodes and control authority as constraints to a non-linear, stochastic planner.

E. Conclusion

This paper discusses the important role which clock synchronization plays in the present and future of the power grid. Devices increasingly incorporate clock synchronization in some form in order to perform coordinated actions in spatially distributed networks. In turn, the presence of clock

[1] OPNET Modeler provided by OPNET Inc., www.opnet.com

synchronization affects the way models are created. Past work has demonstrated that by including the inherent bounds placed on device performance by synchronization early in model synthesis, more accurate and less computationally intense models can be developed than otherwise. These models and the devices are limited by network performance. As new communication mediums and clock synchronization protocols are developed, the devices are able to truly take advantage of synchronization. As a result, new control algorithms can be developed which leverage both the changes in device performance and the newly available information of time. The result of the work is four projects centered around developing performance characteristics of clock synchronized networks, and useful control applications.

VII. Acknowledgments

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References

[1] K. Behrendt and K. Fodero, "The perfect time: An examination of time-synchronization techniques," in *Proc. Western Protective Relay Conference*, 2006.

[2] K. M. et al., "Exploring the IEEE standard C37.118-2005 synchrophasors for power systems," *IEEE Trans. on Power Delivery*, 2008.

[3] R. E. Wilson, "PMUs," *IEEE Potentials*, vol. 13, pp. 23–26, 1994.

[4] P. Komarnicki, C. Dzienis, Z. Styczynski, J. Blumschein, and V. Centeno, "Practical experience with pmu system testing and calibration requirements," in *Proc. IEEE PES General Meeting*, 2008.

[5] P. Korba, M. Larsson, and C. Rehtanz, "Detection of oscillations in power systems using kalman filtering techniques," in *Proc. IEEE CCA*, 2003.

[6] E. Bompard, R. Napoli, and F. Xue, "Analysis of structural vulnerabilities in power transmission grids," *International Journal of Critical Infrastructure Protection*, vol. 2, pp. 5–12, 2009.

[7] D. Anand, J. Fletcher, Y. Li-Baboud, J. Amelot, and J. Moyne, "Using clock accuracy to guide model synthesis in distributed systems: An application in power grid control," in *Proc. IEEE ISPCS*, 2010.

[8] J. C. Eidson, *Measurement, Control, and Communication Using IEEE 1588*. Springer London, 2006.

[9] Y.-S. Li-Baboud, X. Zhu, D. Anand, S. Hussaini, and J. Moyne, "Semiconductor manufacturing equipment data acquisition simulation for timing performance analysis," in *Proc. IEEE ISPCS*, 2008.

[10] K. Harris, S. Balasubramanian, and A. Moldavansky, "The application of IEEE 1588 to a distributed motion control system," tech. rep., Rockwell Automation, 2004.

[11] D. Anand, J. Fletcher, Y. Li-Baboud, and J. Moyne, "A practical implementation of distributed system control over an asynchronous ethernet network using time stamped data.," in *Proc. IEEE CASE*, 2010.

[12] L. Ljung, *System Identification: Theory for the User*. Prentice Hall, 1987.

[13] D. Anand, D. Sharma, Y. Li-Baboud, and J. Moyne, "EDA performance and clock synchronization over a wireless network: Analysis, experimentation and application to semiconductor manufacturing," in *Proc.IEEE ISPCS*, 2009.

[14] J. Amelot, J. Fletcher, D. Anand, C. Vasseur, Y. Li-Baboud, and J. Moyne, "An IEEE 1588 time synchronization testbed for assessing power distribution requirements," in *Proc. IEEE ISPCS*, 2010.

[15] T. Skeie, S. Johannessen, and O. Holmeide, "Timeliness of real-time ip communication in switched industrial ethernet networks," *IEEE Transactions on Industrial Informatics*, 2006.

[16] M. Chenine, *Wide Area Monitoring and Control Systems - Application Communication Requirements and Simulation*. PhD thesis, KTH, Royal Institute of Technology, 2009.