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Abstract. A robust technique is presented for auto-aligning nanostructures to slow-etching planes during crystallographic etching of silicon. Lithographic mask patterns are modified from the intended dimensions of the nanostructures to compensate for uncertainty in crystal axis orientation. The technique was employed in fabricating silicon nanolines having lengths of 600 nm and widths less than 5 nm, subjected to intentional misalignment of up to ±1 deg. After anisotropic etching, the auto-aligned structures exhibited as little as 1 nm of width variation, as measured by a critical dimension atomic force microscope, across 2 deg of variation in orientation. By contrast, the widths of control structures fabricated without auto-alignment showed 8 nm of variation. Use of the auto-alignment technique can eliminate the need for fiducial-based alignment methods in a variety of applications. [DOI: 10.1117/1.JMM.11.2.023005]

Subject terms: auto-alignment; line width; nanoline; anisotropic etching; KOH; TMAH; crystallographic etching; critical dimension-atomic force microscopy.

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1 Introduction

The technique of crystallographic etching of silicon[1–4] has enabled a wide variety of applications in micro- and nano-technology, ranging from high-power metal-oxide semiconductor (MOS) transistors,[5] to inkjet nozzles,[6] to pressure sensors,[7] to accelerometers,[8] to optical waveguides.[9] Recently, the technique has garnered increased interest for applications requiring narrow linear nanostructures, such as quantum wires[10] and atomic force microscopy (AFM) calibration standards,[11–13] as well as those requiring tall sheet geometries with nanoscale dimensions, such as fin-shaped field-effect transistors (finFETs)[14] and silicon tunnel barriers.[15] The high aspect ratios and smooth sidewalls required for these applications can be achieved through crystallographic etching only if the pattern defining the shape of the nanostructure is well aligned to the crystal axes of the material to be etched.

Numerous techniques for performing accurate alignment have been proposed. The simplest of these is to mechanically align the etch mask to the wafer flat during lithographic patterning, which provides crystal axis alignment to within 1 deg.[16] When greater accuracy is required, the crystal axes can be identified by cleaving the wafer or by etching fiducial structures including rosettes, forks, hexagons, or rectangular windows.[15,17–21] These techniques, though effective, are associated with increased process complexity and reduced yield.

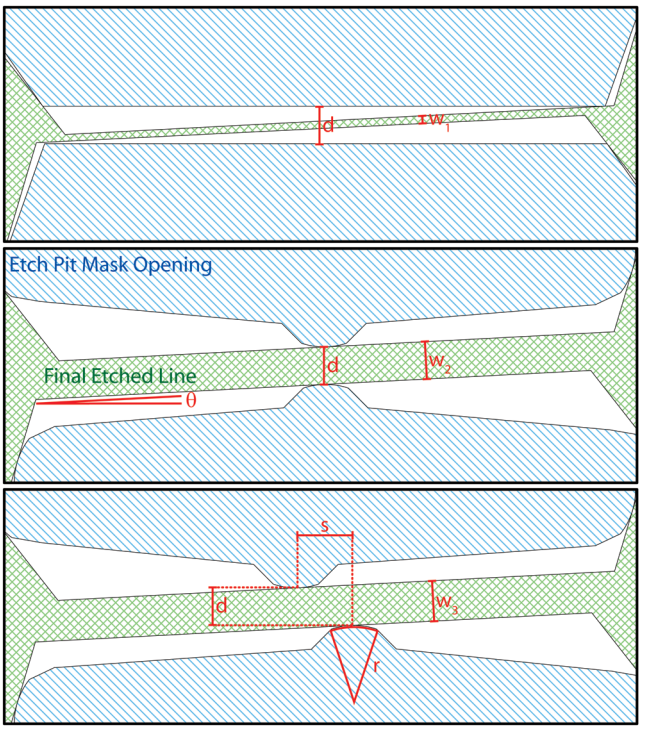

Fig. 1 Three mask designs for fabricating a long, narrow nanoline in (110)-oriented silicon, subject to crystal axis misalignment (θ). Mask openings are shown in blue diagonal hatch, and structures resulting from crystallographic etching are shown in green cross hatch. (Top), When the mask design exactly matches the desired nanostructure, small misalignments cause the actual width of the line, w, to be much smaller than the designed width, d. (Middle), If only one point of the mask opening touches each face of the desired nanostructure, the line width, w, becomes insensitive to small crystal-axis-alignment errors. (Bottom), Separating the contact points of adjacent faces by a small distance, s, makes it possible to fabricate structures with widths below the resolution of the lithography system, even if process bias forces the designed width to be less than zero. The structures remain insensitive to crystal axis misalignment.

Narrow linear nanostructures are particularly vulnerable to alignment errors, as illustrated in Fig. 1 (top). For example, a 600-nm-long nanowire fabricated from (110)-oriented silicon with a masked width of 20 nm would lose over half its width to an alignment error of 1 deg. To control the width of the nanowire to within 1 nm, an alignment uncertainty less than ± 0.095 deg would be required.

In this article, we describe a technique for designing etch mask patterns that compensate for alignment offsets, so that long, narrow nanostructures can be fabricated by crystallographic etching even in the presence of considerable uncertainty regarding the orientation of the crystal axis. We discuss the sensitivity of the technique to crystal axis rotations and demonstrate the fabrication of 600-nm-long high-aspect-ratio lines having widths less than 5 nm, that are robust to rotations of ± 1 deg. We discuss how this technique can accommodate limitations in the resolution of the lithography system and show that these accommodations contribute little or no additional sensitivity.

2 Etch Mask Design

To design a mask that will auto-align to a substrate's crystal axes when subjected to a crystallographic etchant, the desired final structure is first defined by a set of convex polygonal etch pits whose edges all lie along slow-etching planes in an assumed crystal axis orientation. These etch pits are then defined by holes in the etch mask, as shown in Fig. 1 (middle), such that exactly one point on the border of each hole lies along each assumed etch pit edge. During the etch process, the substrate material will dissolve so that slow-etching planes form a convex polygonal boundary around the hole in the mask. The etched boundaries will closely match the shape, size, and position of those defined in the assumed crystal axes, but will be rotated to match the real orientation of the crystal.

In practice, the lithography system used to define the etch mask will have finite resolution, so the contact points between the etch pit edges and the mask holes must exhibit some continuous curvature. In addition, when features are required whose dimensions are below the line resolution of the lithography system, the contact points of adjacent etch pit edges must be laterally separated from one another, as shown in Fig. 1 (bottom). This lateral separation is analogous to subresolution approaches based on resist pattern shifting.[22] The effects of corner rounding and point separation on the sensitivity of auto-aligned structures to crystal axis offsets can be modeled geometrically, producing the following equation:

$$w = s \cdot \sin\theta + d \cdot \cos\theta + 2r \cdot (\cos\theta - 1) + b, \tag{1}$$

where w is the width of the etched line, d is the designed width of the line in the layout, θ is the offset between the assumed and real crystal axes, r is the radius of curvature of the contact points, s is the separation along the assumed crystal axis of the centers of the arcs defining those points, and b is the process bias. The equation is linear and independent of r to within a small-angle approximation. In small-angle cases when $s = 0$, the equation becomes independent of θ as well.

3 Fabrication

To evaluate the auto-alignment technique, three sets of nanolines were fabricated in (110)-oriented silicon by potassium hydroxide etching using the designs shown in Fig. 1. The nanolines were designed to be 600 nm long with widths ranging from 40 nm down to -10 nm. The structures with negative design widths were included to account for the possibility of process bias. These negative-design-width structures were only possible for features using the offset auto-alignment technique, since the design width is defined as the separation between parallel lines drawn tangential to the semicircles shown in Fig. 1 (bottom). The first set of nanolines was designed with the control pattern (Fig. 1, top), the second with the auto-alignment pattern with zero lateral separation (Fig. 1, middle), and the third with 60 nm of lateral separation (Fig. 1, bottom). For the auto-aligned nanolines, the contact points between the mask holes and the assumed etch pits were defined by arcs having a 50-nm radius, which is well within the resolution limits of the electron-beam lithography system employed for the tests.

Fabrication of the silicon nanolines began with the deposition of 22.5 nm stoichiometric silicon nitride onto a 100-mm-diameter, p-type, (110)-oriented silicon wafer by low-pressure chemical vapor deposition. The wafer was then spin-coated with hydrogen silsesquioxane (HSQ) resist to a thickness of 70 nm and exposed with a vector-scan electron beam lithography system at an area dose of

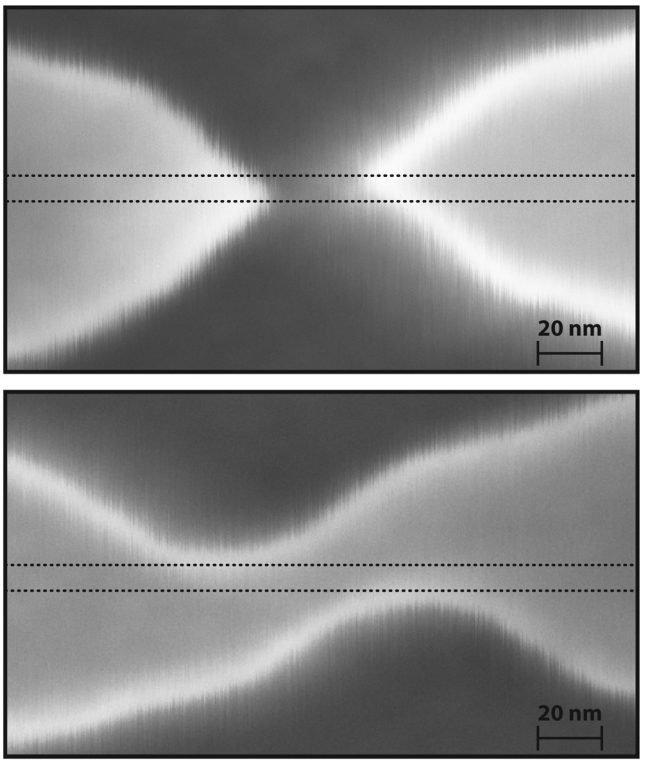

Fig. 2 The effect of lateral point separation on pattern resolution. (Top), Hydrogen silsesquioxane negative electron-beam resist, patterned for auto-alignment without point separation. (The intended nanostructure is the area between the dotted lines.) Underexposure occurs where the width of the exposed region is below the resolution of the lithography system. (Bottom), The same nanostructure is patterned using 60 nm of lateral separation between the two contact points. Underexposure does not occur, allowing realization of nanostructures having dimensions below the resolution of the lithography system.

4000 $\mu C/cm^2$, using a 3-nm-spot-size beam and 0.5-nm pixel resolution. The pattern was written repetitively at 0.5 deg increments from $\phi = -1$ deg to $\phi = 1$ deg, where ϕ is the angular offset relative to the assumed orientation of the [111] crystal axis. After exposure by the electron beam, the samples were developed in tetramethylammonium hydroxide at a mass concentration of 25% and cured in oxygen plasma.

The electron beam lithography system was unable to write nanolines from the control set whose designed width was less than 8 nm. Below this width, adjacent holes in the control structures' etch masks were merged. Nanolines with the auto-alignment etch mask and no lateral separation of the etch pit contact points could not be written with designed widths less than 6 nm. Below this width, adjacent openings in the etch masks of these structures were also merged, as shown in Fig. 2 (top). There was no difficulty writing any of the etch mask patterns for nanolines designed for auto-alignment with 60 nm of lateral separation between the contact points, including those patterns with negative design width. An example pattern is shown in Fig. 2 (bottom).

The etch mask pattern defined in HSQ resist by electron-beam lithography was transferred into the silicon nitride layer by reactive ion etching in tetrafluoromethane and oxygen plasmas. The wafer was then cleaned according to the RCA process[23] and transferred without drying into a potassium hydroxide bath at 50°C, where it remained for 3 min. After removal from the etch bath, the wafer was spray-rinsed with deionized water and spun dry. The silicon nitride hard mask was then stripped in heated phosphoric acid at 180°C, followed by rinsing in deionized water and spinning dry. An electron micrograph of a representative nanoline is shown in Fig. 3.

4 Characterization

The completed nanolines were characterized by critical dimension (CD)-AFM to determine their final widths and

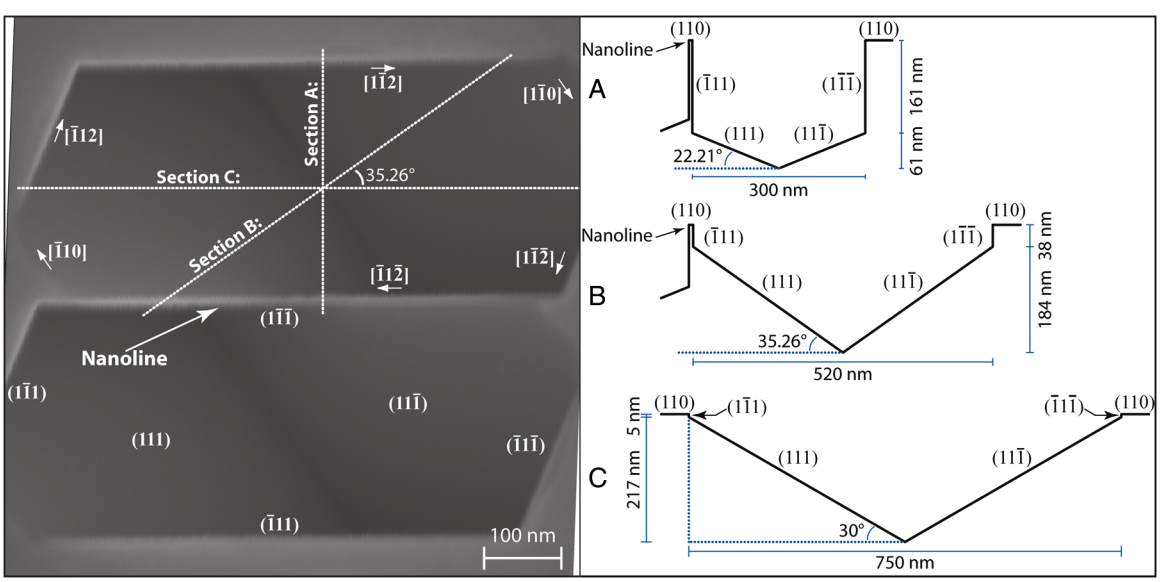

Fig. 3 Annotated electron micrograph of an 8-nm-wide nanoline fabricated using auto-alignment. The nanoline, in the middle of the image, is defined by two etch pits: one above it and one below it. The six {111}-oriented crystal planes defining the lower etch pit are identified by their Miller indices. On the upper etch pit, the lines of intersection between the {111} planes and the (110) surface of the wafer are identified. Three cross-sections (labeled A, B, and C) are shown to illustrate the geometry.

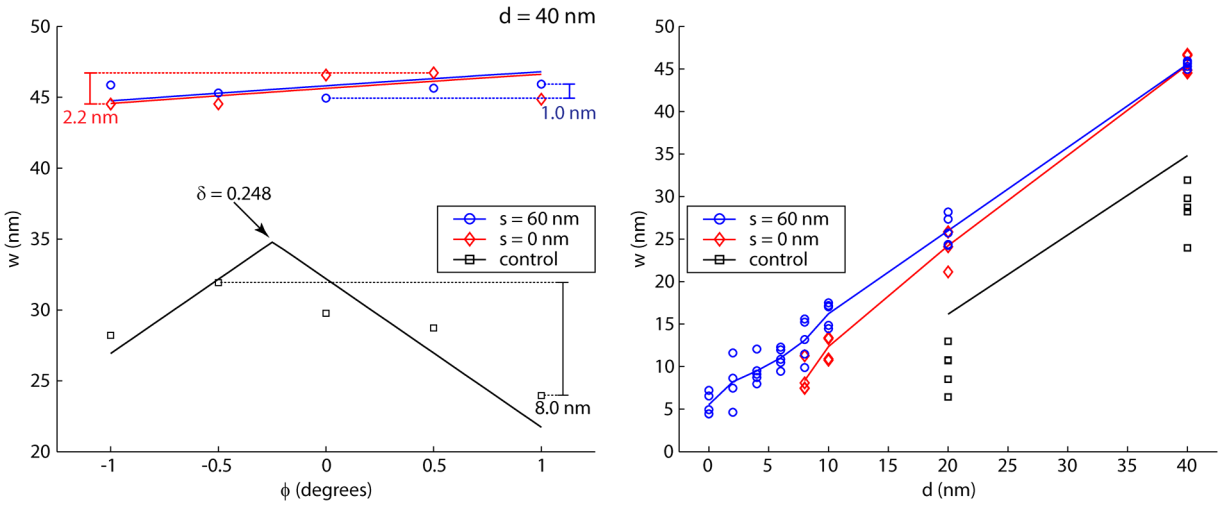

Fig. 4 Nanoline width, w, versus pattern offset angle, φ (left), and designed width, d (right). Data from auto-aligned structures appear in blue and red, whereas data from control structures are shown in black. Auto-aligned structures with lateral separation (s) of 0 and 60 nm are shown. On the left, solid lines show Eqs. (1) and (2) fitted for process bias, b, and wafer misalignment, δ. Width variation in the control structures is a systematic function of the offset angle, whereas the width variation of auto-aligned structures is smaller and largely unrelated to offset angle. On the right, solid lines show the calculated linewidth for perfect crystal alignment ($\varphi = -0.248$ deg), reflecting the process bias for each design width. Lateral separation of $s = 60$ nm reduces process bias variation and allows smaller structures to be fabricated.

their sidewall profile. Unlike conventional AFMs, the CD-AFM can directly access and measure feature sidewalls, providing an exceptionally accurate measurement of lateral dimensions. It does this by not only vibrating the AFM tip in the direction normal to the plane of the sample under test, as conventional AFMs do in tapping mode, but also dithering in the lateral direction at a lower frequency.[24] The specific CD-AFM used for analysis of the nanolines presented here is implemented as a reference measurement system and is calibrated with samples that are closely traceable to the SI definition of length.[11–13,25]

The widths of the nanolines, as determined by the CD-AFM study, are shown in Fig. 4, and a representative CD-AFM image from the data set is shown in Fig. 5. Each value in Fig. 4 represents the average width of a 200-nm segment of the nanoline measured at a depth of 75 nm below the top surface of the feature. For nanolines with a designed width of 40 nm, the control structures exhibit width variation of 8 nm over the domain $\phi = -1$ deg to $\phi = 1$ deg. The auto-aligned structures with no lateral separation vary by 2.2 nm over the same domain. The width variation of the auto-aligned structures with 60-nm lateral separation was only 1.0 nm. Flared or "CD" tips were used for all of the nanoline measurements, since the geometry of these tips is optimized for imaging vertical sidewalls. Specifically, we used CD tips having a round cross-section and nominal width of 50 nm. The size of the AFM scan region for all imaged samples was 200 by 400 nm, with 256 lines per image taken at an approximate scan rate of 0.477 Hz. Note that CD-AFM does not operate with a fixed lateral scan rate; the tip-sample position is controlled with respect to both lateral and vertical axes. A step size of 1 nm was used for both the lateral and vertical axes. The vertical motion perpendicular to the sample surface was restricted to 120 nm. This enabled acquisition of only the nanoline linewidth data needed for the analysis without exposing the tip to additional risk of damage and wear. The sources of uncertainty in the AFM measurement are divided into types A and B. Type A uncertainty sources are evaluated by statistical methods, whereas type B sources are evaluated using some combination of physical models, measured data, or assumptions about the probability distribution of possible error sources. The main uncertainty sources in the results shown in Fig. 4 are type A uncertainty sources-in this case, the repeatability of linewidth measurements. That value is 0.45 nm. Other uncertainty sources include the AFM tip-width calibration, scale calibration factor, and the nonlinearity of the scanner, as well as cosine error. Assuming uncorrelated errors, a root mean square propagation yields combined standard type A uncertainty values of 0.58 nm for the 45-nm features and 0.57 nm for the 4.4-nm features. A more detailed discussion of CD-AFM uncertainties and measurements of etched nanostructures is available elsewhere.[26] The widths of the control structures can be fitted to the equation

$$w = d\,\cos(\theta + \phi) - |L\,\sin(\theta + \phi)| + b, \tag{2}$$

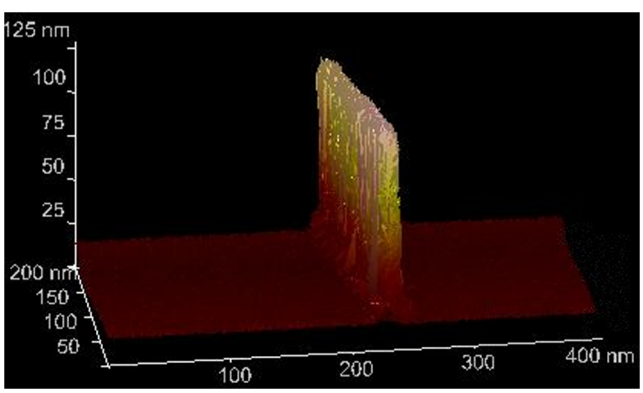

Fig. 5 A representative CD-AFM scan of a silicon nanoline fabricated by crystallographic etching using the auto-alignment technique. The scan, which has been calibrated against samples that are closely traceable to the SI definition of length,[11–13,25] shows an average line width of 8.49 nm, measured at 75 nm from the top.

which, when maximized with respect to ϕ, yields the offset between the assumed crystal axis and the real crystal axis, as shown in Fig. 4. This offset was found to be 0.25 deg. The process bias, b, for each of the three sets of nanolines can then be estimated by interpolating the corresponding width curve at zero angular offset, according to Eqs. (1) and (2). Process biases for the control structures, the zero-offset auto-aligned structures, and the 60-nm-offset auto-aligned structures were -5.2, 5.4, and 5.5 nm, respectively, for designed widths of 40 nm. These biases exhibited slight variation with decreasing width as shown in Fig. 4 (right). The smallest line fabricated using the 60-nm-offset auto-alignment pattern was 4.4 nm; it was noted that even narrower lines survived the etch process but collapsed due to surface tension during drying.

The quality of the nanolines, as measured by line edge roughness and sidewall angle, was largely unaffected by the auto-alignment technique. Nanolines patterned with auto-alignment but no pattern offset exhibited an average roughness and sidewall angle of 0.75 nm and 89.99 deg, respectively, whereas nanolines with auto-alignment and 60 nm offset averaged 0.78 nm and 90.41 deg. The control structures exhibited average roughness of 0.71 nm and average sidewall angle of 89.94 deg.

5 Conclusions

In summary, this article contains a description of an auto-alignment technique for accommodating crystal axis uncertainty during crystallographic etching. The technique is applicable when the orientation of the crystal axes of the material to be etched is known to within some small uncertainty, as is the case for SEMI standard prime-grade silicon wafers. It is particularly beneficial when applied to long, narrow, linear nanostructures of the type required for finFETs, quantum wires, and linewidth calibration standards, the latter application being a principal target of this technique. The technique has been tested for etching silicon in potassium hydroxide solution and has been shown to be compatible with electron beam lithography, including subresolution approaches based on resist pattern shifting. A simple geometric equation has been used to predict the variation in the width of patterned structures due to crystal axis misalignment, and it has been shown that when employing the auto-alignment technique the variation can be held beneath 1 nm. The auto-alignment technique can be used in place of more complex fiducial-based alignment protocols, simplifying fabrication of nanostructures and nanodevices.

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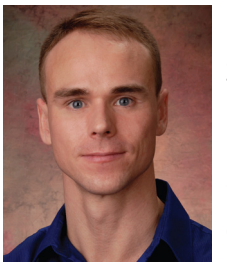

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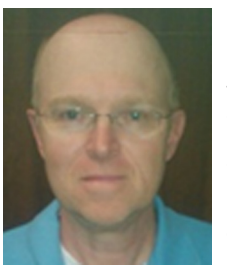

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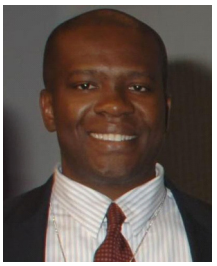

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Richard A. Allen is a physicist in the Semiconductor and Dimensional Metrology Division of the National Institute of Standards and Technology (NIST). His research interests include developing metrology test structures and standards for 3D stacked ICs, microfluidics, MEMS, and microelectronics applications. He received his BS and MS, both in physics, from Rensselaer Polytechnic Institute, Troy, New York in 1982 and 1984, respectively and the MBA from Columbia Union College (now Washington Adventist University), Takoma Park, Maryland in 2007. Since May 2011, he has been the NIST assignee to the 3D Enablement Center of SEMATECH, Albany, New York. At SEMATECH, he is leading activities in standards for 3D Stacked ICs. Prior to joining NIST in June 1990, he worked at the Jet Propulsion Laboratory in Pasadena, California where he developed test structures for *in-situ* monitoring space radiation effects in the VLSI Technology Group and at College Park Software in Altadena, California, where he worked on the development of LISP-based expert systems tools. He is a member of the American Physical Society and a senior member of the Institute for Electrical and Electronics Engineers.

Jon Geist: biography and photograph not available.