A New Interface Defect Spectroscopy Method

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***Abstract*— A new interface defect spectroscopy method based on variable height charge pumping capable of observing the amphoteric nature of Si/SiO$_2$ interface states in production quality sub-micron devices is demonstrated. It can help to resolve the long standing debate about the true nature of Si/SiO$_2$ interface states. Additionally, we show that this is a powerful technique for studying other important material systems.**

Keywords; interface states, P$_b$ centers, charge pumping

I. INTRODUCTION

There is a long standing debate on whether P$_b$ centers account for all electrically observed Si/SiO$_2$ interface states. The inability to establish the amphoteric nature of Si/SiO$_2$ interface states in high quality samples is a key obstacle for resolving this issue. In this work, we introduce a new interface defect spectroscopy method based on variable height charge pumping and report the amphoteric signature of Si/SiO$_2$ interface states in production quality samples for the first time. The new technique is demonstrated on submicron size devices, highlighting the exceptional level of sensitivity.

Our new technique is a modified charge-pumping (CP) measurement. When applied to production quality pure SiO$_2$ MOSFETs with negligible bulk trapping centers, we can be confident that the CP signal is due only to interface states. Fig. 1 shows the key result demonstrating the new technique. The characteristic double peaks (which maintain their shape and increase in magnitude following moderate gate stress) at the expected energy locations clearly show that the interface states are of the P$_b$ center family. Please note the absolute number of defects (left vertical axis) and the defect density (right vertical axis). This is the first ever reported double peak signature on a high quality submicron device.

All previously reported successful electrical observations of the amphoteric nature of Si/SiO$_2$ P$_b$ centers relied on devices with very poor quality interfaces (D$_{it}$>10^{11} cm^{-2}) and/or very large device areas [1-14]. In some cases, the amphoteric nature was only observable after very harsh irradiation [2, 7, 8, 12, 14]. In addition to a high density of interface states, these samples also exhibit high densities of non-interface bulk trapping centers. As most electrical measurements are not capable of truly excluding non-interface defects, quantitative disagreements are common when comparing to P$_b$ center data obtained from electron spin resonance. Such disagreements fueled the controversy [15, 16].

Using CP to perform defect spectroscopy is not new [1-3, 11]. Previous attempts are based on trapped charge emission which has difficulty probing mid-gap and (in some cases) require complicated gate voltage pulse trains that limit access near the band edges (slower pulse rise time (t$_r$) and fall time (t$_f$)) [1-3, 11]. Our approach utilizes a simple square wave, relies on charge capture rather than emission, is able to probe defects through mid-gap, and allows the use of faster t$_r$ and t$_f$ to probe closer to the band edges. Additionally, **choosing a frequency low enough to ensure complete trap filling is the key new aspect** in our approach.

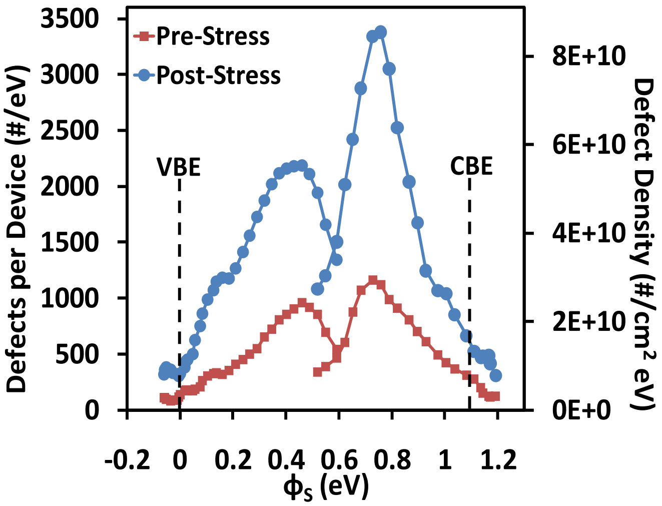

Fig. 1: Amphoteric nature of Si/SiO$_2$ interface states in a production quality submicron device. This is the first ever reported double peak signature on a high quality submicron device.

II. EXPERIMENTAL

The devices used are production quality 16.45 x 0.24 µm^2 nMOSFETs with 5.5 nm pure SiO$_2$ gate dielectrics (V$_{th}$ ≈ 0.65 V). CP was performed by applying a simple square wave (provided by a commercially available pulse generator) to the gate while shorting the source and drain to ground. The substrate (charge pumping) current (I$_{CP}$) was measured with an ultra-low noise current preamplifier and recorded with a digital storage oscilloscope for several seconds. The CP current was then averaged offline to further increase the signal to noise ratio. This approach allowed us to accurately measure very small currents with excellent sensitivity. Our CP method is very similar to the variable pulse height method [17]. The upper half of the band gap is measured by setting the pulse low level (V_{GL}) at strong accumulation (V_{GL} = -2 V in these samples) while sequentially stepping the pulse high level (V_{GH}) from strong inversion to depletion. The lower half of the band gap is measured by setting V_{GH} at strong inversion (V_{GH} = 1 V in these samples) while sequentially stepping V_{GL} from strong accumulation to depletion. By varying the pulse height in this fashion, we can obtain CP current as a function of the probed energy window in the band-gap. Fig. 2 schematically illustrates the pulse conditions. To reduce emission loss and push the measurement window closer to the band edges, t_r and t_f are both held at 2.3 ns for all measurements (unless otherwise noted). Based on instrumentation limits, slower t_r and t_f times can be used, but this will result in greater emission loss and will reduce how close to the band edges one can probe. Alternatively, faster t_r and t_f can be used to push the measurement window closer to the band edges, but care must be taken to avoid CP geometric effects based on the device dimensions as well as waveform distortion. Additionally, for more careful analysis of the band edges, the slope of the pulse transition for various pulse heights should be considered.

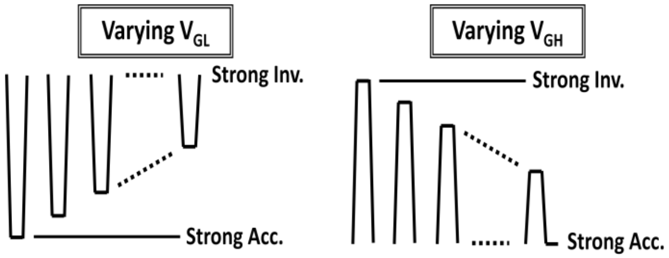

Fig. 2: Schematic illustration of the pulse bias conditions. For the case of fixed strong inversion (left), the pulse low level (V_{GL}) is sequentially stepped from strong accumulation to deep depletion. For the case of fixed strong accumulation (right), the pulse high level (V_{GH}) is sequentially stepped from strong inversion to deep depletion.

For each pulse bias level, the CP current was measured at 1, 2, 3, and 4 kHz. Such low frequency is of key importance and separates our approach from the conventional variable pulse height method, as explained later. Since the CP current should be zero at a CP frequency of 0 Hz, a linear plot of CP current vs. frequency for each pulse bias level allows for leakage current and amplifier offset to be corrected (by subtracting off the linear fit y-intercept value) and the CP current at a 2 kHz to be extracted accurately. Fig. 3 illustrates corrected CP current vs. frequency for two different pulse bias levels along with their respective linear fits. In thinner gate dielectrics, correcting for gate leakage current with this approach becomes difficult as the gate leakage current starts to overwhelm the CP current. Since the ratio of gate leakage current versus CP current can become quite large, this correction looses accuracy and introduces errors in the extracted measurement results. Thus, we estimate that below about 2 nm of pure SiO_2 gate oxide thickness, the gate leakage current becomes large enough such that this method should be used carefully and the results viewed with care.

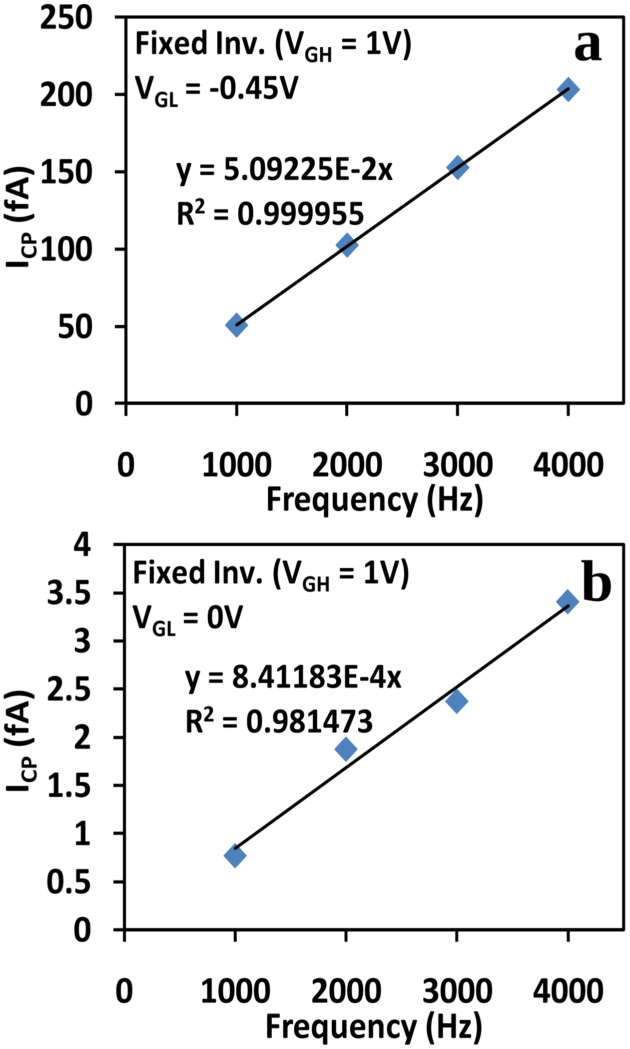

Fig. 3: Linear fits of CP current vs. frequency at fixed inversion for (a) V_{GL} = -0.45 V and (b) V_{GL} = 0 V after correcting for gate leakage current and amplifier offset. The linear fit (R^2) is clearly degraded in (b) indicating the onset of incomplete trap filling, as discussed in the text.

I. DISCUSSION

As mentioned above, choosing a CP frequency low enough to ensure complete trap filling is a vital necessity for an accurate measurement. When we vary the pulse height deep into depletion, the carrier density can become very small. Since the time constant associated with trap filling is inversely proportional to the number of carriers available to fill, the trap filling time becomes longer as the pulse height is pushed deep into depletion. This means that traps expected to participate in the CP process are not filled completely if sufficient time (slow enough frequency) is not given. The result is an apparent loss of measured CP current which detrimentally alters the measurement result. This is the reason we extract our CP results at 2 kHz.

The specific frequency is experimentally determined by measuring the CP current as a function of frequency for various pulse bias conditions as shown in Fig. 4 for the case of fixed accumulation (fixed V_{GL}). It clearly demonstrates that as the frequency is increased and/or V_{GH} is reduced into depletion, charge per cycle decreases; this is caused by insufficient time to ensure complete filling of the traps within the measurement window and **must** be avoided.

Charge per cycle is essentially the number of traps participating in the CP process and is extracted by dividing the measured CP current by the CP frequency and electronic charge (q). When incomplete trap filling is avoided, we equate "charge per cycle" to "defects per device" since all traps within the probed energy window in the device are contributing to the CP current. **Ensuring the measured result is free from incomplete trap-filling effects separates our new method from conventional variable pulse height CP**, which is usually done at higher frequency.

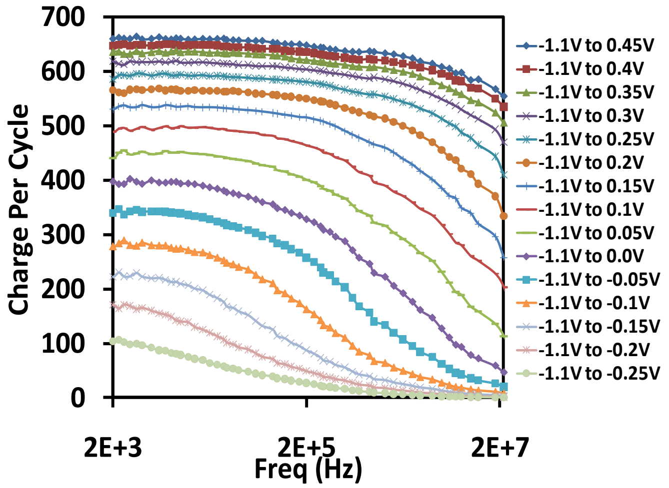

Fig. 4: Charge per cycle vs. frequency at fixed accumulation for a variety of different pulse high levels (V_{GH}). As the CP frequency is increased and/or V_{GH} is pushed into depletion, charge loss due to incomplete trap filling clearly occurs. **This effect must be avoided**.

Fig. 5 shows the measured defect density (#/cm^2) vs. gate voltage (V_G) for both fixed inversion and fixed accumulation cases at a frequency of 2 kHz. For the fixed accumulation case, V_G indicates the stepped pulse high level (V_{GH}) and for the fixed inversion case, V_G indicates the stepped pulse low level (V_{GL}). To obtain the defect density, defects per device (explained above) is extracted at 2 kHz and is then divided by the device area. Superimposed in Fig. 5 is the simulated [18] pre-stress capacitance vs. V_G (CV) curve.

It is clear that the defect density in Fig. 5 refers to the total defects within the probed energy window. As we vary V_{GL} (or V_{GH}) we change the probed energy window. By taking the derivative of the measured defect density with respect to V_G, we can extract the density of states (DOS) of the traps participating in the CP process. This derivative is shown in Fig. 6 (the pre-stress curves of Fig. 1) after converting V_G to silicon surface potential (ϕ_s) using the simulated CV curve (superimposed). The left hand curve (extracted from fixed inversion) peaks at about 0.45 eV above the valence band edge (VBE) and the right hand curve (extracted from fixed accumulation) peaks at about 0.76 eV above the VBE.

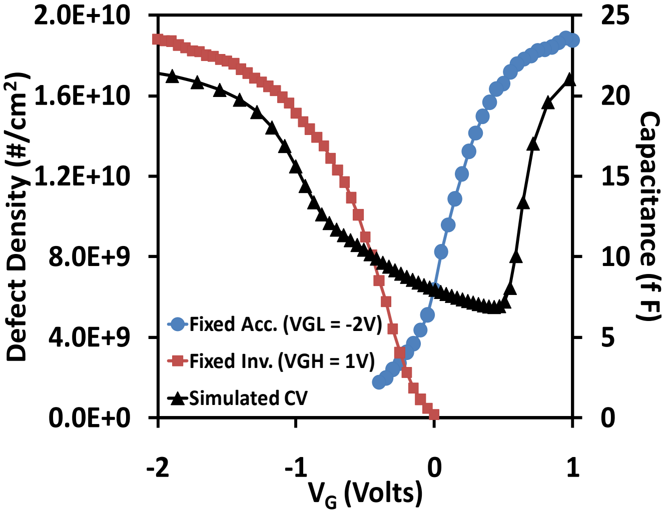

Fig. 5: Defect density (#/cm^2) vs. V_G extracted from the CP current at 2 kHz and a superimposed simulated CV curve. V_G indicates pulse high level (V_{GH}) and low level (V_{GL}) for fixed accumulation and fixed inversion cases, respectively.

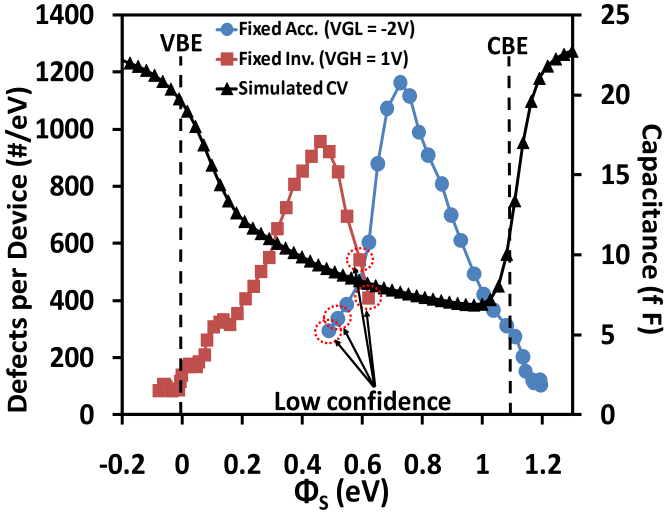

Fig. 6: DOS illustration vs. silicon surface potential (ϕ_S) and a simulated CV curve. The DOS (#/eV) was computed by taking the derivative of the data from Fig. 5 with respect to V_G and ϕ_S was calculated from the simulated CV curve. The indicated data points have low confidence, as explained in the text.

An obvious question is why the two sides of the measured DOS are not in agreement where they overlap? The answer involves the accuracy of the measurement falling off as the pulse height is pushed deep into depletion. As mentioned above, for each pulse bias condition, frequency dependent CP was performed at frequencies of 1, 2, 3, and 4 kHz, and the CP current at 2 kHz was extracted from a linear fit correction. As we push deep into depletion, incomplete trap filling starts to set in (as illustrated in Fig. 4) and the linearity of the frequency dependent CP data will start to degrade (the linear fit R^2 value in Fig. 3b is worse than in Fig. 3a which is in part due to this). Fig. 7a compares the linear fit R^2 values for fixed inversion with V_{GL} = -0.7 V to 0 V. At certain V_{GL} levels (as we push deeper into depletion), the linear fit R^2 value clearly starts to degrade. This is indicative of the on-set of incomplete trap filling (as well as signal to noise degradation). Similarly, the phenomenon is also clearly observed in the fixed V_{GL} case of Fig. 7b. This R^2 approach provides a convenient, objective and stringent method to monitor incomplete trap filling issues.

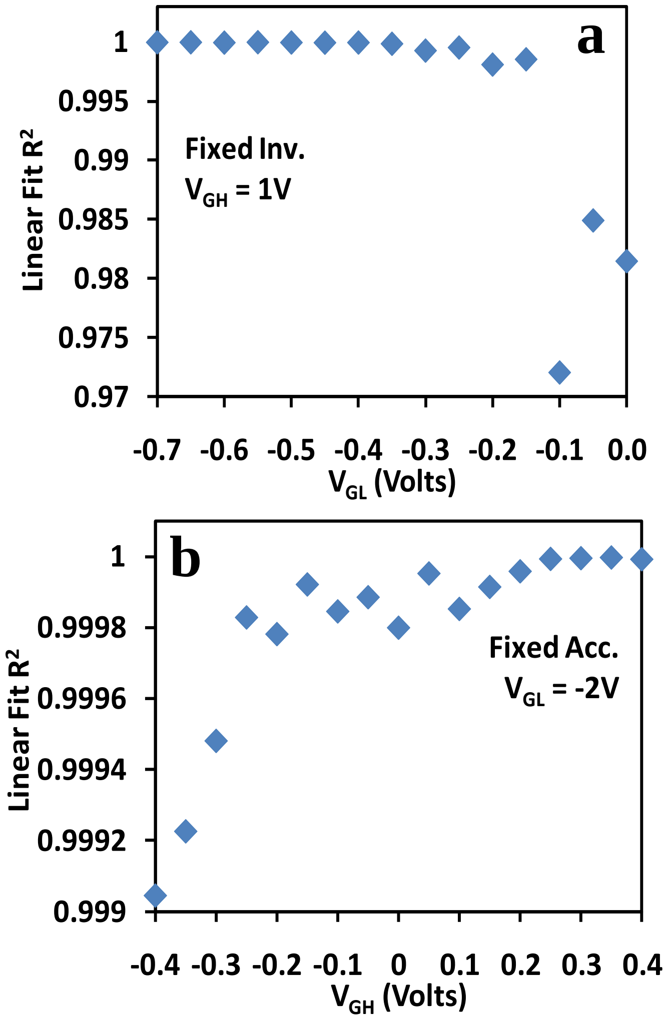

Fig. 7: Liner fit quality (R^2) vs. pulse height for fixed inversion (a) and fixed accumulation (b). As the pulse height is decreased, the linear fit is degraded; the degraded data has low confidence.

Clearly, the reliability of the last three points in Fig. 7a and the first three data points in Fig. 7b should not be trusted. These points are already dropped in Figs. 1 and 6. However, our differentiation routine propagates the influence of these points to the next three points. (We use the Savitzky-Golay method for differentiation, which is formally equivalent to taking a small segment of the curve and fitting it to a second order polynomial, and then differentiating the polynomial [19].) As differentiation tends to amplify small errors, the influence at the first point is significant. The next point is less. From the fourth point on, the influence is no longer there. Based on this consideration, we circle the data points with a low confidence level in Fig. 6, thereby eliminating the disagreement.

To illustrate the new technique and to show that the peak locations are not measurement artifacts, we apply this technique to a different material system, namely SiC/SiO_2. For this system, one would intuitively expect a different DOS distribution than conventional Si/SiO_2 as SiC/SiO_2 could have silicon dangling bonds as well as carbon dangling bonds each with two DOS peaks. Fig. 8 shows the results of applying our new technique on a SiC nMOSFET (400 x 2 μm^2, t_{ox} = 50 nm) and four peaks are observed. Measured CV curves are superimposed and the VBE and CBE markers are estimates only. In this figure, the DOS was extracted at 10kHz, which was experimentally determined to avoid the interface trap filling time issue discussed above, and t_r and t_f were both held at 50 ns to avoid CP geometric effects. This result illustrates the power of this technique when studying different material systems as well as strongly supporting the validity of our Si/SiO_2 DOS peaks.

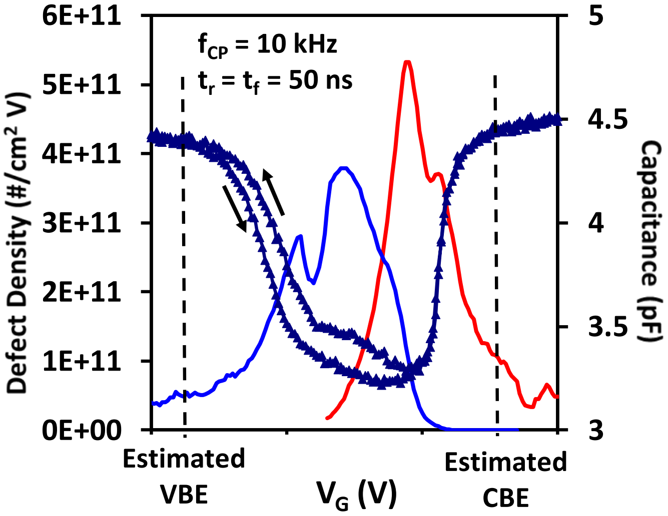

Fig. 8: DOS illustration and a measured CV curve for a SiC nMOSFET. Four peaks clearly appear in the DOS which are intuitively due to silicon dangling bonds and carbon dangling bonds.

II. CONCLUSIONS

We have shown, for the first time, the amphoteric nature of Si/SiO_2 interface states in production quality sub-micron devices with excellent sensitivity and resolution. This work should help resolve the ongoing debate as to whether or not P_b centers are responsible for the "true" electrically measured interface states. Performing the measurements at sufficiently low frequency to ensure complete trap filling separates this method from conventional variable height CP, and is crucial to the accurate extraction of defect density as a function of energy in the band-gap. Furthermore, we have shown that this is a powerful technique for extracting the DOS in other important material systems.

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