Lithography, Metrology and Nanomanufacturing

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Semiconductor chip manufacturing is by far the predominant nanomanufacturing technology in the world today. Top-down lithography techniques are used for fabrication of logic and memory chips since, in order to function, these chips must essentially be perfect. Assuring perfection requires expensive metrology. Top of the line logic sells for several hundred thousand dollars per square meter and, even though the required metrology is expensive, it is a small percentage of the overall manufacturing cost. The level of stability and control afforded by current lithography tools means that much of this metrology can be online and statistical. In contrast, many of the novel types of nanomanufacturing currently being developed will produce products worth only a few dollars per square meter. To be cost effective, the required metrology must cost proportioantely less. Fortunately many of these nanofabrication techniques, such as block copolymer self-assembly, colloidal self-assembly, DNA origami, roll-2-roll nano-imprint, etc, will not require the same level of perfection to meet specification. Given the variability of these self-assembly processes, in order to maintain process control, these techniques will require some level of real time online metrology. Hence we are led to the conclusion that future nanomanufacturing may well necessitate "cheap" nanometer scale metrology which functions real time and on-line, e.g. at GHz rates, in the production stream. In this paper we review top-down and bottom-up nanofabrication techniques and compare and contrast the various metrology requirements.

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Introduction

In 1998, Tennant described the state of the art in nanofabrication and drew attention to the fact that there appeared to be a strong dependence of throughput on feature size for a diverse range of top-down lithographic techniques.[1] Marrian and Tennant produced an updated version of the analysis in 2003[2] and, in keeping with the accelerating pace of technological change, it seems appropriate to examine the current situation. Much has changed in the intervening eight years. In 2003 integrated circuit (IC) technology was at the 120 nm node, just entering the realm of nanotechnology, with microprocessor (MPU) lithographic half-pitches of 120 nm, physical gate lengths – at the then edge of manufacturability – of 65 nm and overlay at a relatively relaxed 35 nm (mean + 3σ). Today, IC's operate deep inside that realm. At the current 32 nm node MPU half-pitches are 38 nm, physical gate lengths are 24 nm and overlay is less than 9.5 nm (mean + 3σ).[3] In 2003, optical lithography operating at a wavelength of 157 nm was the leading contender for production of today's ICs, to be succeeded by extreme ultraviolet lithography (EUVL) operating at 13 nm. In fact, production of leading-edge devices is still accomplished with optical lithography at 193 nm,[4] albeit with the addition of water immersion[5] and strict design rules such as forbidden pitches.[6] This is likely to remain the case for future generations as double patterning techniques become widely deployed.[7,8,9,10]

Over the same time span, there has been an explosive growth in other forms of nanotechnology and, as more and more of the basic science is uncovered, the emphasis is shifting from discovery to production. While many of the unique properties conferred on nanostructures by virtue of their size can be exploited simply by incorporating them into bulk materials in an unstructured fashion, a whole host of additional applications becomes possible once some degree of structure or hierarchy is introduced. Frequently this is because the length scales of different physical processes are mismatched and have to be reconciled. For example, in organic photovoltaic materials the characteristic lengths for photon absorption and exciton diffusion are different,[11,12] but nanopatterning can be used to optimize the device geometry and satisfy both constraints.[13] Alternatively, the desired functionality may require maintaining a precise spatial arrangement on the nanoscale to enable collective behavior, such as resonances in nanophotonic devices.[14]

While existing semiconductor lithography may be appropriate for some applications, it is worth remembering that it has been designed to address a very specific set of requirements that pertain to an extremely complex, high-value product. The majority of the IC industry is centered on the production of a single device (the Complementary-Metal-Oxide-Semiconductor or CMOS transistor), from essentially a single material (silicon) on a single form factor substrate (a rigid 300 mm wafer). The diversity of materials, structures, and applications that reflects the full breadth of the nanotechnology enterprise demands that we consider a similar diversity in patterning techniques. In this

paper we therefore examine the relationship between the constraints on parameters such as critical dimension (CD), placement, CD control, and overlay accuracy, imposed by different classes of nanoscale devices and structures. In addition, we consider the link between throughput and cost per unit area and how this drives the development of high-speed patterning processes. Finally, based on the adage that "you can't make it if you can't measure it", we discuss the role of metrology, and the challenges that must be met to enable profitable nanomanufacturing.

Top-Down Nanofabrication

The microprocessor or logic chip represents the apogee of technical sophistication, with billions of nanoscale devices, working in flawless synchronization, integrated into an area of a few square centimeters. Along with this, the demands on the fabrication technology that enables this are extreme. Feature sizes of less than 40 nm must be controlled to better than 2.5 nm (mean + 3σ) and be spaced a similar distance apart to better than 9.5 nm (mean + 3σ) to properly overlay one lithographic level on the previous level.[15] All of this must take place at a throughput of ≈ 100 to 200 (300 mm diameter) wafers per hour or ≈ (2 to 4) $\times 10^{-3}$ m^2/s ((20 to 40) cm^2/s) and be repeated on the order of 30 times to complete a chip. The need for this degree of control drives the cost of the associated lithographic technology: a cost that can only be borne because of the high value of the product (100 chips/300 mm wafer at 100 dollars per chip ≈ $140000/$m^2$). In addition, the process relies on constant measurements and adjustments taking place inside the lithography tool to maintain dose, focus and alignment during exposure and off-line, using tools almost as complex as the lithography tool itself to ensure that these specifications are being met at all times. It should be noted that, as long as the separate levels are overlayed on each other to the tolerances stated above, the overall IC pattern can be magnified and distorted by several percent and the chip will still function perfectly. This is the reason optical lithography tools are designed and built to independently adjust in-plane x and y magnification, rotation and skew of the projected pattern.[16] The first level does not need to be perfectly scaled as long as all the subsequent levels can be magnified, rotated and skewed to properly overlay it. On the other hand, many MEMs and photonic devices are matched to an external frequency standard and so, unless they can be tuned, must be fabricated with absolute precision.[17]

At this point it is important to comment on the use of CD or "resolution" as the measure of all things. Although the IC technology nodes are typically defined in terms of feature size, making small features is not the primary challenge in semiconductor lithography. As should be clear from the figures given above, making them uniformly, close together, and in the right place is at least as important and possibly more demanding. Satisfying these requirements enables the circuit designer to assume consistent operating voltages and transistor speeds and to develop compact, high-density circuits with improved speed and power-dissipation characteristics. In this section we consider deterministic or "top-down" patterning techniques that can, at least in principle, achieve CD control and overlay accuracy and precision comparable to the feature size being produced.

We begin by discussing an updated version of the first figure from Marrian and Tennant[2] as shown in **Figure 1a**. The graph shows how resolution varies with throughput. The biggest changes between the current graph and original one are the addition of imprint lithography which is significantly off the best-fit line and the fact that the introduction of step-and-scan techniques has significantly improved the resolution of integrated circuit optical lithography with essentially no loss in throughput. The latter change is a result of the industry's efforts to sustain Moore's Law,[18] which dictates that in order to stay profitable, chip features must shrink by a factor of ≈ 0.7 every two years, without loss of throughput or overlay. This is a trend that has been in place for some time[19] and has been sustained most recently in one case by building lithography tools that can align one wafer while simultaneously exposing a second,[20] and in another case by significantly reducing the time required to align a wafer by taking multiple alignment readings simultaneously.[21]

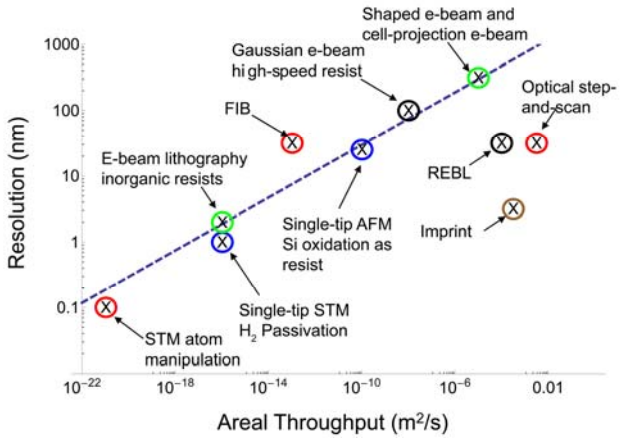

Figure 1a. Resolution versus throughput for a variety of top-down lithographic techniques. The blue line is 3×10^3 nm $\times(\text{Throughput}/(m^2/s))^{0.2}$ and corresponds to the best-fit line from the Marrian and Tennant paper. (REBL stands for reflection e-beam lithography)

In **Figure 1b** we have extended the throughput axis to include very high rate patterning techniques such as inkjet[22] and letterpress.[23] We find that we can now add a second line to the graph that indicates the trend in throughput versus resolution for highly parallelized techniques. Interestingly, while nanoimprint, optical and letterpress lithography all use some form of mask to transfer information in parallel, inkjet printing is a fully digital fabrication technique. Over time, it is likely that this line will move down and to the right (speed and resolution will improve) as mask making techniques for roll-to-roll processing improve and new pattern transfer processes, such as microcontact printing,[24,25] are adapted for high speed. Improving the resolution of inkjet printing is also an active area of research, with systems now capable of producing droplet sizes as small as 05 μm.[26,27,28,29]

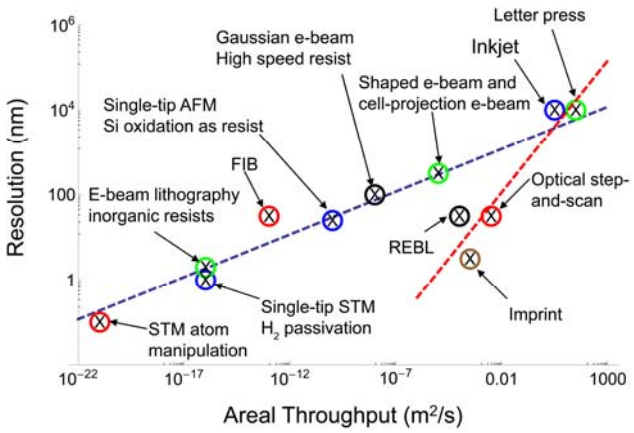

Figure 1b. Resolution versus throughput for a variety of top-down lithographic techniques, with the addition of commercial, high-speed printing processes. The red line is a fit to just the Imprint, Optical Step and Scan, reflection electron-beam lithography (REBL),[52] Inkjet and Letterpress data only and is given by 2×10^3 nm $\times$ (Throughput/(m^2/s))$^{0.6}$. The throughput and resolution numbers used for REBL are those predicted for a fully developed system.

While developments in optical and mechanical systems are necessary to enable progress in optical lithography, they must be matched by improvements in resist technology. However, there are limits for all these systems and the resist may be the first to run up against fundamental limits. Line Edge Roughness (LER), which as the name implies is simply the roughness or deviation in the position of an edge as a function of distance along the edge, is a significant, stochastic component of CD variability.[30] Currently, chemically amplified (CA) resists[31,32] are used almost exclusively in IC manufacturing in order to maximize throughput. Exposing a CA resist releases acid molecules with a number density that depends on the image intensity, hence transferring the mask pattern information to the wafer. After exposure the resist is baked (this is referred to as the Post Exposure Bake or PEB step) which causes the acid molecules to diffuse and deprotect the resist, i.e., convert insoluble resist molecules to soluble ones. In this way, a single photon can effect substantial chemical change in the resist. However, the combination of the statistics governing where the acids are released, which is purely a quantum-mechanical phenomenon, with the diffusion of the acid molecules during PEB and the number of acid molecules required to successfully deprotect the resist leads to an issue known as the Resolution-LER-Sensitivity or RLS tradeoff. Since source brightness is limited,[33] choosing a high throughput means that few photons are available for resist exposure and as a result fewer acid molecules are released. The resulting low number density of acid molecules means that they are therefore, on average, farther apart. To complete the pattern and fill in the volume between the molecules requires increasing the diffusion range of the acid molecules during PEB but this leads to a blurring of the pattern and loss of resolution.[34,35,36,37] Also, the fewer acid molecules the less well defined the pattern, which means ill-defined pattern edges, i.e., edge roughness or LER. A simple analysis leads to the conclusion that it is inherently impossible to have simultaneously a high sensitivity resist requiring fewer photons/exposure, a low LER and good resolution.[38,39,40] This tradeoff is sometimes referred to as the "triangle of death" – a phrase that encapsulates the tension between achieving the desired CD and CD control, and acceptable throughput for optical lithography.

Similar considerations apply to the array of electron-beam[41] and ion-beam[42] fabrication technologies used in the production of nanostructures. Although these techniques are capable of extremely high resolution, they suffer the same constraints regarding the resist material as optical lithography. Small features with low LER can only be realized by using insensitive resist materials.[43] In addition, charged-particle lithography systems are afflicted with space-charge effects.[44] Unlike photons, electrons and ions interact strongly with one another during their passage through the optics of a lithography tool. These interactions lead to perturbations in the particles' trajectories that manifest themselves in three different ways.[45] The Boersch effect describes the changes in velocity along the optical axis caused by particle interactions. These lead to an energy spread in the beam and hence chromatic aberration. Stochastic space-charge effects refer to the random deviations in particle trajectories away from the desired ones that also lead to a blur in the final image. Global space-charge is a result of the beam's tendency to defocus as the particles repel one another and, of the three effects, is the only one that can, at least in principle, be corrected. The net result is that, in order to achieve high resolution, the beam current along a single optical axis must be limited and so, therefore, is the maximum throughput. Charged particle systems tend to be limited to the role of primary pattern generation for techniques that use masks or templates. However, for applications that require a relatively small number of replications of a given pattern, there is still a potential cost advantage if patterning can be done without going to the trouble of fabricating, inspecting, repairing and replicating a mask. There are thus active programs involved in the development of high-throughput maskless techniques. These fall into two groups: those that involve multiple beams[46,47,48,49] in order to limit the current in any one to a level at which space-charge effects are acceptable (though they may still be apparent),[50] and those that use imaging optical systems with an extended beam[51,52,53,54] to achieve the same end. This latter group faces an additional space-charge related effect however. In an imaging system the pattern density varies and this can lead to non-uniformities across the beam. These effectively act as a highly aberrated electrostatic lens element and can cause time-varying, non-uniform blur and distortion across the field,[55,56] which can only be mitigated by careful optical design. It is interesting to speculate that part of the reason for the strong trend in throughput versus resolution originally observed for charged-particle systems[2] is a result of the optimization of optical design for a particular target resolution and the parametric dependence of space-charge effects on factors such as accelerating voltage, column length, beam current and numerical aperture.

Proximal probe methods such as ultra-high vacuum (UHV) scanning tunneling microscope (STM) feedback controlled lithography (FCL)[57] and STM single-molecule[58] and single-atom positioning[59] offer the ultimate in resolution. However, throughputs are not high, with the arrangement of molecules over several square nanometers taking several hours,[60] equivalent to ≈

10^{-20} m^2/s, and hydrogen depassivation lithography[61,62] capable of 10^{-16} m^2/s[63] suggesting that such techniques will be suitable only for very specialized applications. Dip-pen nanolithography (DPN)[64] is another probe-based lithographic approach that does present distinct advantages in terms of its ability to manipulate molecules, including biomolecules,[65] under ambient conditions, though not with the single-atom resolution of UHV-STM. By working at these lower resolutions, similar techniques using arrays of polymer, as opposed to hard material, tips can be operated in a highly parallel fashion[66] to yield throughputs as high as 10^{-7} m^2/s. Scanned probes can also perform lithography in the non-contact mode using the optical near field to expose resist materials. Massively parallel arrays of polymer probes with near-field apertures at the tips have been demonstrated,[67] while in an interesting development, plasmonic lenses flying on an air bearing over a rotating substrate were used to demonstrate a throughput of 10^{-7} m^2/s, with the potential to scale to 10^{-4} m^2/s to 10^{-3} m^2/s, [68] suitable for IC lithography.

Nanoimprint lithography[69,70] is a rapidly emerging technology that does not suffer from the resolution limitations of optical lithography or the throughput constraints that affect charged-particle lithography. If a suitable mask or template can be made, there is nothing intrinsic in the imprint process that precludes the replication of almost arbitrarily small features.[71] Imprint can also avoid the RLS tradeoff since a very high dose can be used to make the mask which therefore can have low LER and good resolution. The technology is, however, 1 x (the feature size on the mask is that same as that on the substrate), unlike optical lithography, which uses a 4 x or 5 x demagnification of the mask. This fact makes mask fabrication for imprint difficult, though not so much as might be imagined. Optical lithography currently makes use of resolution enhancement techniques (RETs) such as sub-resolution assist features[72,73] and optical proximity effect correction (OPC)[74] that require mask features on the order of the minimum wafer CD. Therefore the photomask industry is already dealing with feature sizes close to those required for imprint templates. Since the template makes intimate contact with the substrate for every imprint, the generation of defects caused either by particulate contamination[75] or build-up of resist on the template is a more serious issue. Finally, although imprint lithography is capable of generating extremely small features, it does not yet have the ability to make the kinds of precise scale, shear and distortion corrections[76,77] that enable optical lithography tools to meet the overlay specifications for IC manufacture. For these reasons, the first high-volume commercial deployment of imprint is likely to be in the production of bit-patterned media for hard disk drives.[78,79] The required CDs are smaller and CD control tighter in this application than for ICs, but only a single level of lithography is needed so overlay is not an issue. Interestingly, however, although the long-range feature placement requirements for bit-patterned media are significantly less demanding, the types of short-range placement deviations that arise from "stitching" errors which are tolerated on IC masks are not acceptable for bit patterned media.[80]

With these limitations in mind, various groups have conducted a significant amount of research into reducing or eliminating the potential for overlay errors in nanoimprint lithography. One unique feature of the technology is its ability to structure the imprinted material at several levels simultaneously. Micro-optics have been fabricated in this way for many years[81] and multi-level imprint templates have been proposed as a way of eliminating lithography and processing steps in IC interconnect fabrication.[82,83] Recently, a fully self-aligned process has been demonstrated[84] in the context of roll-to-roll production of flexible electronics. In this case, the substrate is, by definition, not rigid and traditional alignment and overlay techniques would be difficult to implement.

If we consider eliminating the need for any kind of positional control, it turns out that there are still many applications that can be enabled by top-down nanofabrication methods. Nanoparticles with precisely defined shapes and sizes are potentially very useful in drug delivery and medical imaging,[85,86,87,88] photonic bandgap materials, etc. While it is possible to generate significant numbers of particles with conventional[89,90,91] or novel[92] photolithographic methods, these need materials that cross-link or become soluble upon exposure. These constraints can preclude the incorporation of sensitive biologically-active molecules. . In these instances, other techniques can be useful.[93,94] Particle replication in non-wetting templates (PRINT)[95] is one such method that makes use of the particular wetting properties of a fluorinated, elastomeric template to produce discrete particles. In contrast to other nanoimprint methods, these particles are not attached to a residual layer. Thus no post-processing, such as reactive ion etching, is required to separate the particles. It is therefore possible to use or incorporate relatively fragile molecules into the particles. While the throughputs demonstrated so far are comparable with those that can be achieved photolithographically,[96] this type of imprint process has the potential to be scaled up by means of roll-to-roll methods.

Bottom-Up Nanofabrication

Bottom-up nanofabrication makes use of materials or objects, such as nanoparticles, diblock copolymers and DNA[97] that have, typically, a single intrinsic length scale. The interactions in such systems are difficult to control and, so far – while there have been many attempts to integrate disparate collections of nanoscale components into more complex structures – nothing approaching the complexity of the IC, which is deterministic at almost[98] all length scales, has been produced.[99] From the smallest nanoscale features up to the overall device chip size the shape, organization and placement are controlled and coherent. Feature placement accuracy and precision over the entire chip are required for chip functionality. Randomly distributed transistors won't make a functioning chip.

Bottom-up approaches such as block copolymer self-assembly, are, however, making inroads into applications that require this type of long-range order. In particular, it has been shown[100,101,102] that diblock materials can be effectively templated by periodic variations in topography or surface chemistry placed at multiples of the intrinsic diblock domain spacing. This enables conventional lithographic techniques operating at loose pitches, where they function effectively, to produce well-controlled patterns at much higher spatial frequencies.[103,104] In addition, since the feature size variation and LER in the diblock materials is controlled principally by the thermodynamics of the system

and not by the kinds of statistical processes affecting the optical or electron-beam lithographic techniques used to generate the templating patterns, resist and shot-noise related variations can, to some extent, be "healed" by the self-assembly process.[105] The end result of this type of directed self-assembly is the production of very uniform, high spatial frequency, large-area patterns. This approach is being used in the generation of master templates for the imprint of bit-patterned media hard disk drives[106] and also appears promising for extending the range of optical lithography for integrated circuit fabrication[107] with most of the geometries essential to for IC fabrication being replicable with the self-assembled materials.[108]

The two applications discussed above are incremental improvements, in the best possible sense, of existing lithographic technologies. While they extend the lifetime of those technologies they do not represent the real potential of self-assembly methods for producing nanostructures over large areas at high throughputs. In most cases, the interactions leading to self-assembly are quite short-range, which means they respond only to their local environment. Simple topographic or chemical patterns, which can be produced by roll-to-roll nanoimprint or transfer printing respectively, can direct the assembly of diblocks or nanoparticles[109,110] to be coherent or deterministic over large length-scales. These patterned assemblies can themselves be functional, or can be used to pattern functional structures, for example metamaterials with diblock copolymers[111] and nanoplasmonic arrays via colloidal nanosphere lithography.[112] So far, there is very little structural hierarchy in these systems, but we might imagine using a platform such as DNA origami[113] to assemble a collection of nanostructures into a molecularly precise configuration,[114] and then using a directed assembly process to assemble the now-functional origami into an array. If we relax the requirement for long-range spatial coherence, then the utility of self-assembly methods can be extended, for example, to the production of model catalyst arrays of nanoparticles that can help elucidate the critical factors for particular reactions,[115] or to enable the heteroepitaxial growth of single-crystal nanostructures.[116]

Clearly, for structures requiring only modest short-range order, the presence of pattern defects is not an issue. If we return, however, to considering applications in which long-range order and low defect counts are important, self-assembly and directed self-assembly processes pose some novel challenges. Defects generated in top-down fabrication processes may be difficult to get rid of, but are essentially deterministic and can be eliminated by, for example, rigorous approaches to cleanliness. By contrast, bottom-up approaches rely on the combination of thermodynamics and kinetics to generate the structures of interest. This means that, for interactions with finite energies operating over finite times, there will almost always be a significant number of defects present, either as a result of thermal fluctuations (for low energy of formation defects) or kinetic trapping. Hence to include bottom-up approaches in our analysis, we need to add a third dimension that represents the amount of long-range coherence in the structure as shown in **Figure 2**. As indicated in the graph, from the point of view of deterministic top down approaches the lack of long-range coherence can be thought of as defectivity. Alternatively, from the point of view of bottom-up approaches, the new axis – running in the opposite direction – represents increasing complexity in the fabrication process in the sense of having to encode, at the nanoscale, the information required for the system to develop long-range order or coherence at the macroscale.

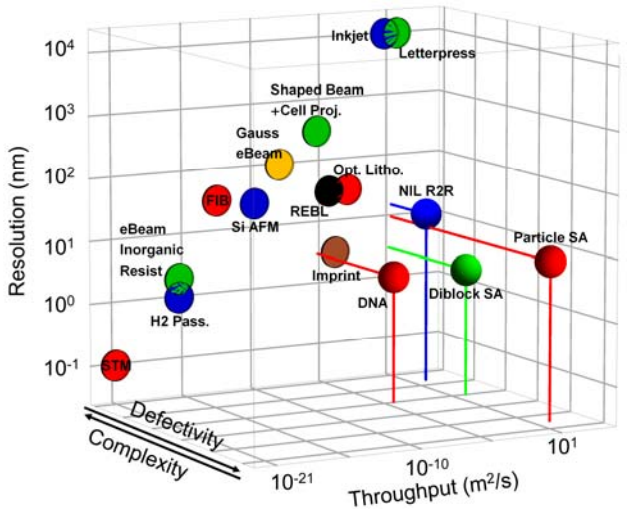

Figure 2. Resolution versus throughput and complexity/defectivity for top-down and directed self-assembly fabrication techniques. (R2R is used to denote roll-to-roll processes).

Metrology

The issues for metrology in nanofabrication are the traditional ones of precision, accuracy, cost and speed coupled with the measurement scale required. Are nanometer scale measurements required, such as the size, shape and placement of each nanostructure, or are only the bulk or average properties of interest? Does the structure need to be coherent or deterministic only locally, or is long-range coherence required? Does functionality necessitate precise spatial relationships between all the nanostructures in the device? Given these different requirements and the 4-dimensional space (resolution, throughput, defectivity/complexity and cost) that nanotechnology lives in, it is clear that the required metrologies will need to be diverse and flexible. There is however a constraint that is common to all nanomanufacturing: the cost of the metrology must be consistent with the selling price of what is being manufactured. If you make something that is cheap then you have to make (and sell) a lot of it to stay in business which implies high throughput and potentially the need for high speed metrology. In a 24/7 manufacturing operation, which is the common mode of operation of the IC industry, to generate a revenue of R dollars per year per tool or fabrication line, given a selling price of P dollars per square meter, the throughput (of product meeting specification) must be $R/(3 \times 10^7 P)$ meters squared per second. **Figure 3** graphically illustrates this relationship. In order to achieve a given yearly revenue at high throughput (the right-hand end of the graph) the selling price per square meter can be fairly low whereas at extremely low throughput (the left-hand end of the graph) the selling price per square meter must be extremely high.

To guarantee revenue requires guaranteeing yield (a high enough fraction of product must meet specification), and guaranteeing yield requires a combination of metrology and process control. Two distinct types of metrology are necessary. One is the detailed, in-depth, relatively slow metrology used to research and develop the process and determine the critical factors that control it, and the second is the minimal, nominally high-speed metrology used to maintain the process once it has been developed.

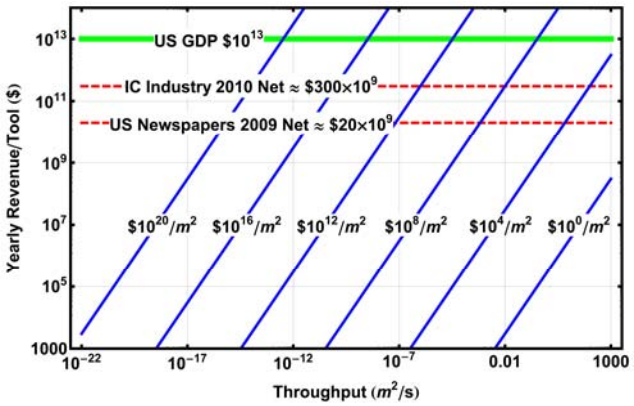

Figure 3. Selling price ($/m^2) versus throughput (m^2/s) showing contours at which various levels of revenue per tool are achieved.

The type of metrology that is needed depends on the structure and function of the product. Ideally one would like to measure the device being fabricated in the way it will be used but often this is not possible. For example in IC manufacturing it's the electrical properties that count but multiple process steps are required to complete the device and during manufacturing its electrical properties cannot be measured directly. Instead CDs, overlay and other indirect measurements are used to verify that fabrication is proceeding as desired. This works in part because of the process stability afforded by the closed-loop control systems in a lithography tool. This tight control of the exposure pattern on the wafer makes it unnecessary to verify the size and placement of every feature. Measuring sample features or fiducials or other ancillary structures is sufficient to maintain process control. This approach allows the metrology to be slow relative to the nominal throughput, but it still must be extremely precise with sub-nanometer spatial resolution which means it is expensive. This expense is balanced by the fact that top-of-the-line logic chips sell for several hundred thousand dollars per square meter and so the metrology costs are still a relatively small percentage of the overall manufacturing cost. After completion, IC chips are binned for speed and functionality using electrical measurements that do indeed test the devices as they are actually used. This final metrology step is critical in allowing the maximum amount of revenue to be extracted from the process. A comprehensive of all aspects of IC metrology, including its impact on revenue, is given by Bunday et al.[117]

In contrast to ICs, many of the novel types of nanomanufacturing currently being developed will produce products worth from only a few cents to a few dollars per square meter and so the necessary metrology must cost significantly less, though of course amortized over the correspondingly higher throughputs. Fortunately, many of these nanofabrication techniques such as block copolymer self-assembly, colloidal self-assembly, DNA origami, roll-to-roll nano-imprint lithography (R2RNIL),[118] etc., will not require the same level of perfection as ICs to meet specification. One major difference is that many of nanostructures being developed are single layer and so do not require aligning one layer on top of another. This obviates the need for alignment systems and overlay metrology. Examples of such structures include masters for bit-patterned hard disk drives, and gratings and wire-grid polarizers[119] fabricated by R2RNIL. In all these cases the goal is to produce a specific material pattern in a single layer of material on an unpatterned substrate. These three different structures differ in the level and type of perfection required. For the hard disk master mold every feature must be sized, shaped and placed within a given tolerance. This will be slow and require the type of costly nanoscale metrology that can yield this level of detail. Since the master will be used as an imprint mold to make on the order of 10,000 daughter molds, which will themselves make 10,000 imprints, the metrology cost is significantly amortized. This is similar to the masks used in IC lithography. There the metrology required to guarantee the perfection of an IC mask is also slow and expensive but this cost is amortized over the number of wafers printed using the mask. However, it is interesting to note that the degree of perfection required in bit patterned media in terms of physically defective bits[120] is approximately 10^{-4}, corresponding to a defect density of $\approx 10^{11}/m^2$ for a 160 Gbit/cm^2 (1 Tbit/in^2) storage density, eight orders of magnitude higher than that for electrical defect densities for ICs ($\approx 10^3/m^2$).[121] This fact is likely to have an impact on the defect inspection requirements, and may possibly permit the use of lower-cost measurement techniques overall.

For the wire-grid polarizers and the gratings it is only the average or bulk properties that count. Wire-grid polarizers are used at wavelengths significantly larger than the feature size of the pattern. Gratings are used with wavelengths that are at the same scale or smaller than the feature size or grating periodicity but the light beam covers many grating periods simultaneously. Hence in both these cases local errors in the pattern are generally tolerable. This should again be contrasted with an IC where it is the slowest transistor in the critical delay path, and not the average transistor speed, that sets the overall speed of the chip.

ICs, photonic structures and hard disk drives all require long range order or coherence. On the other hand nanostructures that are separated from the substrate after production or are produced volumetrically in bulk do not require long range coherence. As discussed earlier, nanoparticles can be fabricated by top-down methods, but are also made in significant quantities by bottom-up approaches. In both instances, measurements of particle size and shape and the distributions of those quantities are needed. However, in the top-down case, the types of metrology tools and the sampling approaches employed in IC fabrication are appropriate, based on the kinds of critical factors involved in the process. Particles fabricated by bottom-up methods, which depend on a very different set of critical process factors, are not amenable to this approach. In this case, optimum control would likely be achieved with close-to-real-time measurements techniques such as static and dynamic light scattering.[122]

All the standard metrology approaches from optical

microscopy to electron microscopy to proximal-probe techniques will continue to be used for the research and development of the fabrication process. But which technique or combination of techniques will be used in production, and exactly how and when the measurements are made, will be determined by the requirement to minimize cost while maintaining process control. In the IC industry the workhorse metrology tool for CD measurement is the scanning electron microscope (SEM). It has nanometer resolution and is sufficiently fast to keep up with the process flow. Although ICs have large sectors that are periodic, the features are far too small to be imaged with standard far field optical microscopy. Near-field optical probes, which avoid the diffraction limit, as do mechanical probes such as atomic force microscopes (AFMs), can be used but they are currently prohibitively slow. It is important to note that the "resolution" required of a metrology tool is not the same as that of the patterning method being measured. As an example, overlay measurements are normally performed using optical images of "box-in-box" targets, in which the feature sizes are on the scale of micrometers and the resolution of the optics is at a similar level. Nevertheless, by making a very high signal-to-noise measurement, overlay measurements can be performed to sub-nanometer precision.

Such an example suggests that metrology of nanoscale structures may be accomplished with tools having an intrinsic resolution much larger than the features being interrogated. Optical scatterometry is such an approach which works on these small periods using more or less the full range of visible wavelengths.[123] In this case the intensity of the light reflected from a periodic fiducial structure on the wafer is measured as a function of wavelength and/or angle. (When the period of the structure is less than the wavelength of light there is only a specular reflection from the structure. All the grating diffraction orders are evanescent, though variations in intensity with angle may still be observed in the zero-order reflection.) The nominal size, shape, period, index of refraction, etc., of this structure are known but the precise values of the parameters of interest, such as feature width, thickness, edge slope etc., are not. To determine the precise values of these parameters an electrodynamic simulation is used to compute how the intensity varies as a function of these values. The values that produce an intensity distribution that most closely matches the measured one are then taken to be actual values.

This procedure can be verified or calibrated by comparing the result to SEM measurements of the same feature and results indicate that the value predicted by this approach can in some cases be precise to the sub-nanometer level. The reason a fiducial periodic pattern such as a simple grating is used is because the number of parameters that must be varied in the simulation can be kept to a minimum and the simulation can be done in just two dimensions. In principle it would be possible to perform scatterometry on the real pattern but this would require fitting many more parameters and doing the full electrodynamic simulation in three dimensions. Not only is this slow, but there is a uniqueness problem: the larger number of fitting parameters makes it possible to find multiple solutions all of which reproduce the intensity data equally well. Finally, we note that scatterometry produces only the average values of the various parameters. It can be used to estimate the root mean square deviations in these parameters as well, but that requires a combination of more measurements and computation. Given that in scatterometry the precise device geometry is computed it can be said to produce images in computation space. An extension of the technique is the through-focus scanning optical microscope (TSOM)[124] that, by using intensity distribution data collected from a series of focal planes, is capable of detecting variations in individual nanoscale particles.

Finally for periodic structures, if a wavelength much smaller than the period is used, then multiple diffraction orders will be generated as in x-ray diffraction from crystals. The position and amplitude of these orders is directly related to the spatial frequency content of the structure and so this type of image is said to be in reciprocal space. With sufficient knowledge about the nominal properties of the structure, as with scatterometry, this information can be transformed back to real space to yield details about not only feature size, placement and spacing but also about roughness and other deviations from perfection.[125] Note that scatterometry and short wavelength (x-ray) diffraction can in principle be used on any periodic or quasi-periodic structure such as those of a bit-patterned media hard disk drive[126] and, as we have seen, many applications of nanomanufacturing require just such structures. Non-periodic structures still present a considerable challenge.

Summary

We have been able only to give a superficial view of all the lithographic tools and techniques that are used in nanostructure fabrication. However, it seems clear that, although the IC industry still dominates nanomanufacturing, the development of novel high-speed, top-down and directed self-assembly patterning methods is poised to enable a whole range of nanotechnology applications. For this to happen, a new suite of metrology tools and methods must be developed. There is a need to establish measurement schemes in order to first understand the process fundamentals, often *in situ* and with nanoscale or even atomic spatial and chemical resolution and in real time. Secondly, once the critical factors have been identified, novel approaches are necessary to enable closed-loop process control to handle the unique challenges posed by the high-throughput manufacturing of nanostructures.

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The full description of the information in this paper requires the identification of certain commercial products and their suppliers. The inclusion of such information should in no way be construed as indicating that such products or suppliers are endorsed by NIST or are recommended by NIST or that they are necessarily the best instruments or suppliers for the purposes described.

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