Graphene production for electrical metrology

(Wytwarzanie grafenu na potrzeby metrologii elektrycznej)

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Since 1990 the representation of the unit of electrical resistance has been based on the integer-quantized resistance plateaus of the QHE occurring in two-dimensional electronic states. These quantized values of resistance are $R_H(i) = R_{K-90}/i$, where R_H is the quantized Hall plateau resistance, R_{K-90} is the 1990 recommended value of the von Klitzing constant, and i is an integer quantum number [1]. In the first years after the discovery of the QHE in 1980, Si-MOSFETs and semiconductor heterostructures (most usually of GaAs/$Al_xGa_{(1-x)}$ As) were used for metrological characterization and comparison [2–4], and more recently several National Metrology Institutes have developed and refined recipes for growing semiconductor QHE devices suitable for precise resistance metrology at relatively high currents and weak magnetic fields [5, 6] so that the standard is more readily accessible and metrologically useful. It is not a simple process to produce devices that are well-quantized on the $i = 2$ plateau for relatively low magnetic flux ($B < 9$ T), while operating at source-drain (S-D) currents of 20 μA to 100 μA and at temperatures $T \geq 1.4$ K. This requires difficult-to-reproduce material composition in GaAs/$Al_xGa_{(1-x)}$As heterostructures such that the electron mobility is intentionally lowered by impurities to increase the plateau width while a relatively high carrier concentration is maintained [1]. In addition, metallic contacts must be diffused into the device layers of heterostructures, and it is often difficult to obtain multiple, highly conductive contacts using modern lithographic techniques.

Since the discovery of graphene using the micromechanical cleavage technique [7], several other relatively simple methods have been developed to produce carbon-based 2DEG (two dimensional electron gas) devices which exhibit QHE plateaus. Some of the most significant features for fundamental physics occur due to the unique electronic state in monolayer graphene, in which the single-particle band structure gives both electrons and holes the characteristics of relativistic Dirac fermions with, for example, a very wide separation between the lowest Landau energy levels. For some monolayer graphene devices, this contributes to broadening or pinning of the $i = 2$ QHE plateau [8, 9] and may result in devices that are well-quantized for precision metrology at significantly higher temperatures, higher currents, or lower B fields than conventional semiconductor QHE devices. In contrast to heterostructure devices, where the 2DEG is buried inside a semiconductor, the conducting channel in graphene devices can reside on the surface of a substrate, and thus it can be microscopically scanned and characterized using surface-science techniques. Moreover, direct fabrication of electrodes on the exposed surface allows for electronic transport measurements in a variety of configurations. With the use of atomic force microscopy (AFM), low-energy electron microscopy (LEEM) [10], scanning tunneling microscopy/spectroscopy (STM/STS) [11] and Raman spectroscopy, graphene devices allow the collection of data on the relationship between detailed morphology and microscopic electronic structure in the anomalous QHE state in graphene.

Considerations for electrical metrology

Typical dimensions of the conducting channel in metrological heterostructure QHE devices are $L = 5$ mm and $W = 0.5$ mm. QHE plateau resistance measurements can be influenced by the size or shape of the device through localized self-heating near the current contacts, a possible length consideration, or non-equilibrium edge states in contact arms, which can occur for small contact area. Devices with larger separation between longitudinal voltage contacts allow more accurate measurements of the longitudinal resistivity, ρ_{xx}, which should be as low as 10 μΩ for the most precise measurements of the Hall resistivity ρ_{xy} [12]. Thus for most resistance metrology the use of exfoliated graphene is precluded since only small monolayer flakes can be obtained. To produce larger devices it is apparent that controlled epitaxial growth methods are necessary. Two methods that utilize self-organization of graphene layers are CVD on metals such as Cu or Ni and epitaxial growth on SiC by thermal disassociation followed by Si sublimation [13].

Of these two processes, the advantage of synthesis on SiC is that the substrate can be insulating and electrical measurements are possible without transferring the graphene to another surface for device fabrication. For ideal graphene coverage to occur on SiC, the surface should be uniform enough for a continuous process of step-flow growth. This requires that the wafer be nearly defect-free and that the surface should be prepared to approach atomic-level flatness, interrupted only by the unavoidable effects of the miscut angle. Surface etching of nominally on-axis, polished 4H- and 6H-SiC(0001) by flowing H_2 gas at temperatures of 1400°C to 1700°C can result in the desired surface reconstruction by evaporation/condensation [14] and formation of atomically-flat terrace steps that are one or more unit cell in height, with the preferred orientation of steps in the (1−100) directions [15].

Single-crystal SiC wafers cut with (0001) surface orientation have Si-terminated and C-terminated basal planes and graphene growth at elevated temperature occurs at different rates on these two wafer faces. On the Si-face, the first layer is a graphene-like non-conducting interface layer with covalent bonding to the substrate. In subsequent Si-face layers true graphene electronic structure is present, and in the unperturbed state several conducting layers may have n-type doping due to charge transfer from the SiC [16, 17]. The SiC graphene-synthesis process begins at temperatures above about 1200°C in high vacuum or at higher temperatures in inert background gas [16] where sublimation is inhibited by collisions. The use of Ar or other inert background gas helps to control the growth rate and can reduce the number of initiation sites, allowing controlled few-layer graphene synthesis on the Si-face at process temperatures from 1600 to 2000°C [18]. Such high temperatures in turn favor additional surface reconstruction and the formation of large homogeneous terraces (step bunching). This technique has been used by several groups [11, 19] to achieve high mobility and broad QHE plateaus.

The above ambient and SiC-substrate conditions appear to allow large-scale graphene synthesis with good control over the number and uniformity of atomic layers, sometimes limited only by the size of the substrate. Thus, in our laboratory at the National Institute of Standards and Technology (NIST) in Gaithersburg, MD, we are installing a 2100°C inert gas/vacuum furnace for etching and annealing SiC substrates. The furnace chamber pressure and temperature will be controlled by a computer interface (RS-485) with separate control of background gas flow and outlet pumping speed. We will seek to produce epitaxial monolayer graphene with high charge carrier mobility favorable for the QHE, as well as large domains which maintain good homogeneity in mobility and carrier density. In particular, the QHE may require relatively uniform electron-hole homogeneity near the Dirac point, or equivalently a low density of electrons plus holes in the graphene layer when the entire region is charge neutral [20].

Characterization and Measurement

Recently, using various samples synthesized in our collaborators' laboratories, we have developed methods for efficient fabrication and characterization of few-layer graphene (FLG) devices. The graphene was grown by chemical vapor deposition (CVD) and epitaxial SiC processing. Most steps in the device fabrication process are already available at NIST and we can quickly profile the room-temperature mobility after fabricating gated graphene devices to estimate the FLG coverage and quality. The microscopic surface morphology can be characterized by collaborators at NIST, Purdue University and Carnegie-Mellon University using Raman Spectroscopy, AFM, LEEM, and other methods. Characterization of magnetotransport and the QHE plateaus can be conducted in magnetic fields of up to 16 T in our laboratory and at higher fields in the U.S. National High Magnetic Field Laboratory (NHMFL) in Tallahassee, Florida. In our laboratory at NIST we have developed two automated methods for our QHE measurements and characterization.

The first is a characterization method using conventional lock-in amplifier techniques, with automatic relay scanners used to connect device terminals to the S-D signal source and two lock-in detectors. The S-D current (I_{SD}) is typically 100 nA (RMS) at 13 Hz. The initial measurement sequence for a gated device is as follows. First the magnet current is ramped to the maximum (or other) level and held constant. Six connections are selected for the S-D pair, longitudinal voltage pair, and Hall voltage pair. One of each pair of voltage probes may be the same. All device connections except for the gate have been shorted to ground until this time, thus avoiding damage to a graphene device when switching connections. The gate bias voltage is ramped from zero to a selected starting value, typically −60 V, and then the I_{SD} measurement and lock-in output signals are recorded after every 0.1 V change as the gate bias is ramped slowly to maximum positive value (60 V). The gate bias is finally ramped to zero and the device terminations are shorted together. These measurements may be made in a 9 T magnet in a ^{4}He cryostat with 0.005 K temperature control from 1.45 to 4.2 K in liquid ^{4}He and in He vapor up to 100 K, or in a 16 T magnet system with ^{4}He/^{3}He inserts, presently used with ^{4}He to 1.4 K. As a design consideration for the following alternate measurement method, all cryostat leads to the QHE devices have resistance values of order 5 Ω.

The second characterization method employs high-precision measurements made with a dc-SQUID based multi-terminal cryogenic current comparator (CCC) which compares the Hall resistance of a device in the vicinity of a plateau against either a standard resistor or a second, well-characterized QHE device in a separate cryostat. This CCC is a resistance-ratio bridge of a type designed at NIST for high resistance scaling and single-electron tunneling measurements [21, 22], modified to allow direct comparison between two QHE devices. The bridge utilizes a multi-terminal configuration [23–25] with bridge connections to six asymmetrically opposing contacts of both QHE devices (*Fig. 1*). Provided that all of these parallel-circuit measurement leads and associated QHE contacts have resistances of order 5 Ω or less and the device longitudinal resistance is also similarly small, this multi-terminal QHE measurement can have an insignificantly small difference from conventional 4-terminal CCC measurements that require a nanovolt detector [9]. Direct comparisons between GaAs heterostructures can achieve a relative measurement uncertainty of 3×10^{-9} with this system. The resistance values shown in the graph of *Fig. 2* are measured from a GaAs device in a slow sweep of the magnetic flux through the region of the $i = 2$ plateau in our 9 T magnet. The device used as the reference for this data was a characterized NIST GaAs QHE standard at the center of the $i = 2$ plateau at fixed magnetic flux density of 10.4 T. A set of sweeps similar to that of *Fig. 2* were carried out at several different temperatures for a second uncharacterized GaAs device, as shown in *Fig. 3*. This shows the variation in the plateau magnetic flux profile and the loss of quantization at progressively higher temperatures.

Graphene devices with Hall mobilities in the range of 0.02 m²/Vs to 0.4 m²/Vs have been provided by our collaborators to support our development of graphene QHE characterization and analysis. The data in *Fig. 4* shows the typical temperature dependence of resistance at low S-D current for a graphene sample grown on Cu foil by CVD and transferred to a SiO_2/Si substrate [26]. The fabricated Hall bar device has a width of 4 μm and length of 60 μm. Resistivity was measured using a standard lock-in technique in a ^{3}He cryostat with a perpendicular magnetic field up to 18 T, using facilities at the NHMFL. The carrier mobility is around 0.37 m²/Vs. It can be seen from *Fig. 4* that even at 70 K, the $i = 2$ plateaus for both electrons and holes are still well defined, showing the potential of graphene as a quantum resistance standard that can work at much higher temperatures than at present, compared to conventional heterostructure Hall bar devices.

In-depth device electrical characterization of the QHE in graphene will include CCC sweeps and other measurements to fully determine ρ_{xy} and ρ_{xx}, by measuring R_{xy} on all transversely opposed pairs of contacts and R_{xx} values between all contacts on each side of the device. These comprehensive measurements help to define the homogeneity and the extent of quantization in the 2DEG region. Graphene presents greater challenges for characterization than GaAs heterostructures, since the gate voltage and possible changes in the carrier concentration represent additional or possibly time-dependent variables that affect graphene devices. Recent studies [27, 28] are pointing to techniques that can improve the stability and controllability of doping and its effect on the carrier concentration.

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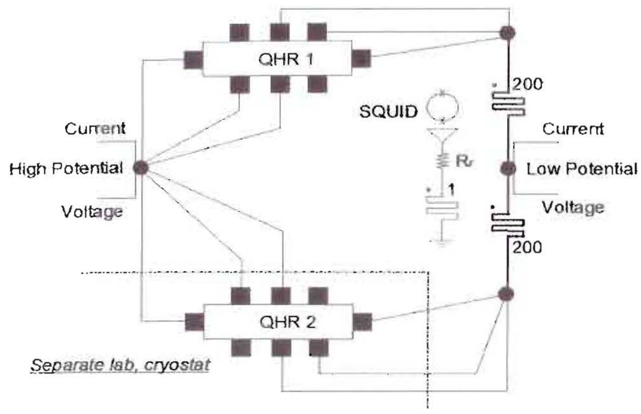

Fig. 1. Diagram of a CCC used to compare Hall resistance values of two QHE devices, with each device approximating the same quantum state (Hall plateau) and in series with a 200-turn detection winding. A characterized GaAs heterostructure is used as the reference, typically with the magnetic flux density held constant at the center of a well-quantized plateau. The CCC bridge connections and windings represented by the filled circles and thick lines are superconducting interconnections, in order to correctly define and equalize the potential across the central terminal pairs of the two QHE devices

Rys. 1. Schemat CCC wykorzystany do porównania wartości rezystancji Halla dwóch próbek QHE, a stan kwantowy (plateau Halla) każdej z nich przyjmuje się tak sam, razem wraz z włączoną szeregowo cewką detekcyjną o 200 zwojach. Opisywana heterostruktura GaAs została użyta jako punkt odniesienia, typowo ze stałą indukcją magnetyczną w centrum dobrze skwantowanego plateau. Połączenia mostka CCC i uzwojeń są reprezentowane przez wypełnione kółka oraz grube linie przedstawiające połączenia linii nadprzewodzących, w celu poprawnego określenia i wyrównania potencjału centralnych par zacisków dwóch próbek QHE

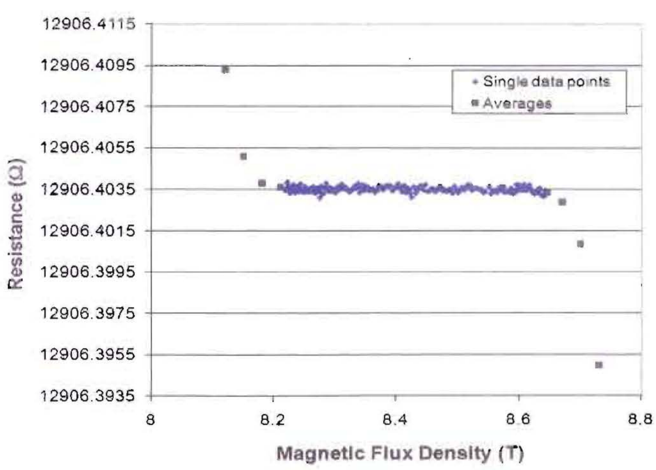

Fig. 2. High-resolution magnetic flux dependence of the Hall resistance for the i = 2 plateau of GaAs-AlGaAs device HH143e at constant temperature T = 1.45 K and S-D current 85.2 μA. A previously characterized QHE device at the center of the i = 2 plateau was used as the reference resistance, at T = 0.32 K. The single data point comparison values shown have relative uncertainties of 4 × 10^{-8} and the average data points have similar uncertainty but are shown only to illustrate the general characteristics of the plateau

Rys. 2. Zależność rezystancji Halla dla plateau i = 2 w funkcji strumienia indukcji magnetycznej w GaAs-AlGaAs próbki Halla nr HH143e w stałej temperaturze T = 1,45 K i dla prądu drenu 85,2 μA. Wcześniej opisaną próbkę QHE pracująca w środku plateau i = 2 wykorzystano jako źródło rezystancji odniesienia, w temperaturze T = 0,32 K. Porównano wartości pojedynczych punktów pomiarowych ze względną niepewnością 4 × 10^{-8} z wartością średnią i otrzymano podobne wartości niepewności. Zostały one pokazane jedynie dla zilustrowania ogólnej charakterystyki plateau

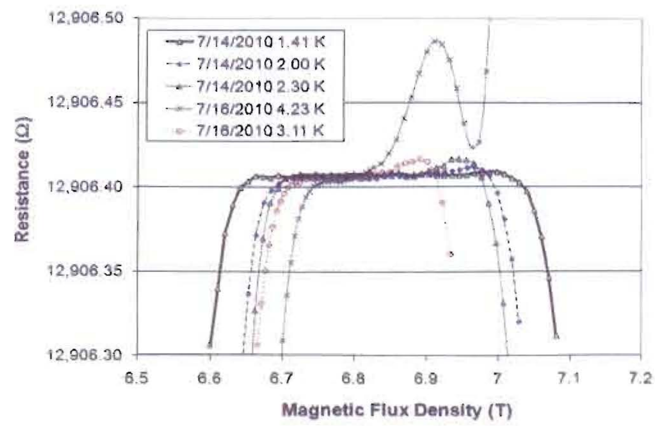

Fig. 3. Temperature dependence of the full Hall resistance profile for the i = 2 plateau of GaAs-AlGaAs device HH138d. The S-D current for all data was 53.6 μA and the device was compared against a calibrated standard resistor using the CCC configuration shown in [22]. The comparison values shown have relative uncertainties of 2 × 10^{-7}, including the uncertainty in the value of the resistor

Rys. 3. Zależność temperaturowa pełnego profilu rezystancji Halla dla próbki Halla nr HH138d wykonanej z GaAs-AlGaAs i dla plateau i = 2. Prąd drenu we wszystkich pomiarach wynosił 53,6 μA, a parametry próbki porównano ze skalibrowanym rezystorem wzorcowym. Układ porównania to komparator CCC opisany w [22]. Przedstawione wartości są obarczone względną niepewnością 2 × 10^{-7}, przy uwzględnieniu niepewność rezystancji rezystora

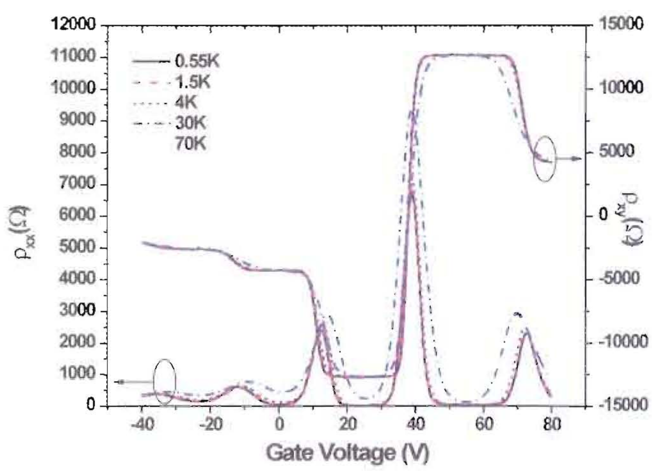

Fig. 4. Temperature dependence of the longitudinal resistivity ρ_{xx} and Hall resistivity ρ_{xy} of a CVD graphene Hall device as a function of the back gate voltage at 18 T, with back gate sweeps at five different device temperatures. The S-D current for all data was 100 nA. Data at temperatures of 0.5 K and 1.55 K overlap at this resolution. QHE plateaus near ρ_{xy} = 12.9 kn and 4.3 kn indicate that the conducting channel is primarily monolayer graphene. The graphene material for this device was grown on Cu foil by CVD and then transferred to a SiO_2/Si substrate at the University of Houston. The 4 μm × 60 μm Hall bar was fabricated at NIST

Rys. 4. Temperaturowa zależność wzdłużnej rezystancji ρ_{xx} i rezystancji Halla ρ_{xy} próbki grafenowej CVD w funkcji napięcia wstecznego bramki w polu magnetycznym 18 T, dla pięciu różnych temperatur. Prąd drenu wynosił 100 nA we wszystkich pomiarach. Wyniki pomiarów w temperaturze 0,5 K i 1,55 K pokrywają się w granicach rozdzielczości pomiaru. Plateau QHE w pobliżu ρ_{xy} = 12,9 kn oraz 4,3 kn oznaczają, że kanał przewodzący przede wszystkim stanowi jednocząsteczkową warstwę grafenu. Grafen w tej próbce został wytworzony na folii Cu przez CVD, a następnie przeniesiony na podłoże SiO_2/Si na Uniwersytecie w Houston. Pasek Halla o rozmiarach 4 μm × 60 μm został wyprodukowany w NIST

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